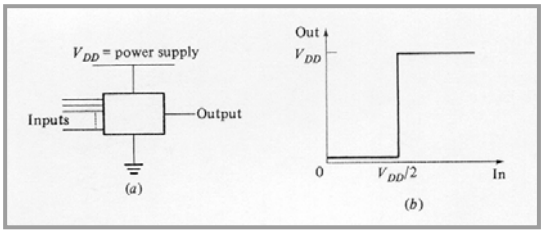
Addendum: Digital Integrated Circuits

ECE 152A – Fall 2006

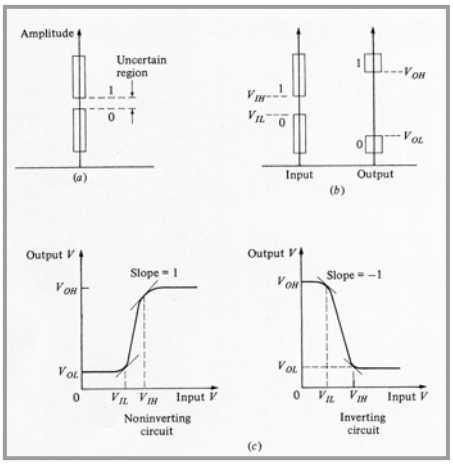
Properties of Digital Integrated Circuits

- The Ideal Digital Circuit



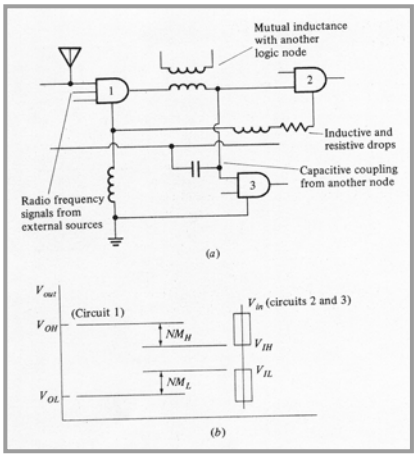
Digital IC Definitions

- Amplitude and Voltage Transfer Characteristics



Digital IC Definitions

- Noise Margins
  - Sources of noise
  - Definition of noise margins



TTL Electrical Characteristics

- Standard TTL (54/74)

TABLE 7.3
Standard transistor-transistor logic (54/74 TTL): typical electrical characteristics at $T_A = 25°C$

V_{OH}/V_{OL}	3.5 V/0.2 V	Fan-out	10
V_{IH}/V_{IL}	1.5 V/0.5 V	Supply volts	+5.0 V
NM_H/NM_L	2.0 V/0.3 V	Power dissipation per gate	10 mW
Logic swing	3.3 V	Propagation delay time	10 ns

TTL Electrical Characteristics

- Comparison of Standard TTL (74), Schottky Clamped TTL (74S) and Low Power Schottky TTL (74LS)

TABLE 7.4
Transistor-transistor logic: performance characteristics at $T_A = 25°C$

	Series 74	Series 74S	Series 74LS
min V_{OH}/max V_{OL}	2.4 V/0.4 V	2.7 V/0.5 V	2.7 V/0.5 V
min V_{IH}/max V_{IL}	2.0 V/0.8 V	2.0 V/0.8 V	2.0 V/0.8 V
min I_{OH}/min I_{OL}	−0.4 mA/16 mA	−1.0 mA/20 mA	−0.4 mA/8 mA
max I_{IH}/max I_{IL}	40 μA/−1.6 mA	50 μA/−2.0 mA	20 μA/−0.4 mA
Typical propagation delay time	10 ns	3 ns	10 ns
Typical power dissipation per gate	10 mW	20 mW	2 mW

TTL vs. CMOS

- Comparison of Electrical Characteristics

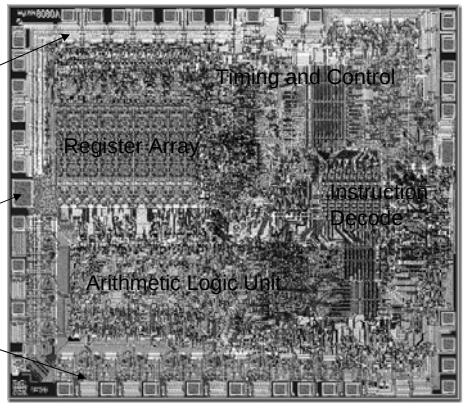
TABLE 3.2
Bipolar and CMOS logic performance characteristics ($T_A = 25°C$)

	Series				
Parameter	**74LS**	**74HC**	**74HCT**	**74AC**	**74ACT**
min V_{OH}/max V_{OL}:					
CMOS load	2.7/0.5	4.4/0.1	4.4/0.1	4.4/0.1	4.4/0.1
TTL load	2.7/0.5	4.0/0.3	4.0/0.3	3.9/0.3	3.9/0.3
min V_{IH}/max V_{IL}	2.0/0.8	3.1/0.9	2.0/0.8	3.1/1.3	2.0/0.8
min I_{OH}/min I_{OL}, mA	−0.4/8	±4	±4	±24	±24
max I_{IH}/max I_{IL}, μA	20/−400	±0.1	±0.1	±0.1	±0.1
Typical t_P, ns	10	10	10	5	5
Typical dc P_D/gate	2 mW	2.5 μW	2.5 μW	2.5 μW	2.5 μW

For Series 74LS: $V_{CC} = 5$ V $C_L = 15$ pF
For CMOS Series: $V_{CC} = 4.5$ V $C_L = 50$ pF

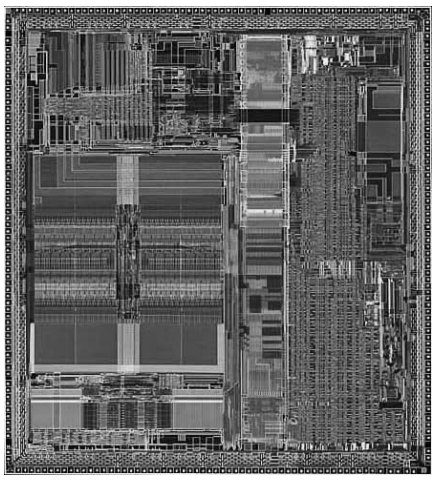
VLSI Circuits

- Intel 8080



VLSI Circuits

- Intel Pentium



Power Dissipation in CMOS Circuits

- There are two components that establish the amount of power dissipation in a CMOS circuit
  - Static Power Dissipation
    - Constant current
  - Dynamic Power Dissipation
    - Currents attributed to switching

Power Dissipation in CMOS Circuits

- Static dissipation
  - Reverse bias leakage current
    - Parasitic diode between diffusion regions and substrate
  - Subthreshold leakage current in static CMOS circuits
    - pMOS and/or nMOS devices not completely turned off
  - Constant current in non static CMOS circuits
    - Psuedo-nMOS, I/O, Analog circuits, etc.

Power Dissipation in CMOS Circuits

- Dynamic dissipation
  - Switching transient current
    - Occurs on transition from 1 to 0 (or 0 to 1)
      - Results in short current pulse from V_{DD} to V_{SS}
      - Referred to as “short-circuit dissipation”
    - Dependent on rise and fall times
      - Slow rise and fall times increase short circuit current
    - Critical in I/O buffer design
      - Dominant component of dynamic power with little or no capacitive loading

Power Dissipation in CMOS Circuits

- Dynamic dissipation (cont)
  - Charging and discharging of load capacitances
    - As capacitive loading is increased, the charging and discharging currents begin to dominate the current drawn from the power supplies

$$P_d = \frac{1}{t_p}\int_0^{t_p/2} i_n(t)\,V_{out}\,dt + \frac{1}{t_p}\int_{t_p/2}^{t_p} i_p(t)\,(V_{DD} - V_{out})\,dt,$$

where

i_n = n-device transient current

i_p = p-device transient current.

Power Dissipation in CMOS Circuits

- Dynamic dissipation (cont)
  - Charging and discharging of load capacitances

For a step input and with $i_n(t) = C_L\, dV_{Vout}/dt$ (C_L = load capacitance)

$$P_d = \frac{C_L}{t_p}\int_0^{V_{DD}} V_{out}\,dV_{out} + \frac{C_L}{t_p}\int_{V_{DD}}^{0} (V_{DD} - V_{out})\,d\,(V_{DD} - V_{out})$$

$$= \frac{C_L V_{DD}^2}{t_p}$$

with $f_p = 1/t_p$,
resulting in

$$P_d = C_L V_{DD}^2 f_p.$$

Power Dissipation in CMOS Circuits

- Dynamic short-circuit vs. capacitive current

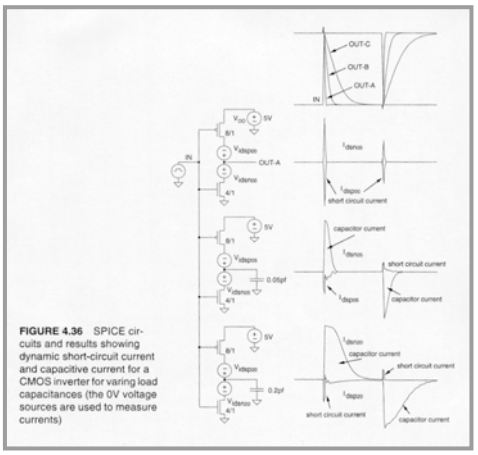


FIGURE 4.36 SPICE circuits and results showing dynamic short-circuit current and capacitive current for a CMOS inverter for varing load capacitances (the 0V voltage sources are used to measure currents)