```
module test_taillights();
reg   clock, left, right, brake, hazards;
wire  tail_lights;
initial begin
      clock = 1;
      left = 0;
      right = 0;
      brake = 0;
      hazards = 0;
      #5 hazards = 1;
      #100 $finish
end

always begin
#5 clock = ~clock;
end

State_Machine G1(tail_lights,clock,left,right,brake,hazards);

endmodule
```