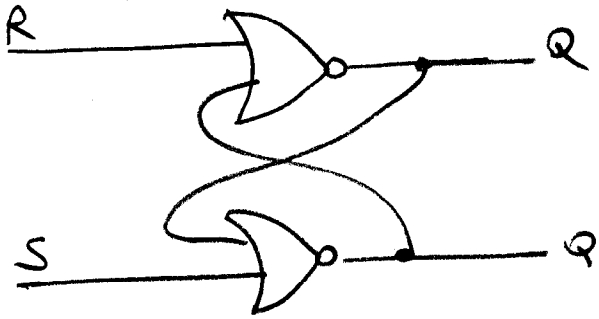
Timing of sequential circuits

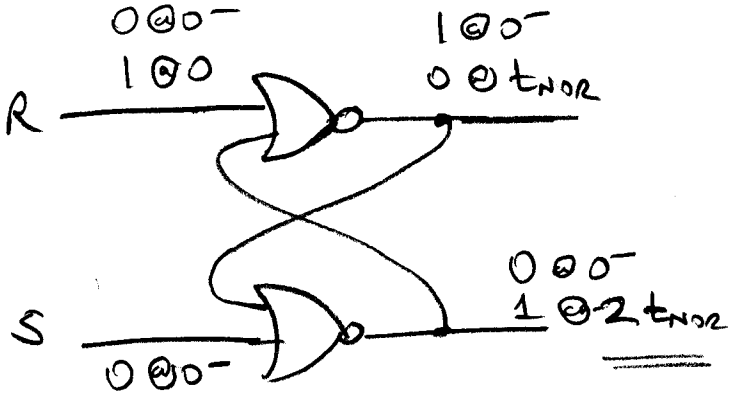
Ex 1] R-S latch ("basic latch"):

- made of cross-coupled NOR gates.



- Max propagation delay of a sequential circuit $\stackrel{\text{def}}{=}$ maximum delay from a change in any of the inputs to a stable vector of outputs (Q and Q'.)

Above:



Transitions to $\begin{bmatrix} R \\ S \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}$ have no delay (since output remains same). Hence, examine: $\begin{bmatrix} 0 \\ 0 \end{bmatrix} \to \begin{bmatrix} 1 \\ 0 \end{bmatrix}$

(and $\begin{bmatrix} 0 \\ 0 \end{bmatrix} \to \begin{bmatrix} 0 \\ 1 \end{bmatrix}$ is symmetric.)

$\therefore$ $\boxed{2t_{NOR}}$ is the maximum prop. delay of the R-S latch.

– can also define:

R-to-Q delay: R to stable Q and Q'.

In this case, this is $2t_{NOR}$. as $\begin{bmatrix}0\\0\end{bmatrix} \rightarrow \begin{bmatrix}1\\0\end{bmatrix}$ is the critical transition

By symmetry, S-to-Q delay is $2t_{NOR}$, as well.
$\begin{bmatrix}?\\0\end{bmatrix} \rightarrow \begin{bmatrix}0\\1\end{bmatrix}$ is a critical transition

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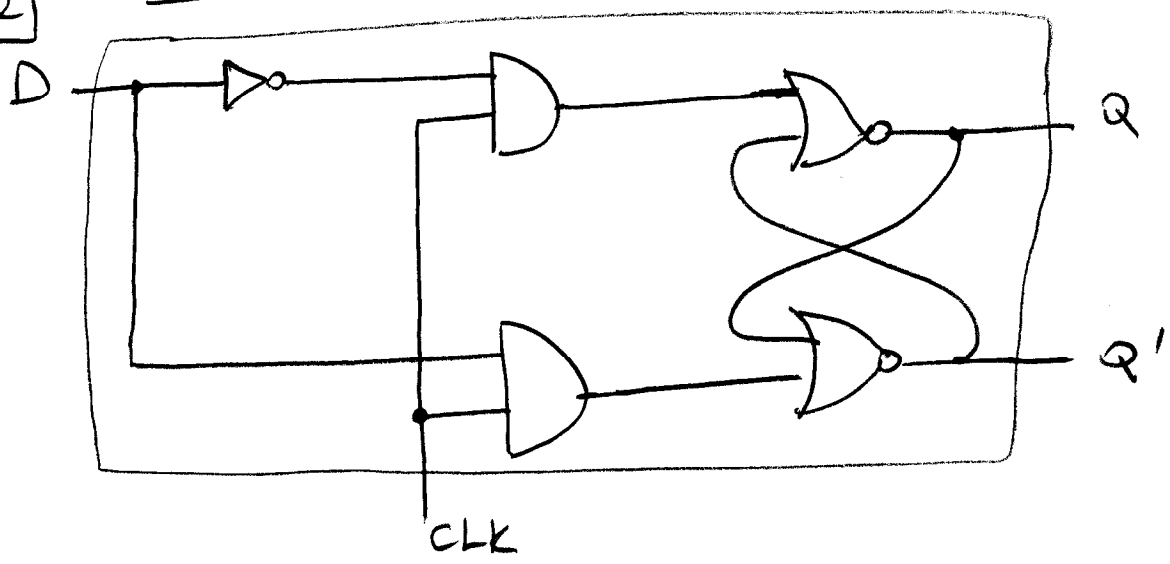
EX 2] (clocked) D latch:



(A) D-to-Q delay: Max. delay incurred from a change in D (all other inputs are held constant) to a stable Q and Q'.

(In this case, CLK is the only other input.)

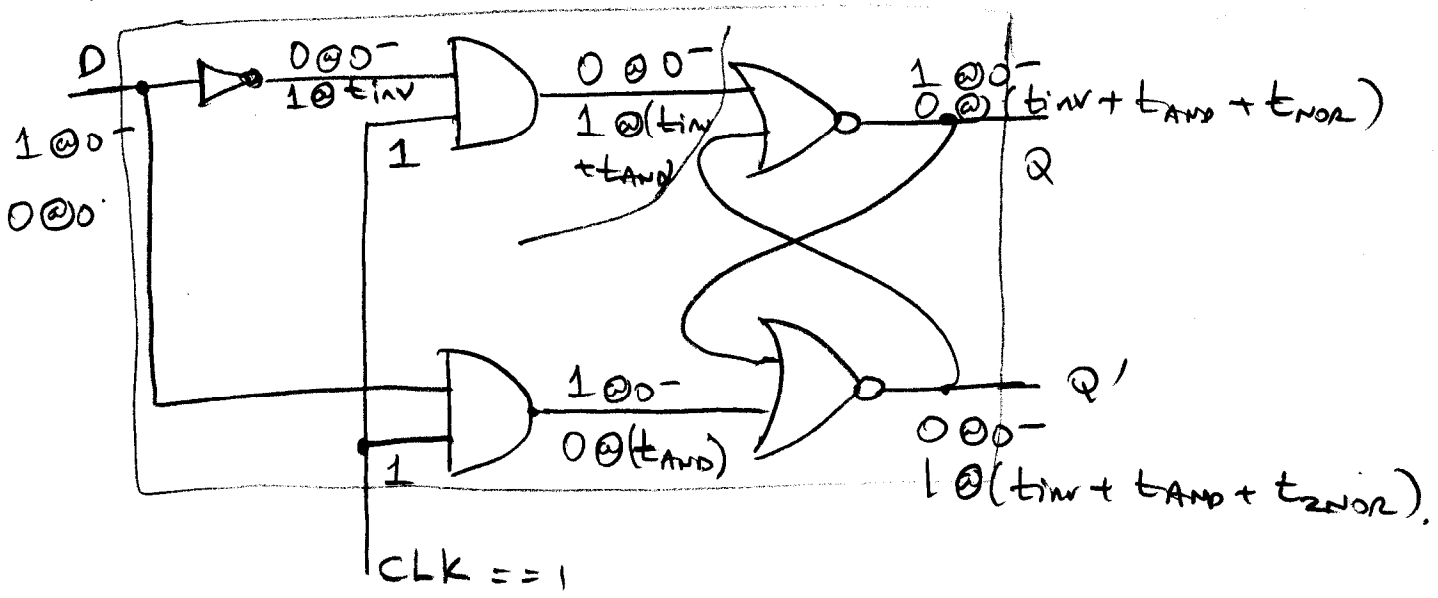
- Note that if CLK == 0, then D will have no effect on the output. ∴ cannot realize max. delay this way.

∴ Let CLK == 1.

- Now, be careful: cannot simply add the max. delay of R-S latch to an AND and INV delay.

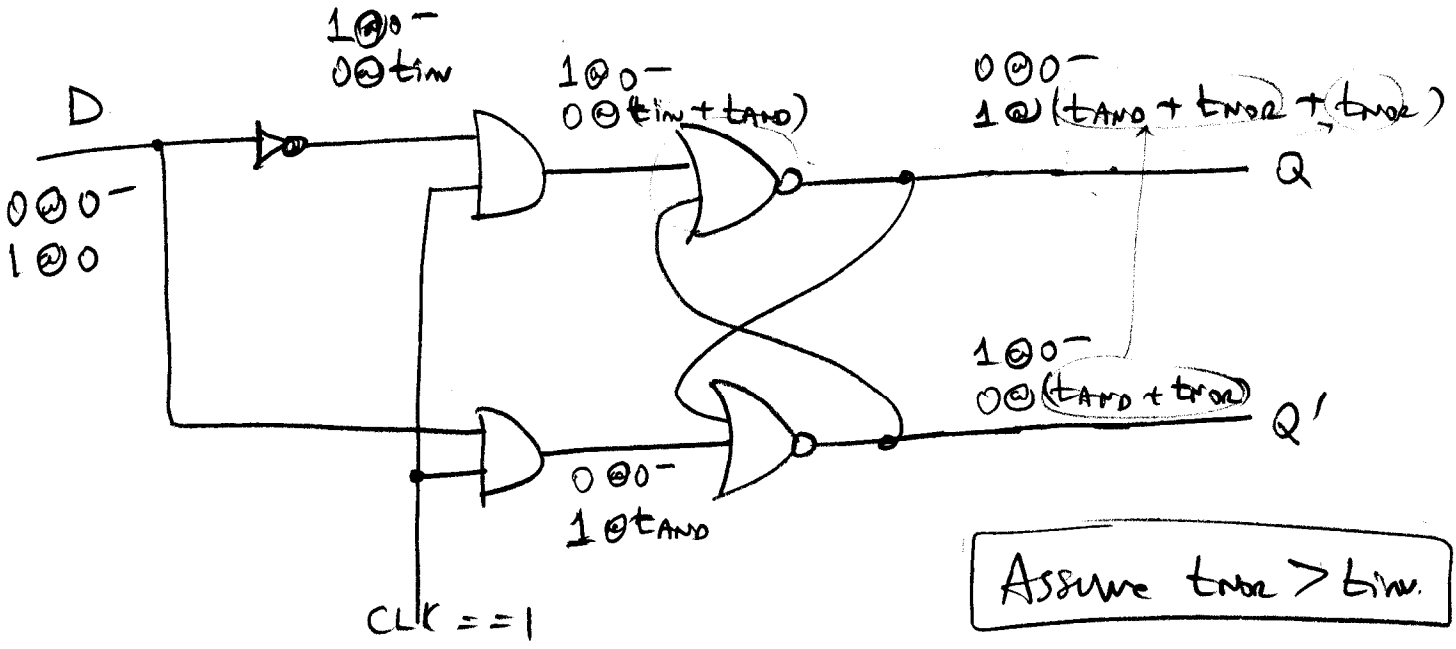
Since $\begin{bmatrix} 0 \\ 0 \end{bmatrix}$ never occurs when CLK == 1,

(a) Examine: D: 1 → 0



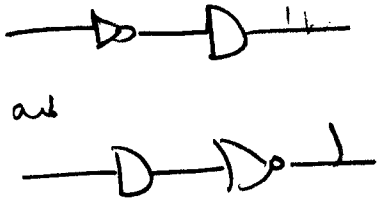
∴ Q' becomes stable @ $(t_{INV} + t_{AND} + 2t_{NOR})$

(b) Examine: $D: D \to 1$ (not symmetric due to inverter delay!)



∴ Q becomes stable @ ($t_{AND} + 2t_{NOR}$)

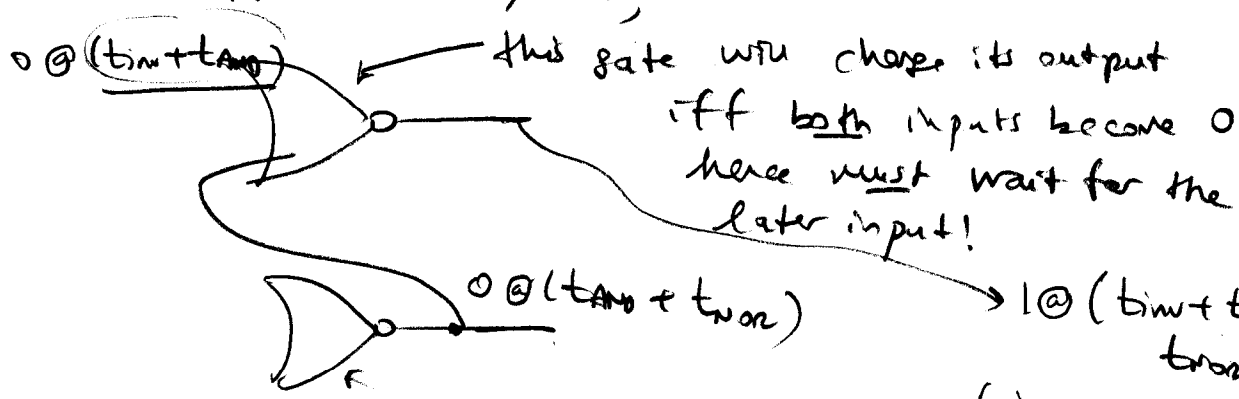
(The inverter delay does not appear because:



both caused changes and $t_{INV} < t_{NOR}$

(∴ inverter delay was absorbed)

[If we had $t_{INV} > t_{NOR}$, then,



then Q stable @ ($t_{INV} + t_{AND} + t_{NOR}$)]

absorbs lower t_{NOR} ↑ upper t_{NOR}

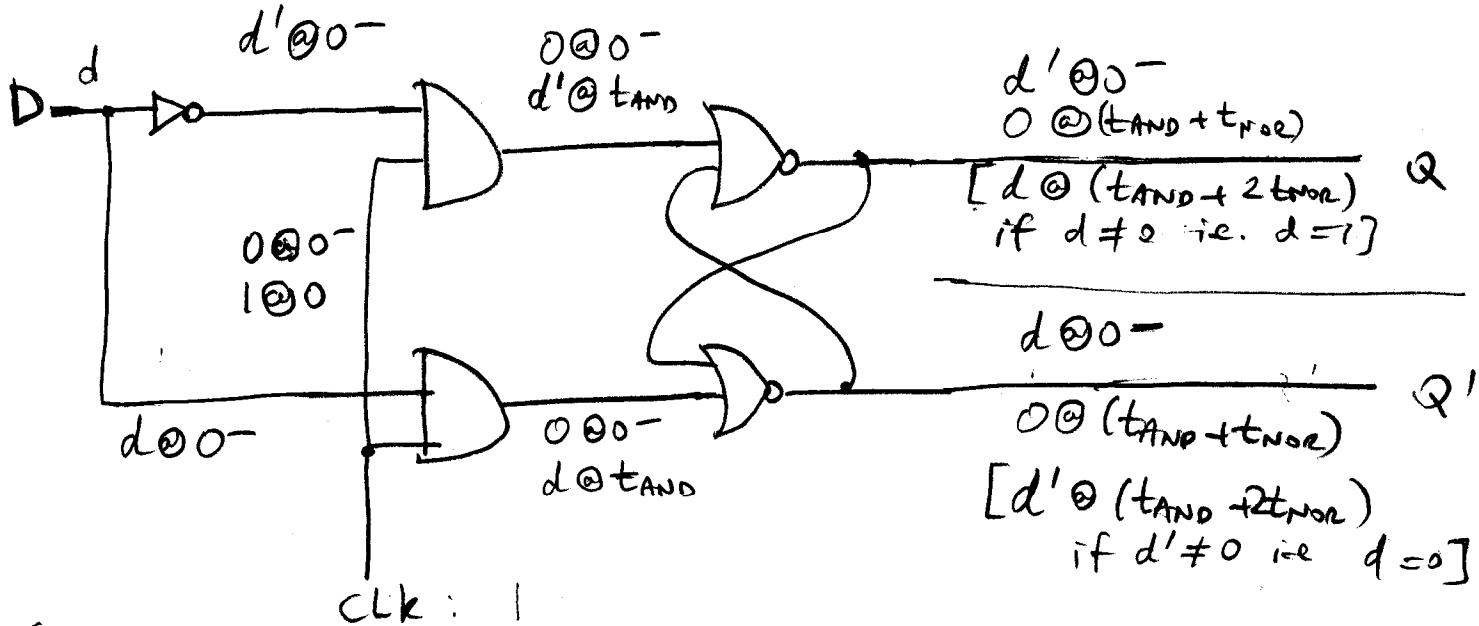
Now,

$$D\text{-to-}Q \text{ delay} = \max\{\underbrace{t_{INV} + t_{AND} + 2t_{NOR}}_{D:1\to0},\ \underbrace{t_{AND} + 2t_{NOR}}_{D:0\to1}\}$$

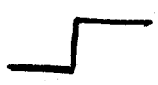
$$= t_{INV} + t_{AND} + 2t_{NOR}$$

with critical transition: $D: 1 \to 0$

(B) CLK-to-Q delay: Max. delay from a change in CLK to stable Q and Q'. (All other inputs (in this case, only D) held stable.)



(a) If CLK: $1 \to 0$: we know, no change will happen in Q. ✓

(b) Examine: CLK goes high. (CLK: $0 \to 1$.)  Positive edge

* Note that inverter delay won't show up because while the CLK was low, the values of these wires were

computed. (∵ I do expect the symmetry to be restored.)

- Second, a change will occur in (Q, Q') iff present D is different from new D. Here assume Q = d' @ 0⁻.

- Following the analysis above,

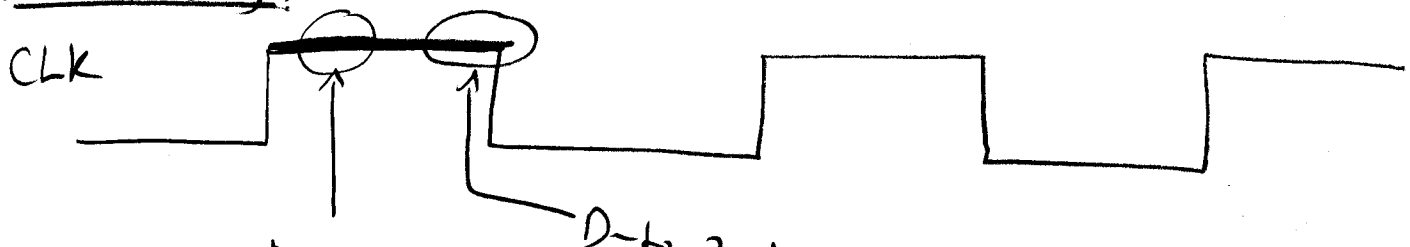
Q or Q' become stable @ $(t_{AND} + 2\,t_{NOR})$

∴ **CLK-to-Q delay = $t_{AND} + 2\,t_{NOR}$**

(OR: observe that the critical transition $\begin{bmatrix}0\\0\end{bmatrix} \to \ldots$ of R-S latch used here.
∴ CLK-to-Q delay = t_{AND} + (delay of R-S latch) = $t_{AND} + 2\,t_{NOR}$)

- Now we should ask: which of the delays is relevant to the operation of the D latch, and under what circumstances?

A) D-to-Q delay:

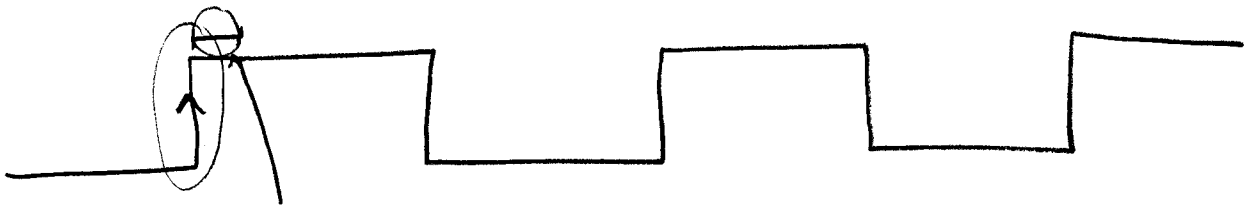


D-to-Q delay irrelevant here since, there is plenty of time remaining to copy D to Q. (clock stays here)

D-to-Q delay starts becoming relevant as you approach the clock edge. — need time to propagate the input D to Q, Q' before CLK ↓

(B) CLK-to-Q delay

CLK: 0 → 1



will take this much time to propagate the D to Q after CLK ↑.

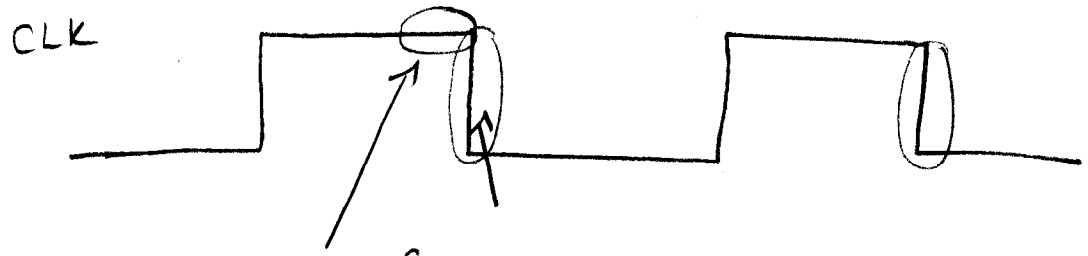
but <u>irrelevant</u> (since there is plenty of time remaining to copy inputs)

<u>unless</u> the CLK period is too short.

∴ we see that the half CLK period (T/2) <u>cannot</u> fall below the CLK-to-Q delay; otherwise won't have time to arrive at stable Q, Q' before the CLK ↓.

Summary for the positive level-sensitive D latch

1- The important clock edge is the <u>falling edge</u>.



must finish copying values to output (i.e. output Q, Q' stable) <u>before</u> the CLK falls!

2- The <u>D-to-Q delay</u> starts becoming important as the falling clock edge nears
(D-to-Q delay = $t_{INV} + t_{AND} + 2t_{NOR}$; D: 1→0 critical)

3- The <u>CLK-to-Q delay</u> (CLK: 0→1) not important unless the CLK period has been made too short.- i.e. places limitations on minimum clock period.)

(CLK-to-Q delay = $t_{AND} + 2t_{NOR}$)

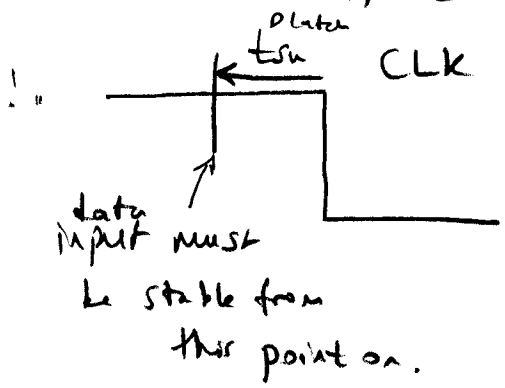
- What happens as we get close to the falling edge?
- If D changes too close to the falling edge, then may not latch correct value.

Hence: ∃ a minimum duration for which the data input has to be stable before the CLK ↓

© <u>Set-up time</u>: (for the level sensitive latch)

≡ minimum duration for which the data input has to be <u>stable</u> before the CLK ↓ such that the latch works correctly.

- We found that for D: 1 → 0, it takes $(t_{inv} + t_{AND} + 2t_{NOR})$ as for D to be propagated to a stable {?, ?!} in worst-case.



(transparent device)

always true <u>for latches</u>

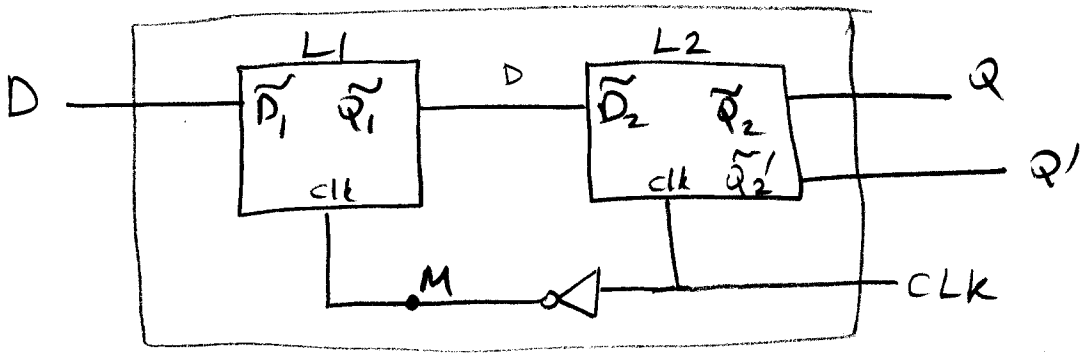
$t_{su}^{D\text{-latch}}$ ≡ max prop. delay Data → stable output (while CLK = =1)

$t_{su}^{D\text{-latch}} = t_{inv} + t_{AND} + 2t_{NOR}$ for D-latch

II D flip-flop

PET

- Assume Master-slave implementation:



(A) D-to-Q delay: if CLK = constant 0, Q unaffected.

if CLK = = 1, Q unaffected

∴ D-to-Q delay not relevant because the flow of D to Q requires CLK to change.

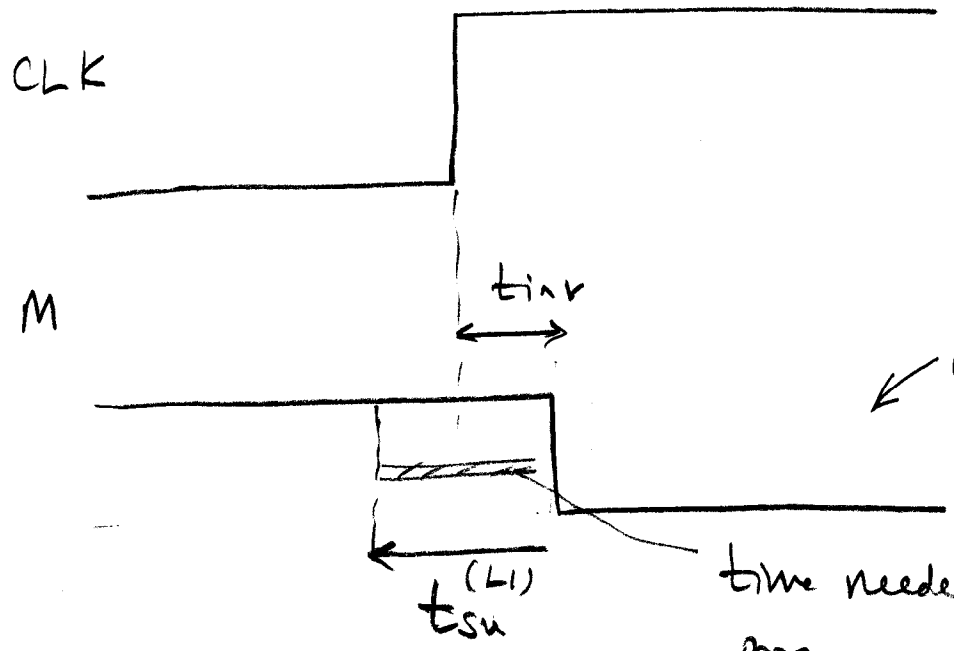
(B) CLK-to-Q delay: – assume D has been stable for a long time.

Key transition: CLK: 0 → 1

Then: $\boxed{t_{CLK-Q}^{(ff)} = t_{CLK\text{-}to\text{-}Q}^{(L2)}}$

$(= t_{AND} + 2t_{NOR})$

(C) Setup time ≡ minimum duration for which D has to be stable before the active edge of the CLK



$$\therefore \boxed{t_{su}^{(ff)} = t_{su}^{(L1)} - t_{inv}} \quad (= \cancel{t_{NR}} + t_{MUX} + 2t_{NOR} - \cancel{t_{INV}})$$

1 – always w.r.t. the active edge of ff. CLK

2 – the inverter buys you time (the falling clk edge arrives "late" due to inverter delays. ∴ buys you time.)