ECE 120A Winter 2016

UNIVERSITY OF CALIFORNIA, SANTA BARBARA

Electrical and Computer Engineering Department

NMOS Transistor Lab Report – due March 16th, 2016 by 5:00 pm

For your final lab project, you will be fabricating an NMOS transistor (*n*-channel MOSFET). Complete instructions for device fabrication are included in the class handouts. While you are fabricating the devices, make sure to perform necessary tests and measurements along the way (i.e. oxide thickness measurements, 4 point probe,…) to make sure your process steps have been successful. Also make sure to take lots of pictures and document your entire process.

Once the fabrication is complete, you will be testing your devices and turning in a lab report (1 report per lab group). However, each person should turn in their own individual 'Discussion of results' and 'Conclusions' (sections IV and V). The lab report should consist of the following:

I. Abstract
  - One paragraph summary of what you did and your results

II. Description and documentation of process
  - Complete description of process, observations, problems
  - Include pictures, other documentation
  - Construct fabrication process flowchart

III. Device characterization. You should include the following data (if not already presented in part II):
  - Field and gate oxide thicknesses (measure by as many techniques as you can and compare)
  - Sheet resistance of substrate and diffused region
  - Contact resistance of ohmic contacts (specific contact resistance in ohm-mm, resistance of the actual contacts in ohms)
  - Junction depth, lateral extent of diffusion (calculate what this should be)
  - *I*-*V* characteristics of MOSFETs (I_{DS}-V_{DS} curves, and I_{DS}-V_{GS} curve at constant V_{DS})
  - V_T of the MOSFETs (can you find V_{FB}?)
  - Breakdown voltage of MOSFETs (measure this after you have completed the other measurements)
  - Transconductance g_m, channel conductance g_d, and output conductance G_D of the MOSFET, estimate the electron mobility in the inversion layer
  - Resistance of resistors and capacitance of capacitors on the wafer
  - *C*-*V* characterization of devices, compare V_T to that calculated from *I*-*V* characteristics (optional)

IV. Discussion of results
  - How do your MOSFET *I*-*V* characteristics compare to physical models? Are they consistent with long-channel and/or short-channel approximations (which of these should they be consistent with?)? Do your curves scale as expected with varying gate lengths and widths? Explain any discrepancies.
  - How do V_T and g_m compare with what you estimated for Al/SiO_2/Si system?
  - Are the resistor values consistent with the contact and sheet resistances calculated from TLM?
  - Are the capacitor values consistent with the measured gate oxide thickness? What value of gate oxide thickness do the capacitor values yield?
  - Key problems you encountered.

V. Conclusions

- One paragraph summary of what you did, what worked well, what didn’t work well, and what you would do differently next time if you had to fabricate a 2nd round of devices.

Note: The above outline is merely a *suggested* format. Feel free to arrange your report however you see fit, as long as all the information is contained within the write-up.