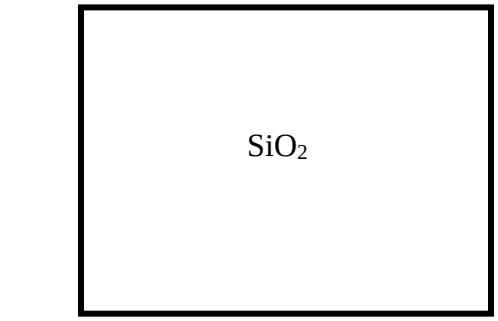
UNIVERSITY OF CALIFORNIA, SANTA BARBARA
Electrical and Computer Engineering Department

NMOS Transistor Lab Pre-Lab – due February 16th, 2016 by 5:00 pm

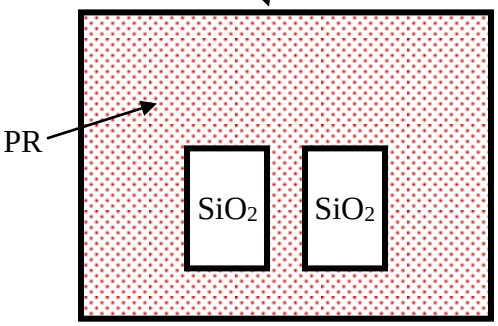
This pre-lab assignment is to be completed individually by each student in the class (this is not a group assignment). Groups may not begin working in the lab on the final project before every member of their group has submitted the pre-lab assignment (if you wish to begin working on the lab earlier, turn in your pre-lab early). Grades on the pre-lab will figure in to the final grade that each individual receives on the final project.

For the pre-lab, draw a flow chart illustrating a TOP VIEW of your transistor for each processing step – this should complement the flow chart illustrating the CROSS-SECTIONAL VIEW of the transistor that the instructor presented in class. Also for each step, include a brief description of the procedures to be carried out for that step. The beginning of this assignment is done for you below:

1. Clean sample, grow 5000 Angstroms of wet oxide on sample. Include [fill in the number] extra samples.



2. Coat [fill in the number] samples with photoresist, expose and develop with mask 1 to expose diffusion regions.



3. Wet etch one of the unpatterned samples from step 1 to determine etch time of oxide. Etch oxide from the exposed window regions to expose underlying Si. Remove PR and clean samples.