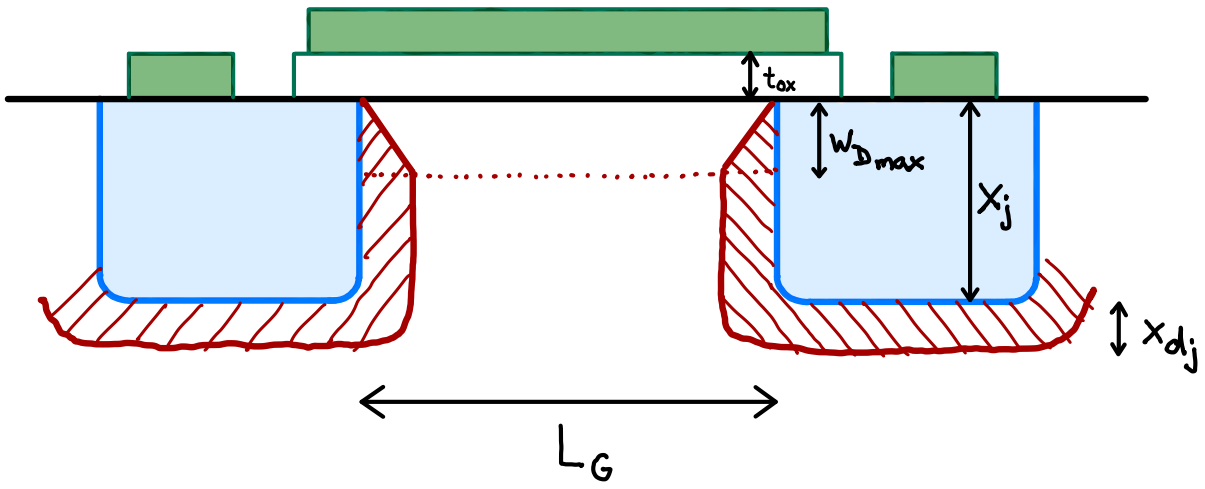
SHORT CHANNEL EFFECTS IN MOSFETs

1. Source-drain charge sharing
2. Drain-induced barrier lowering (DIBL)
3. Subsurface punchthrough

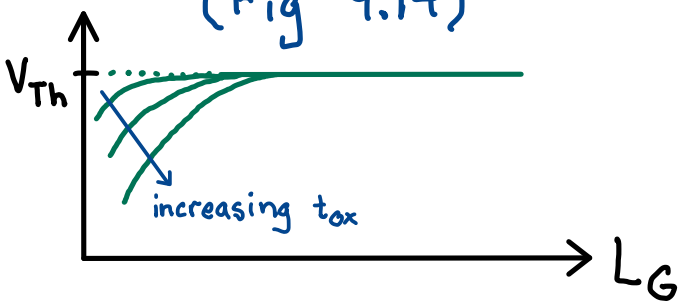
1. Source-drain charge sharing:



- V_{Th} is reduced when L_G is reduced. Less gate voltage is required to deplete Si to a depth W_{Dmax} due to depletion from n+ source and drain regions

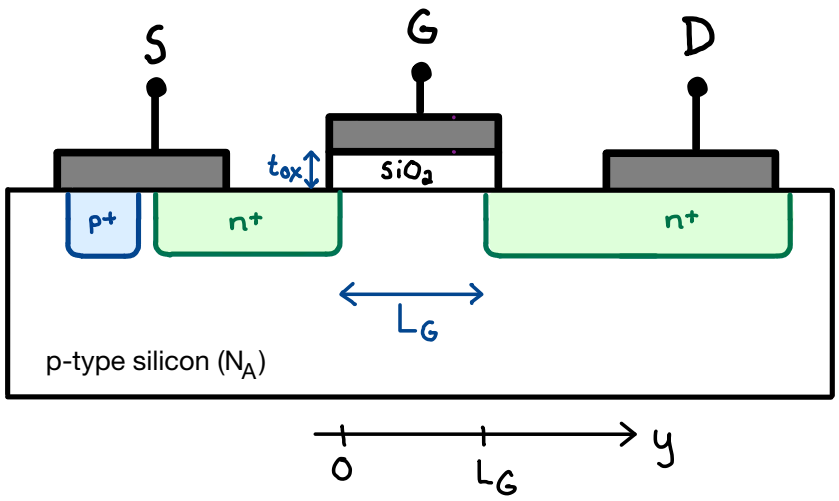
- Effects are more severe for thicker oxides

(Fig 9.14)



- To minimize S/D charge sharing:
  - → Reduce t_{ox} (constant field scaling)
  - → Reduce x_j (shallow implant)
  - → Reduce x_{dj} (increase substrate doping)

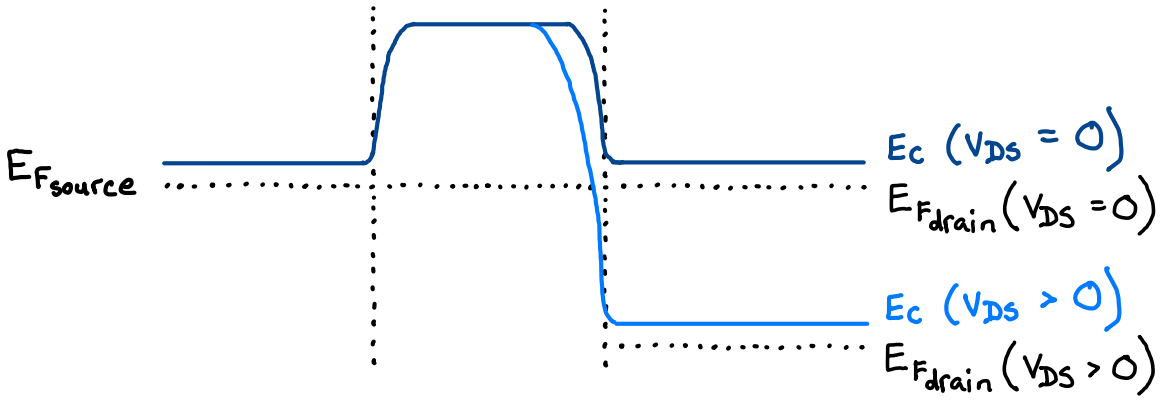
2. DIBL



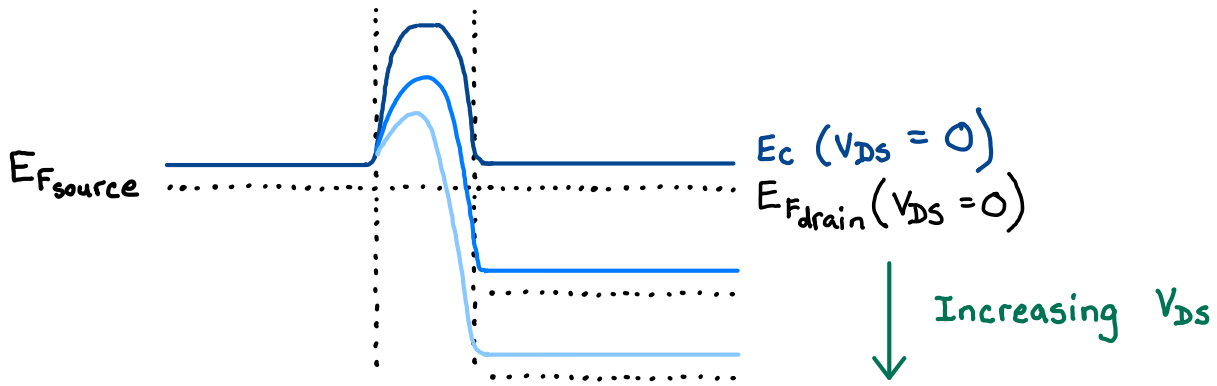
$V_{GS} \leq V_{Th}$

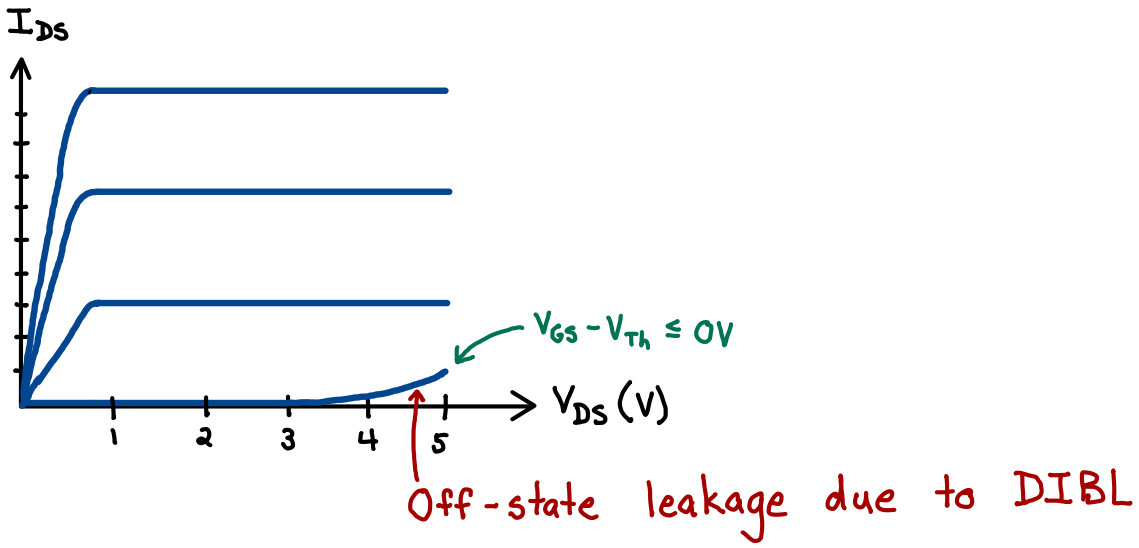
$V_{DS} > 0$

Long L_G:



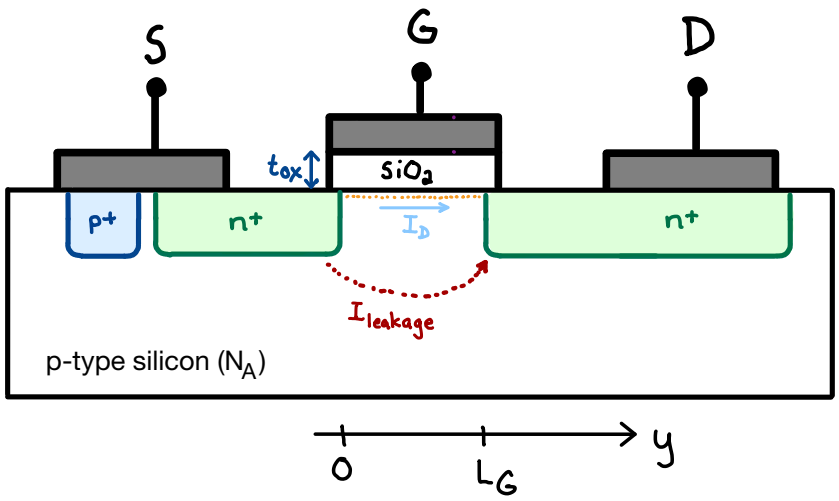
Short L_G:





- DIBL causes an increase in subthreshold leakage
- Mitigate by increasing C_{ox}, thereby increasing coupling between gate and channel (constant field scaling)

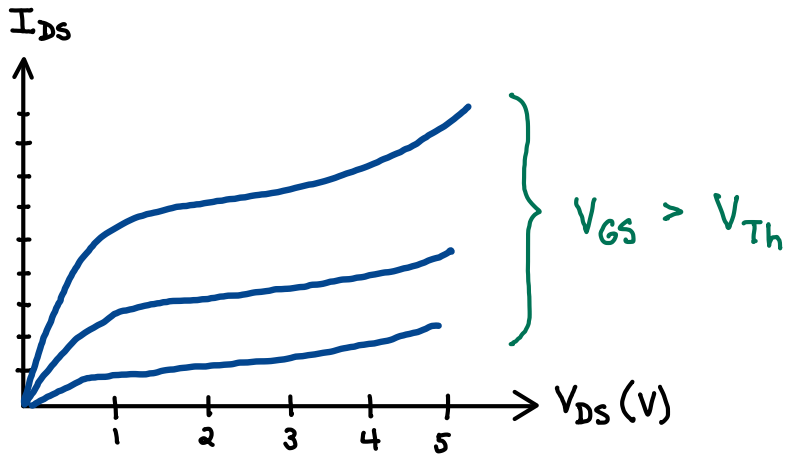
3. Subsurface Punchthrough



$V_{GS} \geq V_{Th}$

$V_{DS} > 0$

- Similar to DIBL, only leakage occurs through substrate while the device is ON



- Mitigated by eliminating leakage path
  - SOI
  - FinFET

} next lecture

Summary:

1. Source-drain charge sharing

   - Causes shift in threshold voltage as L_G is reduced

   - Mitigated by reducing oxide thickness, reducing n-well junction depth, and increasing substrate doping

2. Drain-induced barrier lowering (DIBL)

   - Causes an increase in off-state leakage

   - Mitigated by increasing the oxide capacitance (e.g., by reducing the oxide thickness)

3. Subsurface punchthrough

   - Causes an increase in on-state leakage (increased output conductance)

   - Mitigated by modern device design (SOI or FinFET) that eliminates leakage path