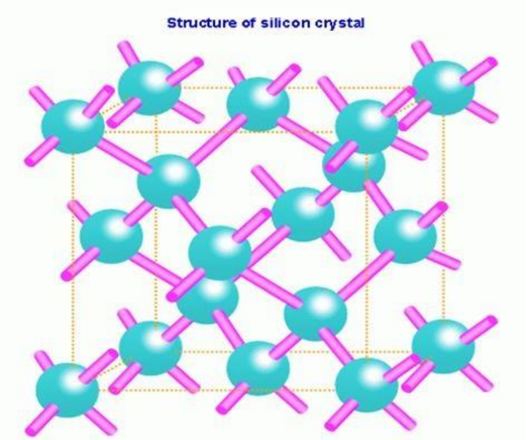

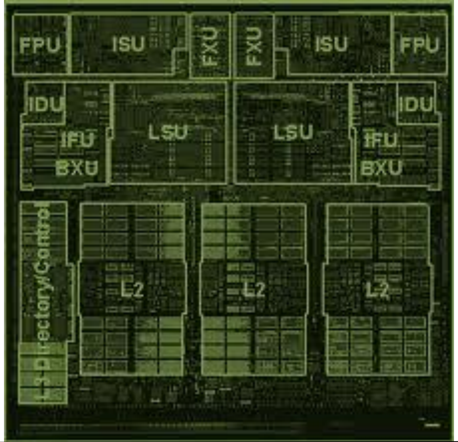

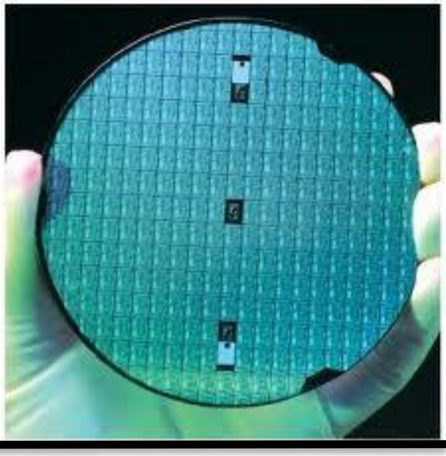

ECE 122A

VLSI Principles

Lecture 1

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Electrical and Computer Engineering
University of California, Santa Barbara
E-mail: kaustav@ece.ucsb.edu

Why VLSI?

- Difficult to imagine life without integrated circuits….
- Applications in:
  - Consumer Electronics
  - Computing
  - Communication
  - Medical/Health
  - Entertainment
  - Energy
  - Aerospace
  - Automobile
  - Military

Electronics inside a BMW…

http://www.bmw.com/com/en/insights/technology/technology_guide/articles/digital_motor_electronics.html

Digital Motor Electronics (DME).

The comprehensive management system for your engine: Digital Motor Electronics (DME) controls all key aspects of the engine's operation, ensuring optimum reliability, maximum performance and the lowest possible fuel consumption and emissions.

By managing key engine functions, Digital Motor Electronics (DME) guarantees optimum reliability, maximum performance and the lowest possible fuel consumption and emissions. Its sensors continually all factors affecting the operation of the engine. The data is then evaluated by a microprocessor and translated into commands for the fuel injection and ignition systems.

The DME system receives up to 1,000 separate items of data input per second, including engine speed, air intake volume, air temperature and density, coolant temperature, throttle position, accelerator position and vehicle speed.

DME verifies all incoming data by comparing it with the reaction of the rest of the system. If a defective sensor delivers unrealistic data, DME replaces this with preset standard values. If a spark plug fails, DME immediately cuts fuel flow to this cylinder in order to prevent engine damage.

DME looks after the electrical power system too, with sensors measuring the charge and condition of the battery as well as current electrical power consumption. By maintaining optimum battery charge levels and thus avoiding flat batteries, it prevents damage to the battery and guarantees maximum battery life, thereby helping to ensure the engine always starts readily.

BMW introduced the world's first Digital Motor Electronics system in the BMW 732i in 1979.

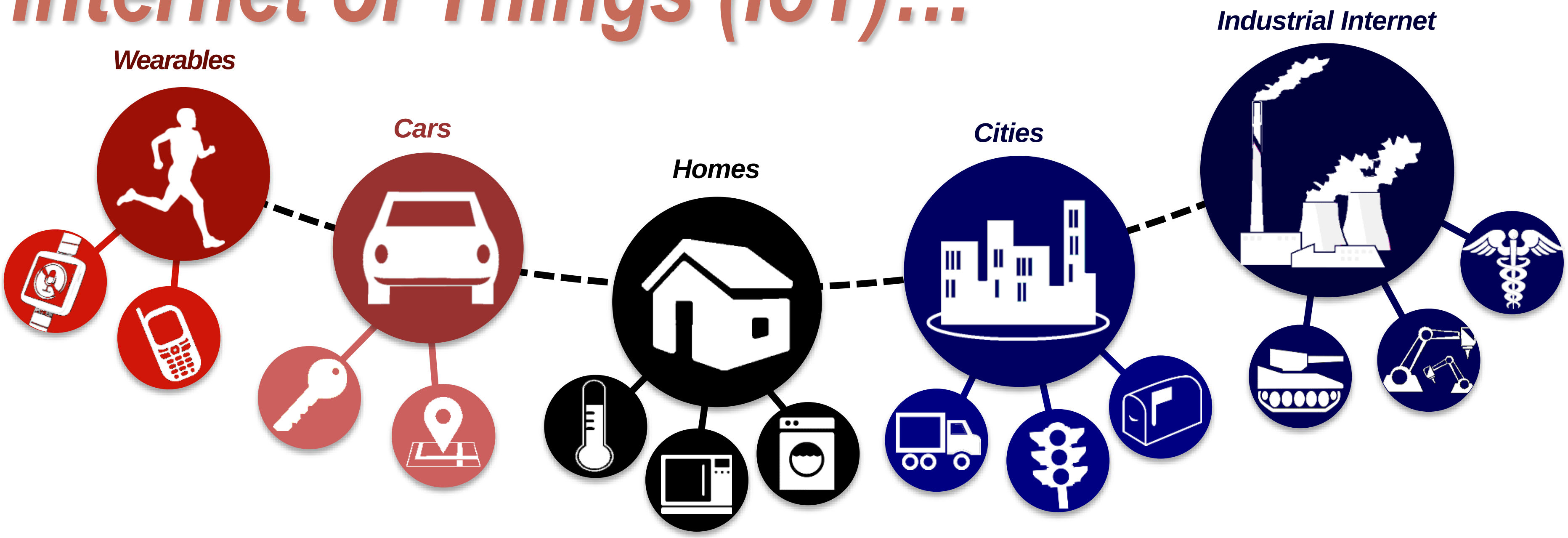
BMW Z4 Roadster

VLSI inside…

Hard drive of a PC

Digital Mobile Phones

Internet of Things (IoT)…



- *1990s' fixed Internet wave connected 1 billion users*
- *2000s' mobile wave connected another 2 billion*
- *The IoT has the potential to connect 28 billion "things" by 2020*

—— The third wave of Internet development

Bottom Line:

To enable IoT - need low power sensors and ICs….

What is VLSI?

- *Very Large Scale Integrated ~~Circuits~~ Systems*
- ***Very-large-scale integration*** *(**VLSI**) is the process of creating integrated systems by combining billions of transistors into a single chip.*

1971: *Intel 4004*

2300 Transistors…with CPU, memory and input/output controls

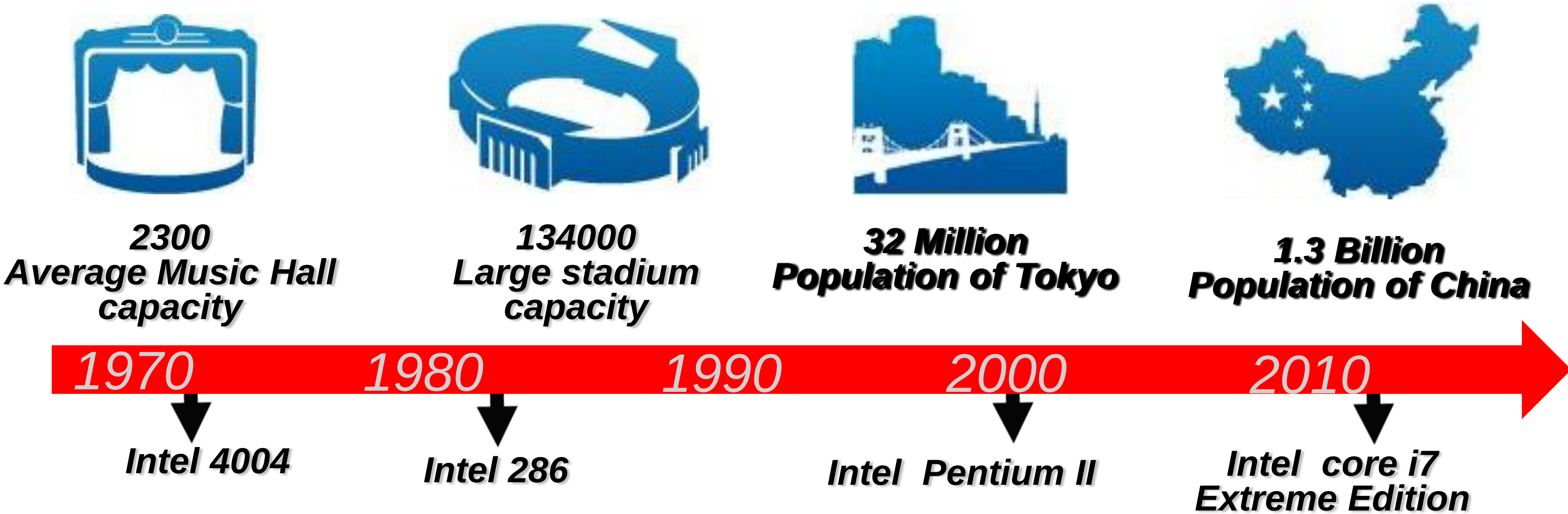
2008: *Intel® Xeon® Processor MP X7460*--***1.9 Billion Transistors!!!***

For details on Intel Microprocessors:

http://www.intel.com/pressroom/kits/quickreffam.htm

Amazing Transistor Scaling….

- *If transistors were people ….*



Now imagine 1.3 Billion people in the original music hall!!!!

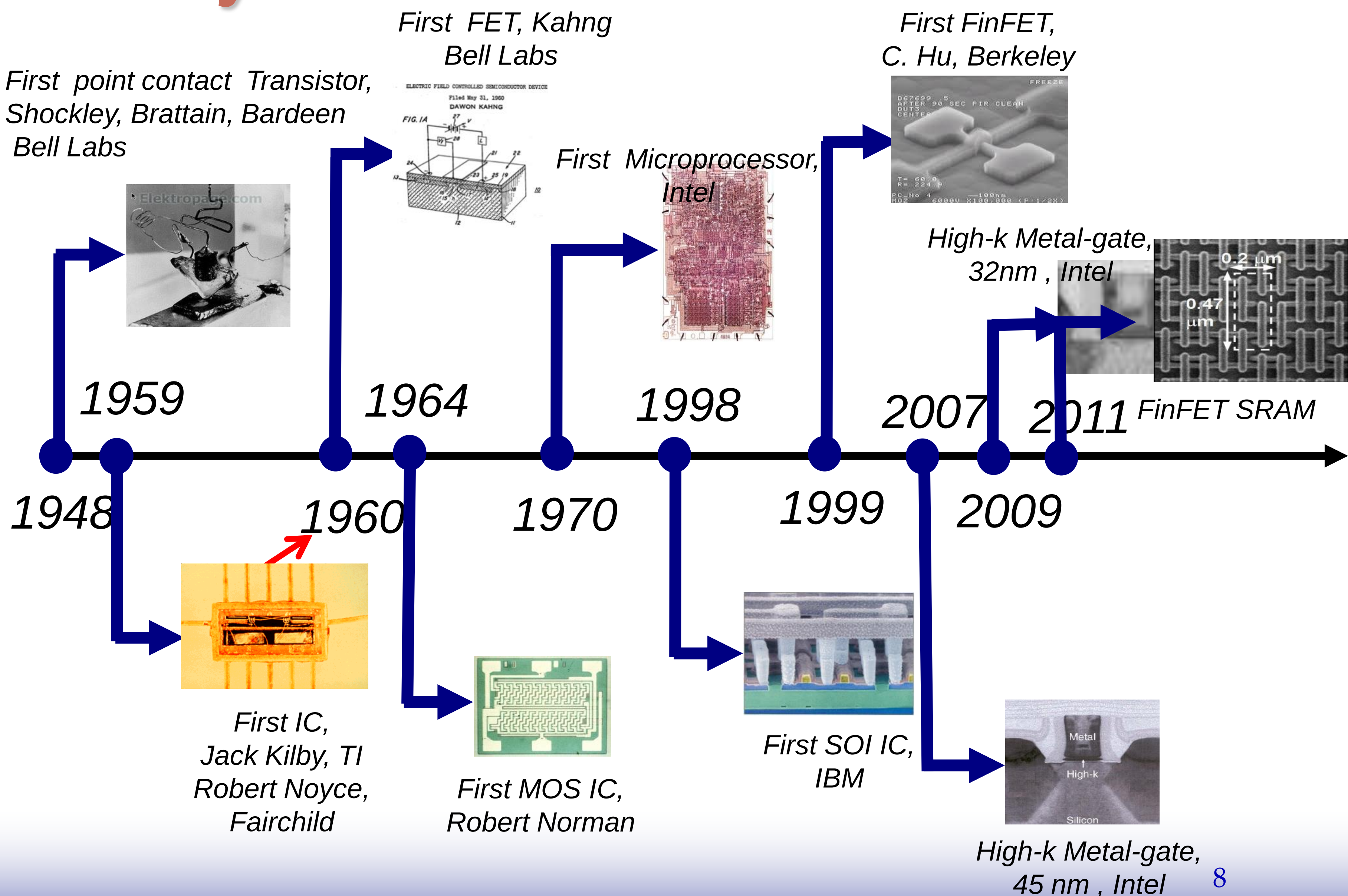
Why Scaling?

- *Higher number of devices in chip*
- *Faster operation*
- *More functionality and lower cost*

Scaling Challenges

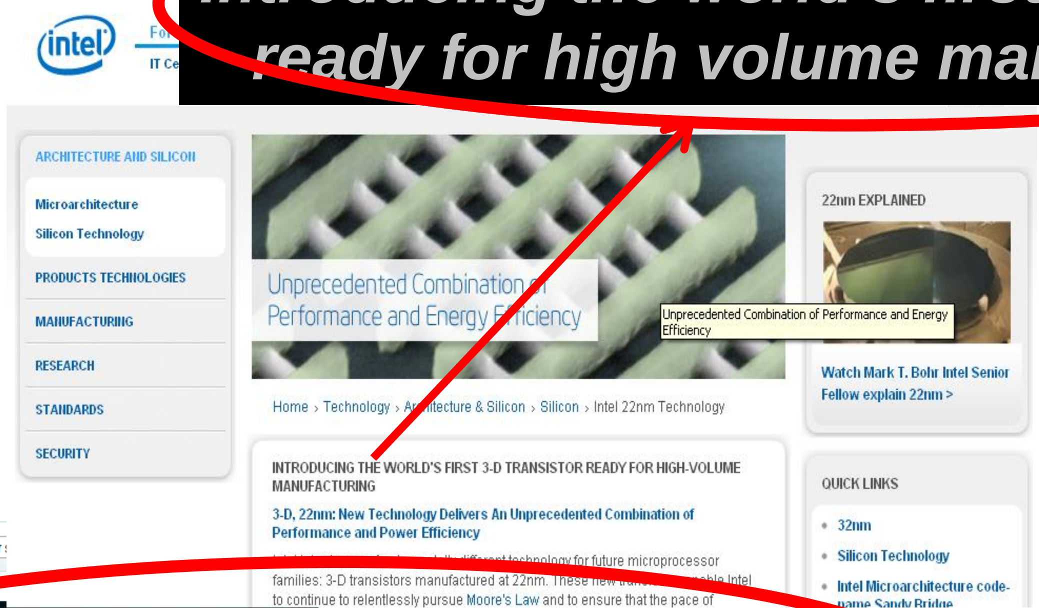
- *Higher power consumption*
- *Severe short-channel effects*
- *Higher leakage*

History…

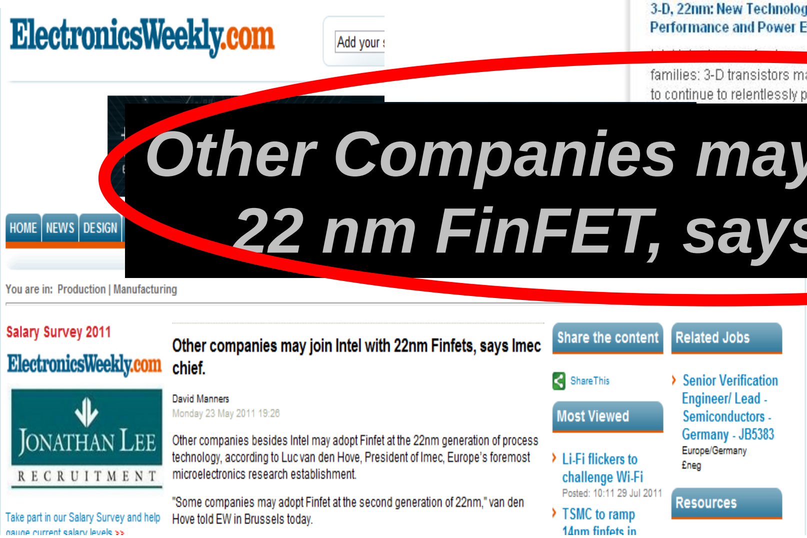

First point contact Transistor, Shockley, Brattain, Bardeen Bell Labs
First FET, Kahng Bell Labs
First Microprocessor, Intel
First FinFET, C. Hu, Berkeley
High-k Metal-gate, 32nm , Intel
0.2 µm
0.47 µm
FinFET SRAM
1948
1959
1960
1964
1970
1998
1999
2007
2009
2011
First IC, Jack Kilby, TI Robert Noyce, Fairchild
First MOS IC, Robert Norman
First SOI IC, IBM
Metal
High-k
Silicon
High-k Metal-gate, 45 nm , Intel

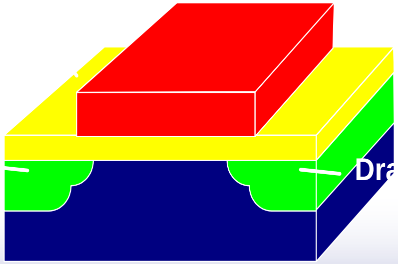
2011: a paradigm shift

Introducing the world's first 3-D transistors ready for high volume manufacturing

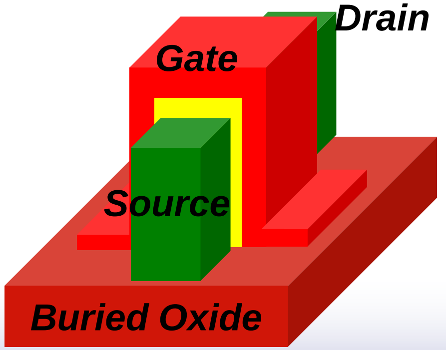


Other Companies may join Intel with 22 nm FinFET, says IMEC chief.



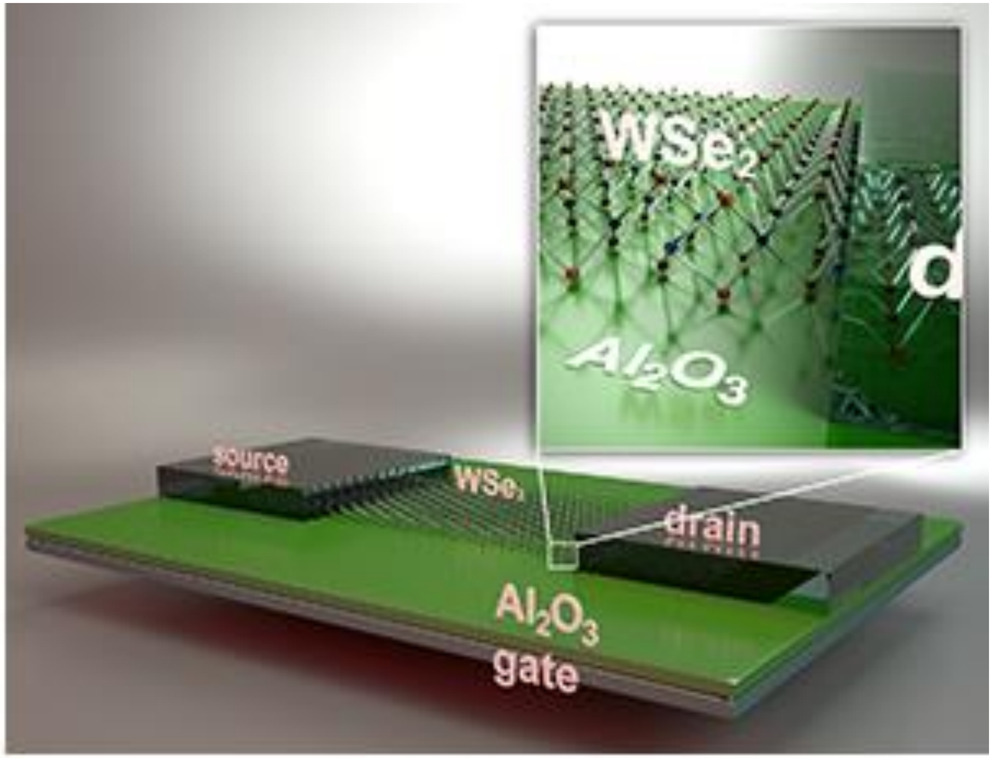


Planar MOSFET



FinFET

Ultimate Thin-body Transistors



Schematic view of a back-gated field effect transistor fabricated by UCSB researchers using monolayer tungsten diselenide (WSe2) channel material. *Credit: Peter Allen, UCSB*

Read more: http://engineering.ucsb.edu/news/711

Who should be taking this course?

- Those interested in pursuing career in nanoelectronics, bioelectrononics etc: transistor design, circuit design, or computer-aided design
- Those interested in exploring "emerging devices and technology" driven circuit/system design
- Those interested in passing the ECE PhD Screening Exam in the VLSI & CMOS Design Area
- Those interested in finding a lucrative position in the semiconductor industry as an IC design engineer
  - *In the past, students recruited by Intel, AMD, IBM, TI, SanDisk, nVidia, Marvel, Global Foundaries, Maxim, Micron Technology and other IC companies have found the course invaluable…*

About this course…….

Not bipolar,
Not ECL, Not GaAs
Little NMOS

Not SSI or MSI
Emphasis on Large Scale
and integration

CMOS Digital VLSI Design

Not Analog

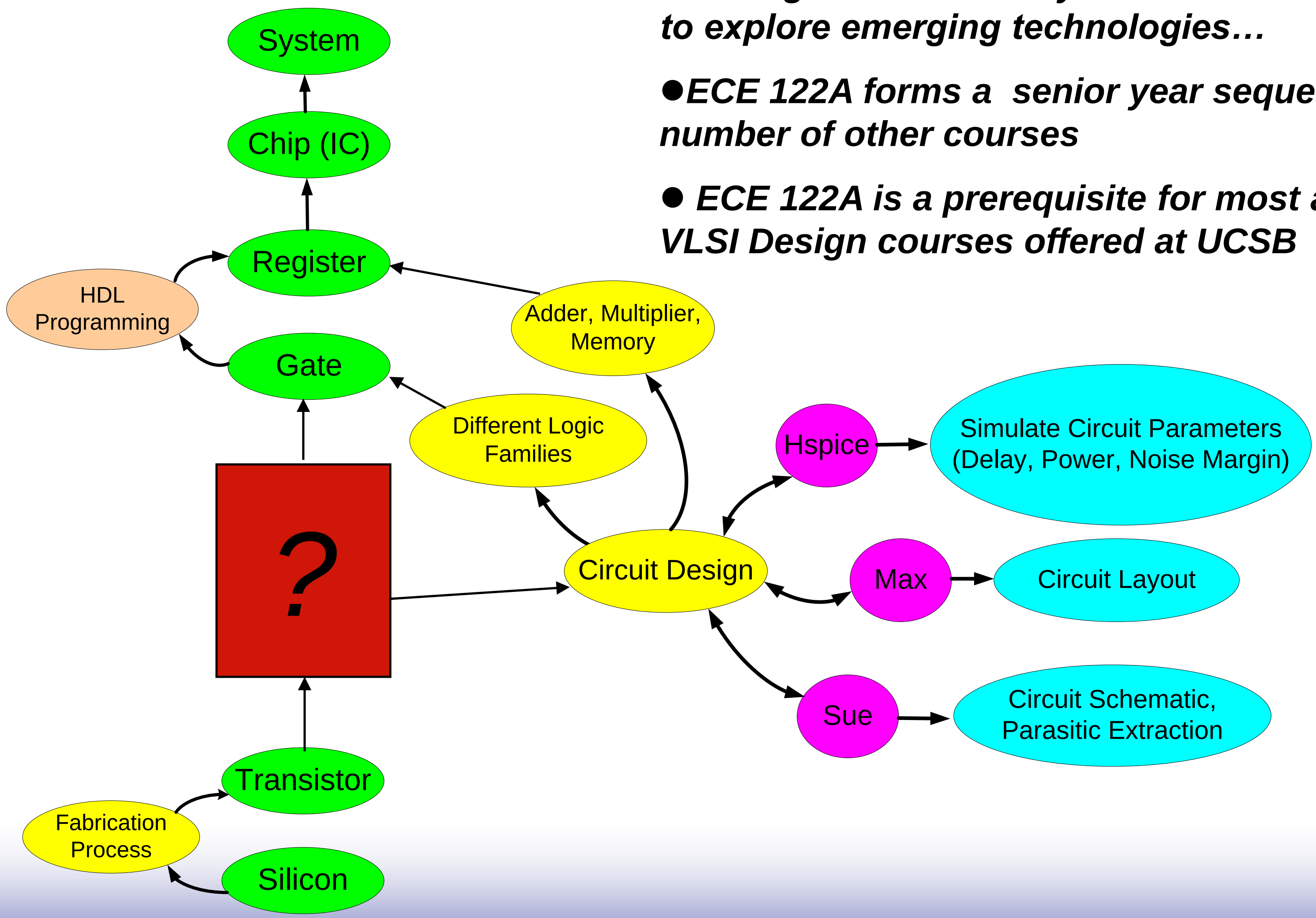
Not testing
Not tool development
Not Architecture

What to expect out of the course…

- **The course is:**
  - To learn transistor level design of logic gates, components
  - to learn practical aspects of design including design trade-offs
- **The course is not:**
  - A tutorial to build expertise in CAD tools, or
  - A forum to demonstrate architecture skills, or
  - A test of your logic design expertise, or
  - An exercise to design a microprocessor.
- **Course time is short: < 20 classes**
  - A lot of self-study is expected
  - Homeworks and assignments could be time consuming—but a key component of this course
  - Project is a major commitment and calls for <u>a lot of hard work</u>!
- **This is not a class just to improve your GPA!**

Why take this course?

- ***This is what you will need to do anything meaningful in circuits/systems research as well as to explore emerging technologies…***
- ***ECE 122A forms a senior year sequence with a number of other courses***
- ***ECE 122A is a prerequisite for most advanced VLSI Design courses offered at UCSB***



What are we going to cover?

- **Introduction to digital integrated circuits.**
  - CMOS devices and manufacturing technology. CMOS inverters, gates and interconnects. Circuit characterization: delay, noise margins, and power dissipation. Combinational and sequential circuits. Arithmetic operations and memories

- **What will you learn?**
  - Understanding, designing, and optimizing digital circuits with respect to different quality metrics: area, speed, power dissipation, and reliability using analytical methods and circuit simulation
  - Practical aspects of IC design: impact of manufacturing variations (device level variations) on circuit level metrics, effect of device and interconnect parasitics on circuit performance
  - Learn to use various IC design tools: Layout, Extraction, Circuit simulation

Textbook and References

- Textbook
  - *CMOS VLSI Design: A Circuits and Systems Perspective* (Fourth Edition, 2011)
    - by Neil H. E. Weste and David Harris
    - Addison Wesley Publishing Company
- Supplementary Text:
  - *Modern Semiconductor Devices for ICs*

    (First Edition, 2010)
    - by Chenming Hu
    - Prentice Hall Publishing Company

- Lecture Notes: Combination of slides + discussion
  - Only slides will be posted on the class web page

- Reference Materials and Recommended Reading
  - Will be posted on the class web site:

    Class Home Page:

    http://www.ece.ucsb.edu/courses/ECE122/122_F15Banerjee/

Prerequisites

- Logic Design (ECE 152A or equivalent) …at least ECE 15A
  - Combinational and clocked logic, gates, latches, flip-flops, etc.
  - Logic reduction: K-maps
  - Fundamentals of EE
  - Resistance, capacitance, inductance, power/energy
- Circuit Analysis (both analytical and simulation based)
  - at the level of ECE 2A, 2B and 2C
- Semiconductor and Device Physics (basics will be covered in this course)
  - Energy band diagrams, p/n junctions, MOS transistors

….Most important prerequisite is your desire to excel!!

Homework, Exams, Grading (1)

- Homeworks: will be posted on the class home page
  - Weekly HW/Lab assignments
  - Late homework will be penalized (20% per day), submission (beyond the second day) will get ZERO grade
  - Solutions will be Posted on the class web site a week after the due date
  - Homework assignments require Lab work
  - All Labs MUST be completed for passing
  - **Will count towards 20% of the final grades**
- Exams
  - Midterm Exam: **Will count towards 20% of the final grades**
  - FINAL Exam: **Will count towards 40% of the final grades**
- Final Project: must complete to pass
  - Will be posted on class home page
  - **Will count towards 20% of the final grades**

- **No "make-up" homework, exams, labs**

Homework, Exams, Grading (2)

- Project
  - You may work as part of a team (not more than 2), yet graded individually
    - – Your grade = Oral questioning by TAs + project report
  - The project report MUST summarize the contribution of both students
- Final grades
  - Distribution of grades depends on class performance
  - Standard grading techniques will be applied (histograms, curves)--- same criteria for all students
    - *No incomplete grade (no exceptions)*

Class Calendar

Lectures	Homework	Covered Topics	Lab & Project
9/ 29 Lecture 1 **10/ 1 Lecture 2** **10/ 6 Video I & II**	Homework 1 (10/01) Digital Design Review Due 10/09	Boolean Algebra Combinational Circuit Sequential Circuit Moore's Law	Lab 1 Environment Setup and Practice 10/06 Due 10/16
10/ 8 Lecture 3 **10/13 Lecture 4** **10/15 Lecture 5**	Homework 2 (10/08) CMOS and Pass Transistors Due 10/16	CMOS Implement Pass Transistor Transmission Gate Multiplexer Finite-State-Machine Euler Path	Lab 2 HSpice, CMOS Sizing 10/13 Due 10/23
10/20 Lecture 6 **10/22 Lecture 7**	Homework 3 (10/15) Semiconductor Physics Due 10/23	Carrier Statistics Current in Semiconductor PN Junction MOS Capacitor	Lab 3 Static CMOS 10/20 Due 10/30
10/27 Lecture 8 **10/ 29 Lecture 9**	Homework 4 (10/22) MOSFET and CMOS Inverter Due 10/30	Threshold Voltage Body Bias Current Saturation Device Parasitics CMOS Inverter	Lab 4 Inverter 10/27 Due 11/06
11/ 3 Lecture 10 **11/ 5 Midterm** **11/10 Lecture 11** **11/12 Lecture 12**	Homework 5 (10/29) Inverter, CMOS Sizing, Interconnect Due 11/13	Logical Effort Interconnect	Final Project Starts from 11/01
11/17 Lecture 13 **11/19 Lecture 14** **11/24 Lecture 15** **11/26 Holiday**	Homework 6 (11/12) Logic Design Styles Due 11/23	Ratioed Logic Pass Transistor Logic Dynamic Logic	
12/ 1 Lecture 16 **12/ 3 Review**	Homework 7 (11/23) Sequential Logic and Memory Due 12/ 4	Sequential Logic DRAM SRAM	
Final Exam: 12/10 (Thursday) 4:00 – 7:00 PM			
Project Report Due: 12/12 (Saturday)			

Preparation for the course

- Computing environment and tools
  - Setup computer account, and the compute environment
  - Familiarize with the schematic and layout editors (SUE, MAX)
  - Familiarize with extractor (CALIBER-Mentor Graphics)
  - Familiarize with the circuit simulator (HSPICE)
  - Tutorials on these tools are posted on the class web page
- Theory
  - Review logic design (ECE 152A)
  - Review device physics (I will provide some tutorial material to help you)
- Project
  - You may start formalizing your project team

A few hints

- Homeworks
  - Most important part of the course….
  - Spend most of the time thinking, planning, and exploring on your own
  - Discussions are encouraged but refrain from extracting the answers from the TAs or other students
  - Show your work on the homework! Thought process is more important than final answer → partial credit given
  - Use simulators for verification of your design
- Difficult to take notes?
  - Note down important points, not essays…all slides will be posted
  - Read topics from the textbook BEFORE and AFTER the class
- Actively participate in the class discussion
  - Don't be afraid if you are wrong
- Question everything, even the book