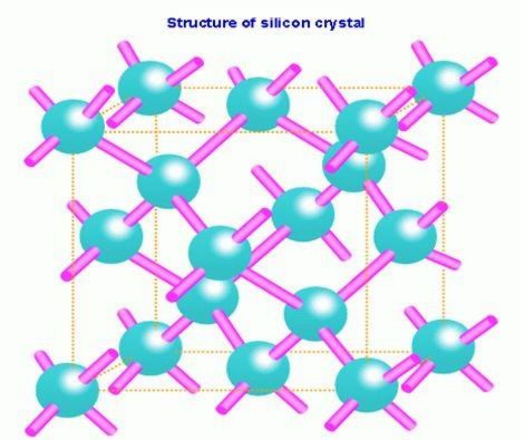
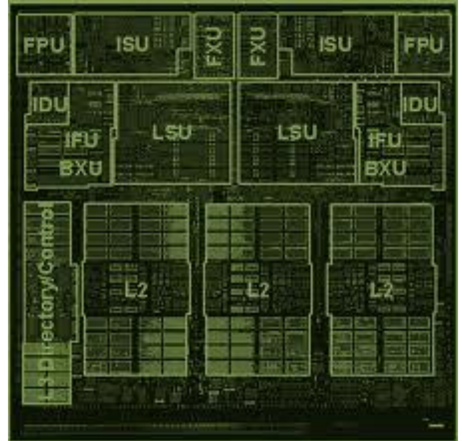
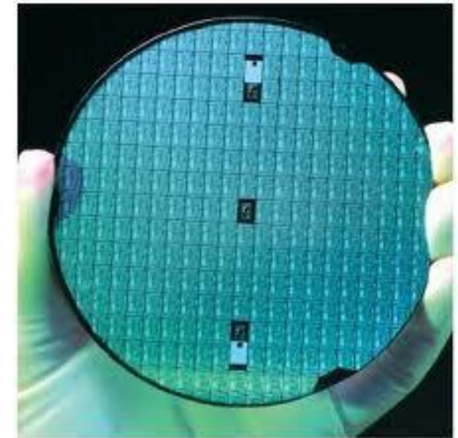






ECE 122A

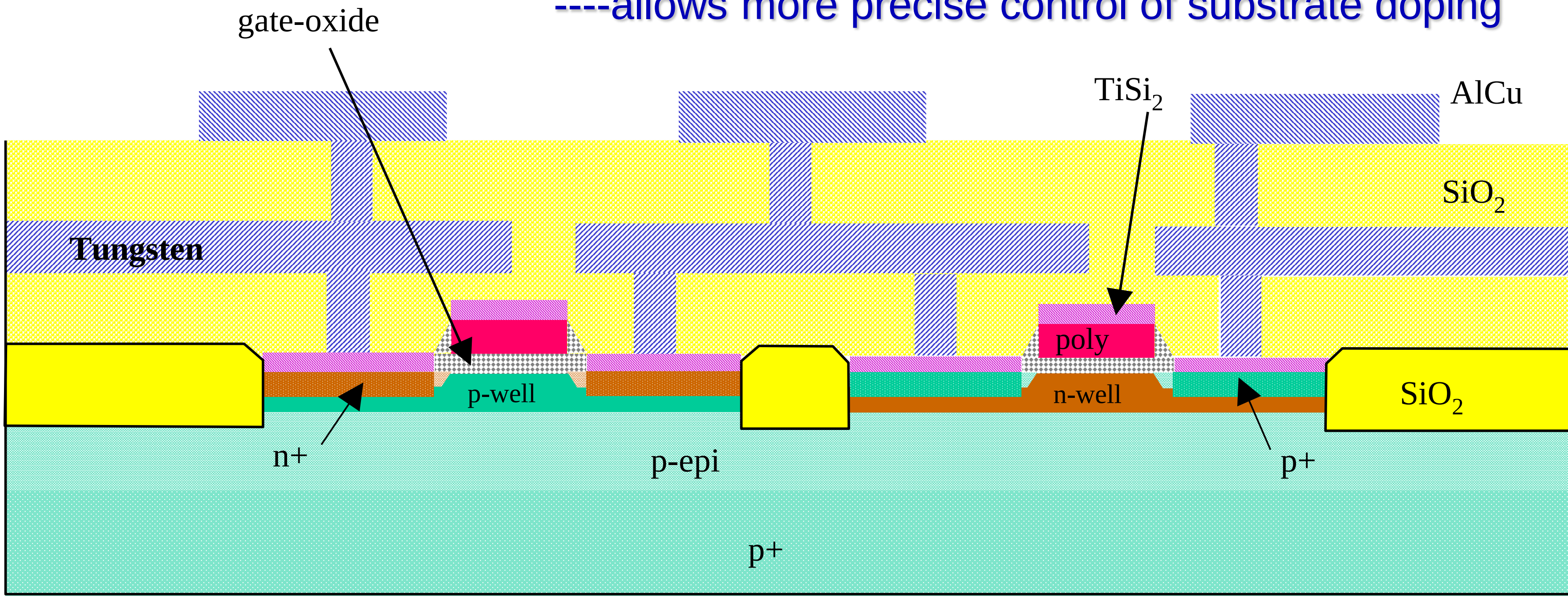
VLSI Principles

Lecture 4

Prof. Kaustav Banerjee
Electrical and Computer Engineering
University of California, Santa Barbara
E-mail: kaustav@ece.ucsb.edu

A Modern CMOS Process

Dual-Well Trench-Isolated CMOS Process
----allows more precise control of substrate doping



- *p+ substrate is typical for pure digital circuits….*
- *For state-of-the-art bulk CMOS processes (say 32 nm)…substrate need not be heavily doped since "Latchup" is not as severe at low Vdd (~1V)*
- *For RF or high-frequency circuits, substrate is usually lightly doped …..to prevent large eddy current losses in inductors*

Basic Steps-I

- **Si Wafer:**
  - Single-crystalline, lightly-doped wafer (6-12 inch diameter)
  - Thickness of at most 1mm
  - Obtained by cutting a single crystal ingot into thin slices
  - An epitaxial layer is grown over the surface of the wafers before device processing
  - A starting p- wafer has a typical resistivity of 25-50 Ohm-cm, which corresponds to a doing level of the order of 10^{15} cm^{-3}
  - Defect density must be very low
  - Well dopings are of the order of 10^{16} to 10^{17} cm^{-3} (this explains the lower doping of the p substrate
  - Crystal orientation: all ICs are manufactured using (100) surface orientation. Why? (fewer imperfections on a (100) surface….gives significantly better Si/SiO_2 interface)

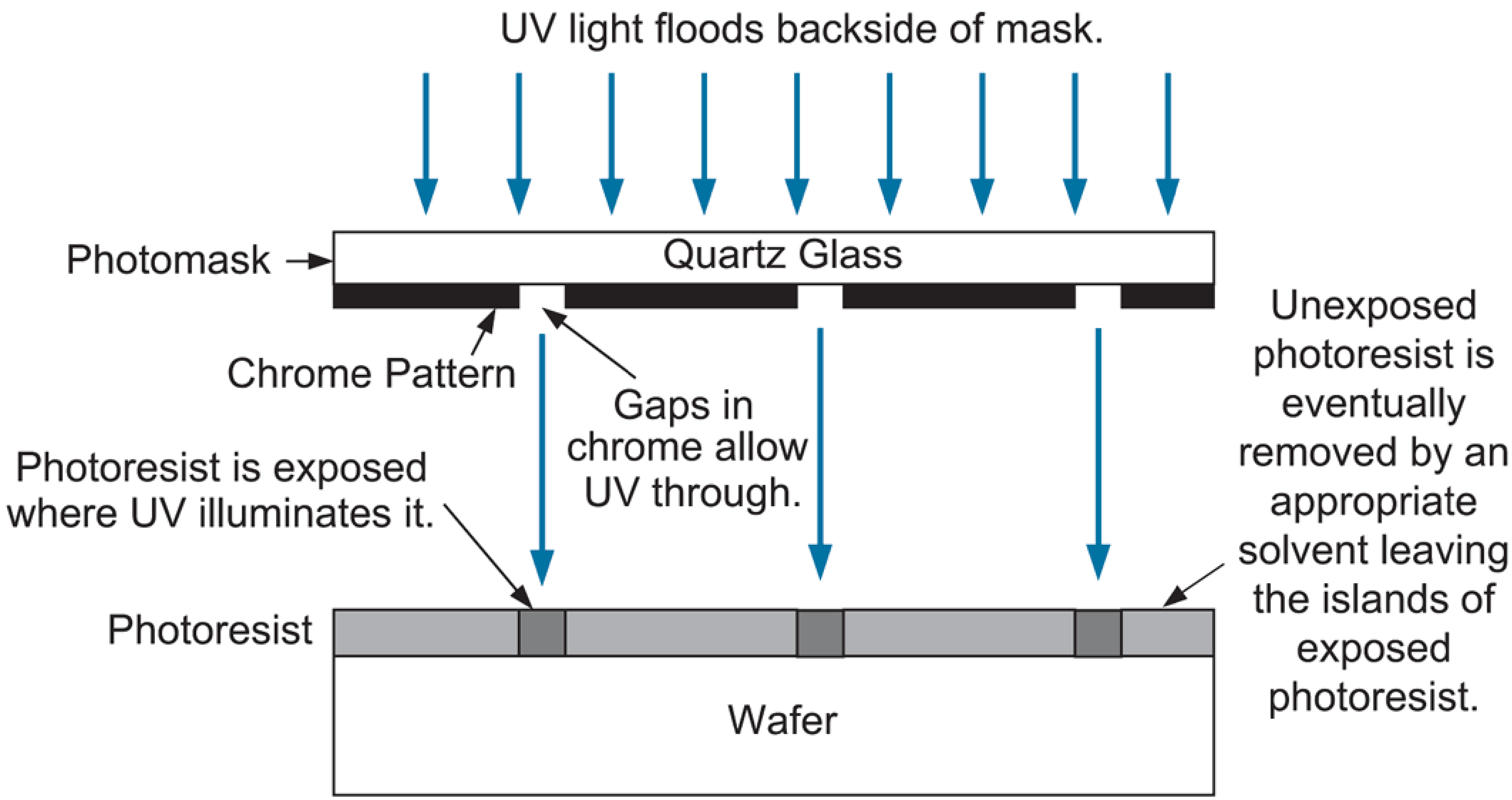
Basic Steps-II

- **Photolithography:**
  - Applied throughout the manufacturing process
  - In each processing step, a certain area of the chip needs to be masked out---using an appropriate optical mask
  - Desired processing step can be selectively applied to the remaining regions
  - Needed for a number of processing steps:
    - oxidation, etching, metal and polysilicon deposition, ion implantation
  - Different operations involved in a typical photolithographic process
    - Oxidation layering, photoresist (PR) coating, stepper exposure, PR development and bake, acid etching, spin-rinse-dry

Negative PR: a light sensitive polymer that is originally soluble in an organic solvent, but has the property that the polymers cross-link when exposed to light, making the affected areas insoluble.

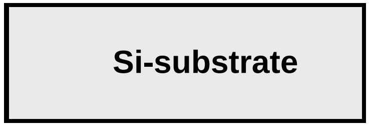
Positive PR: originally insoluble but soluble after exposure

Photolithography:

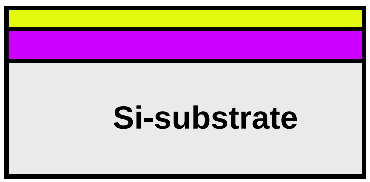


Photomasking with negative photoresist

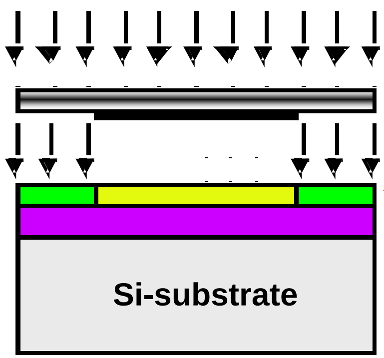
Patterning of SiO2



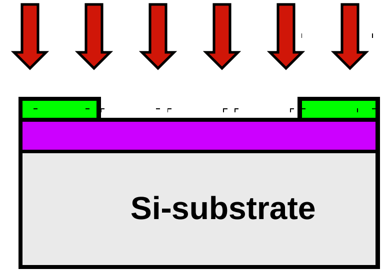
(a) Silicon base material



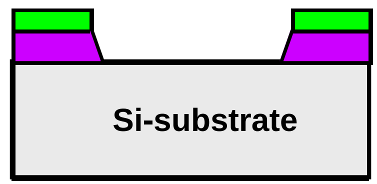
(b) After oxidation and deposition of negative photoresist



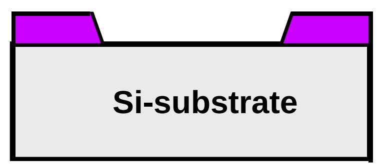
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2



(e) After etching



(f) Final result after removal of resist

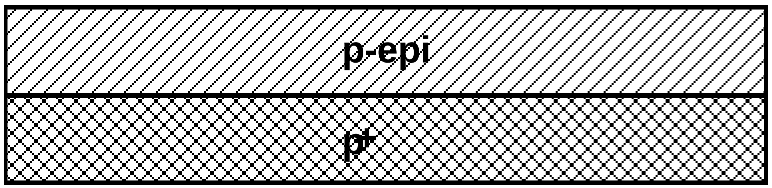
Recurring Process Steps-I

- Diffusion
  - Wafers placed in quartz tube embedded in a heated furnace (900-1100 C)
  - Dopants introduced through a gas
  - Dopants diffuse into the exposed surface
  - Final dopant concentration greatest at the surface and decreases in a gaussian profile deeper into the material
- Ion Implantation:
  - Dopants are introduced as ions in the material
  - Implantation system directs and sweeps a beam of purified ions over the Si surface
  - Wafer needs annealing (wafer is heated to 1000 C for 15-30 minutes) to repair lattice damage and to activate the dopants

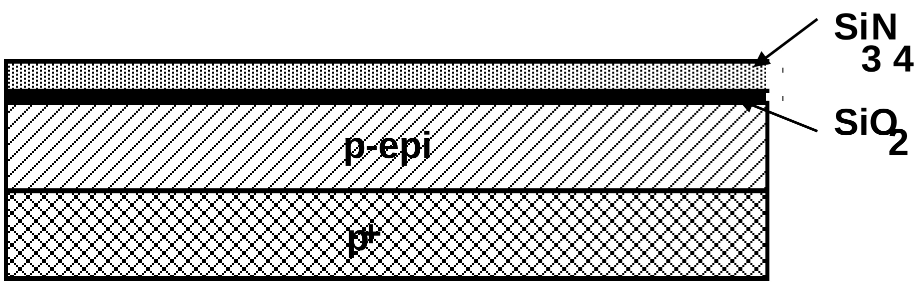
Recurring Process Steps-II

- Deposition
  - Many of the materials (gate oxide, silicon nitride, poly etc) are directly deposited
  - Using a chemical deposition process (CVD etc)
- Etching:
  - Wet etching: uses acid or basic solutions
  - Dry etching: uses plasma (like sandblasting…)
- Planarization
  - Surfaces must be flat
  - Chemical Mechanical Polishing (CMP) before deposition

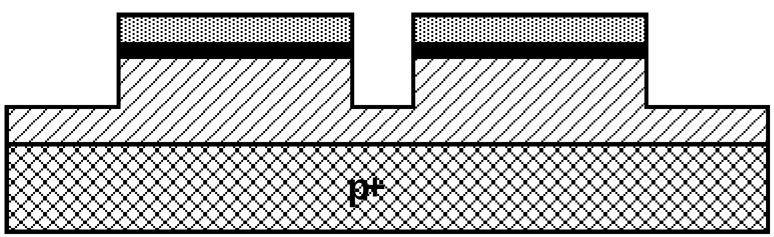
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer

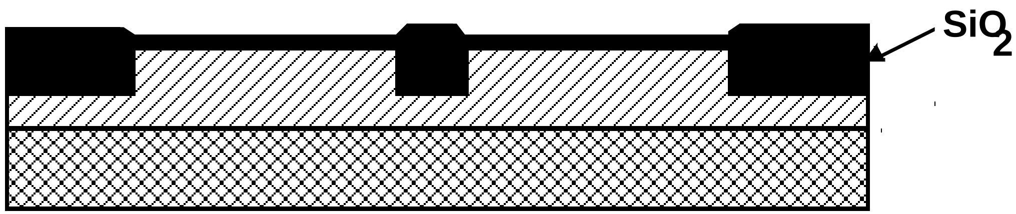


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

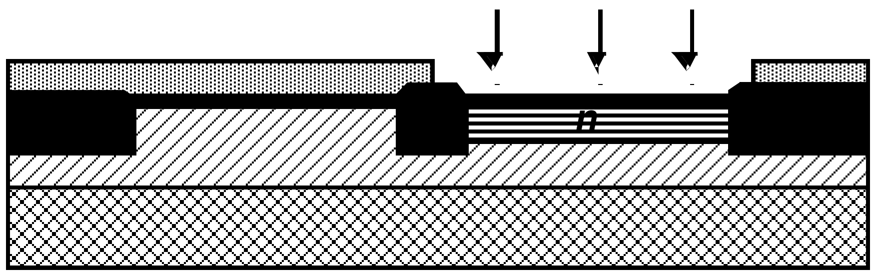


(c) After plasma etch of insulating trenches using the inverse of the active area mask

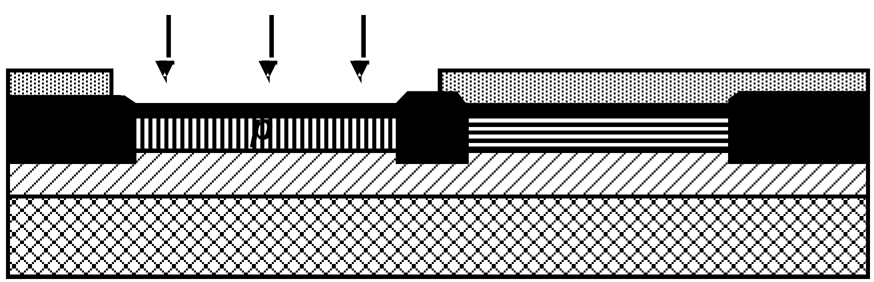
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

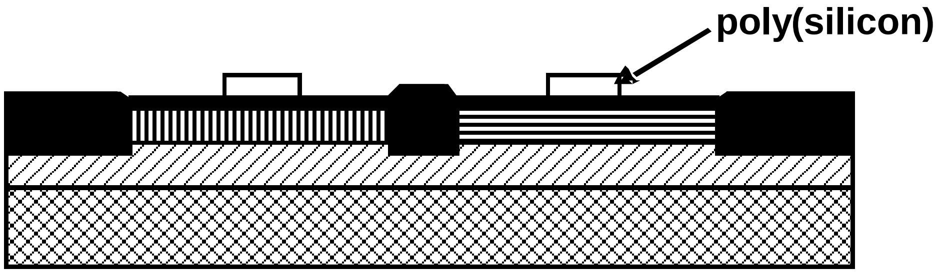


(e) After n-well and V_{Tp} adjust implants

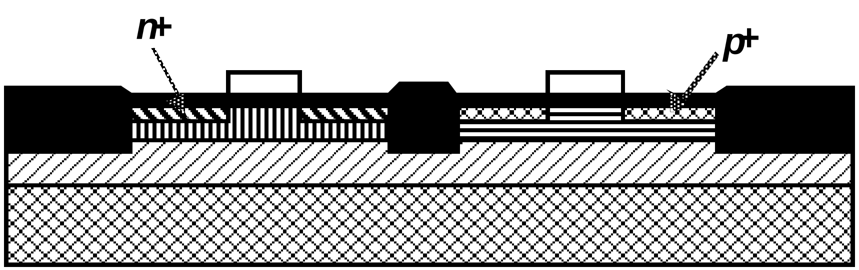


(f) After p-well and V_{Tn} adjust implants

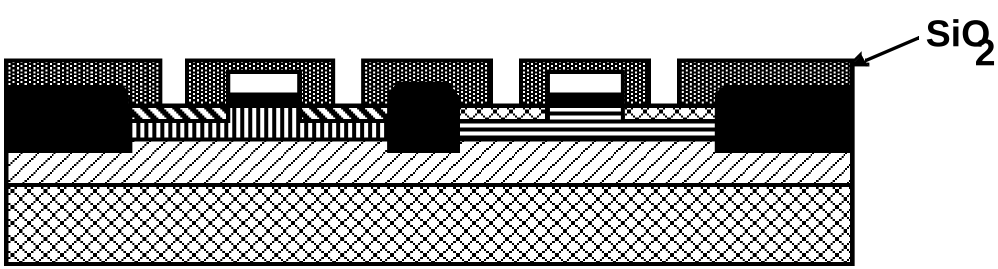
CMOS Process Walk-Through



(g) After polysilicon deposition and etch

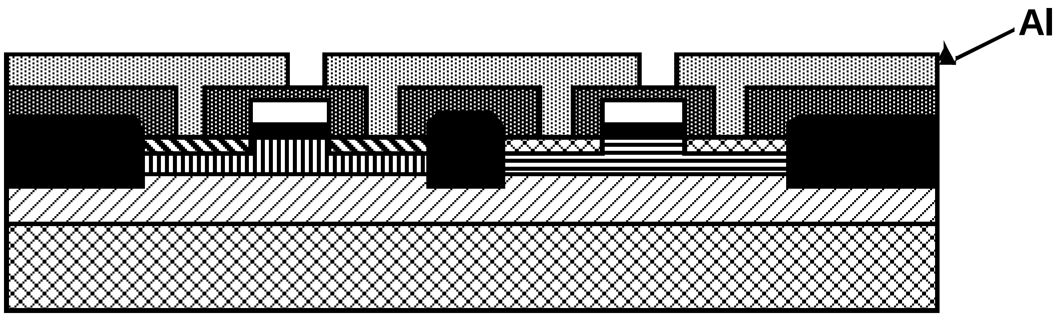


(h) After *n*+ source/drain and *p*+ source/drain implants. These steps also dope the polysilicon.

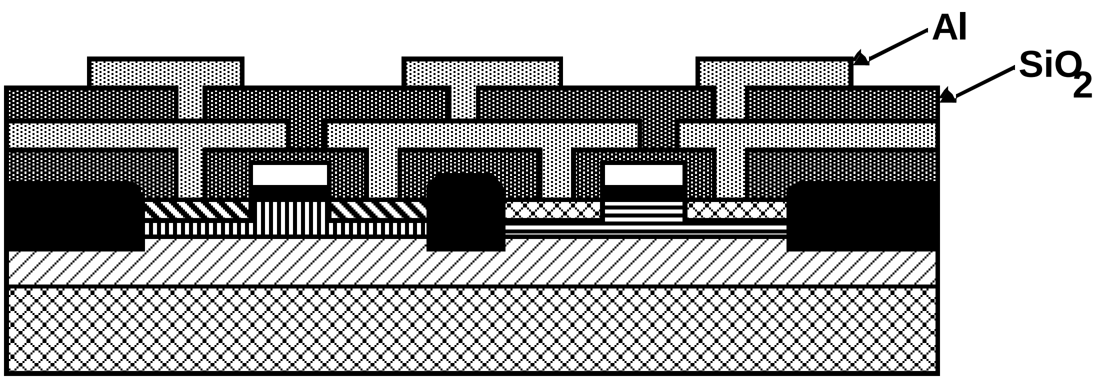


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process Walk-Through

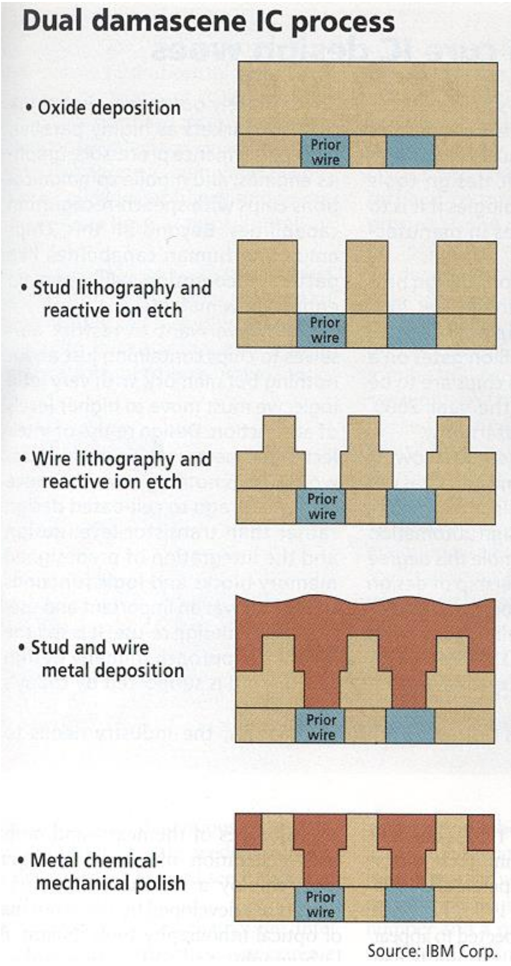


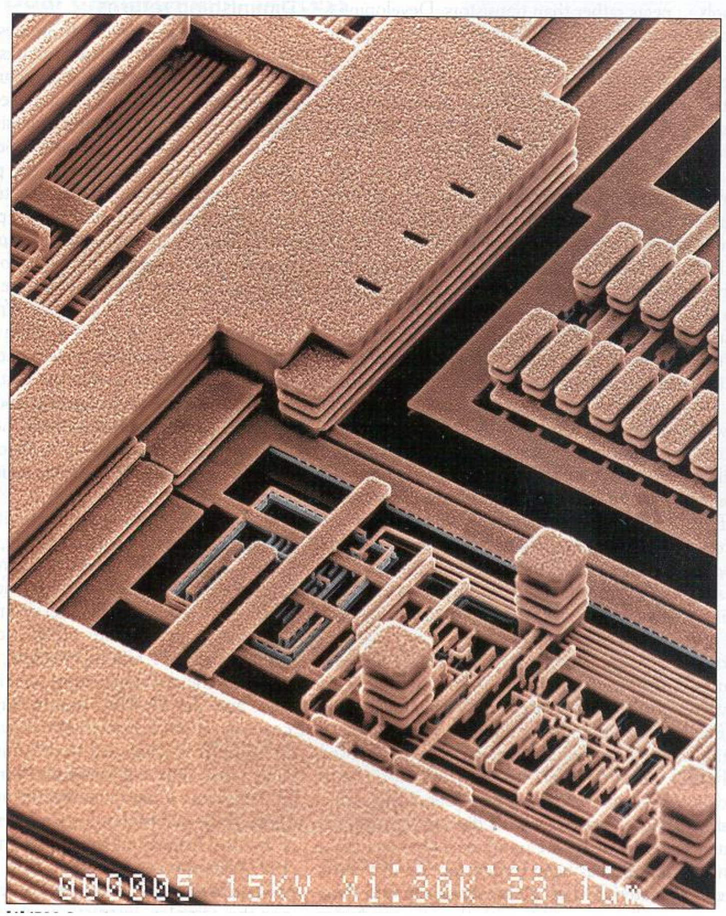
(j) After deposition and patterning of first Al layer.



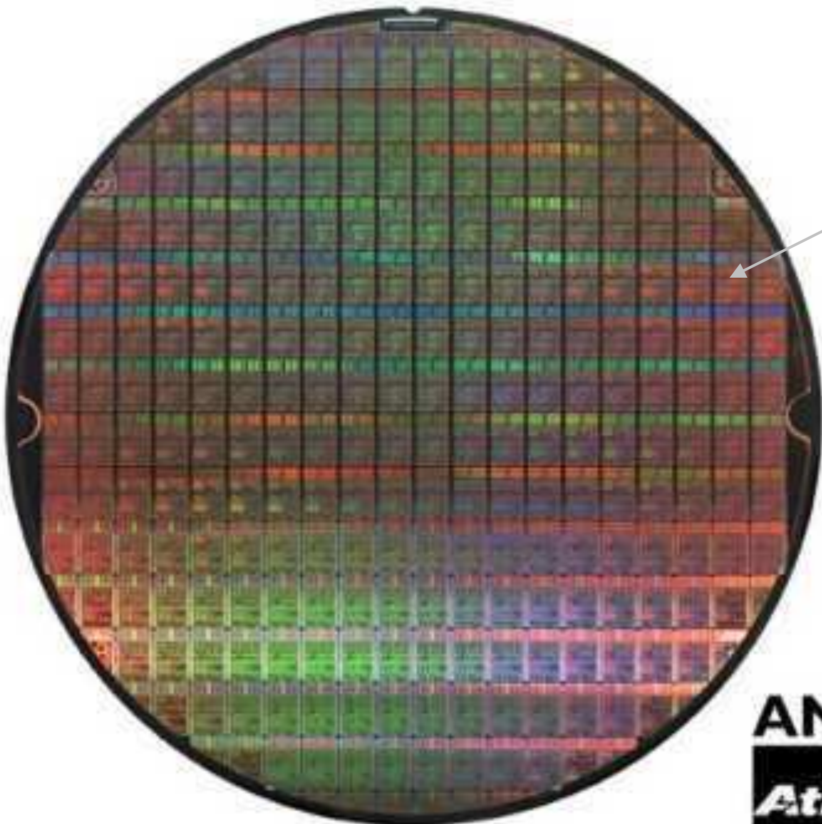
(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

Advanced Metallization: Cu based





Fully Processed Wafer



Single die

Wafer

Going up to 12" (30cm)

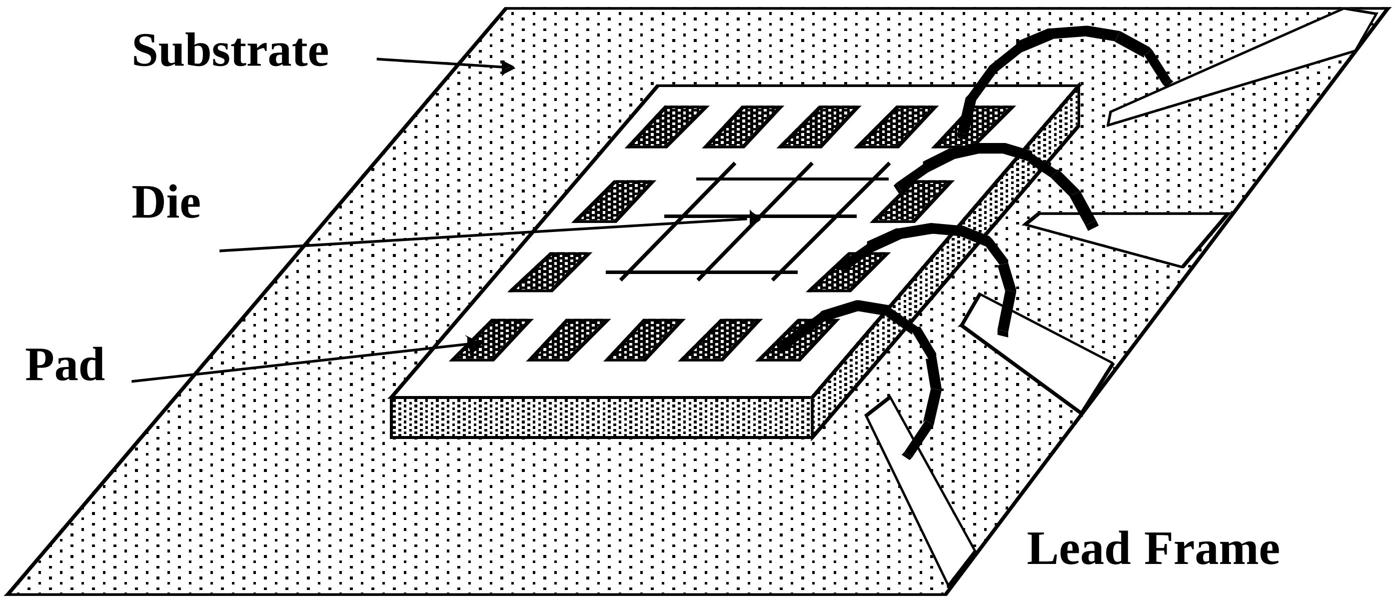
From http://www.amd.com

Packaging Requirements

- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap

Bonding Techniques

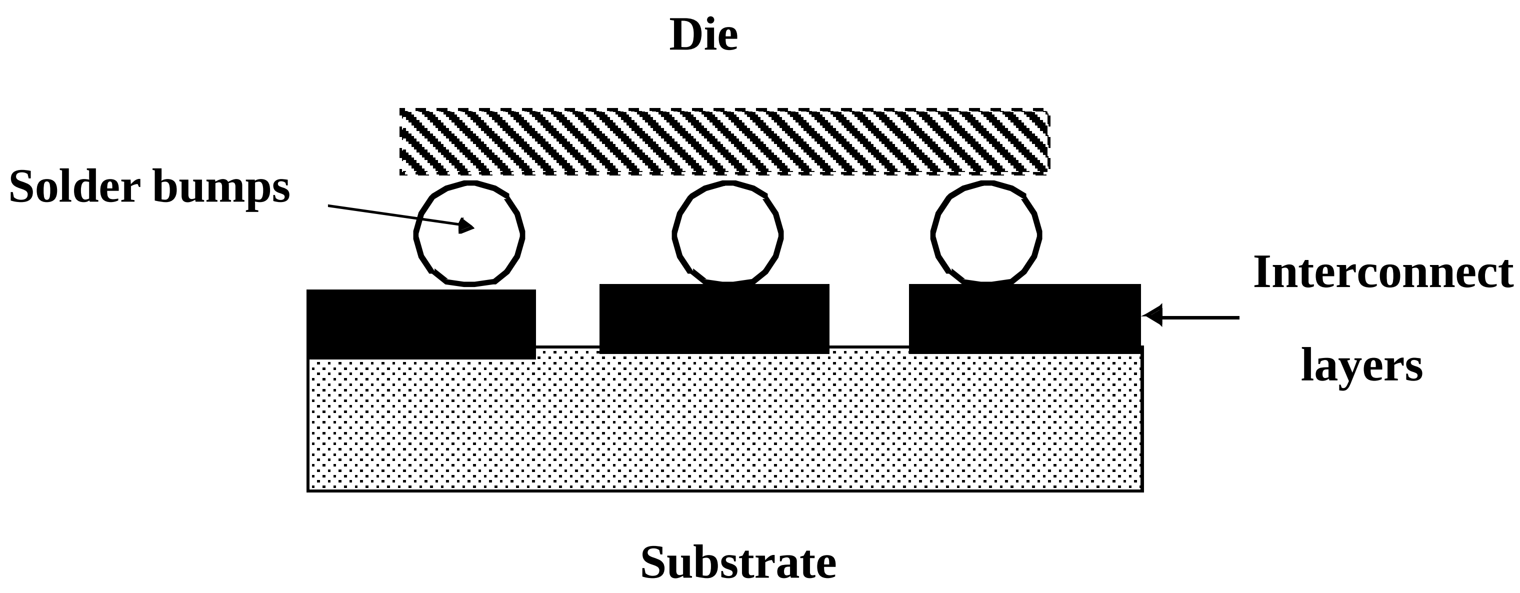
Wire Bonding



Less reliable….

More parasitics….difficult to predict

Flip-Chip Bonding



Less parasitics…..more reliable

Packaged Chip…

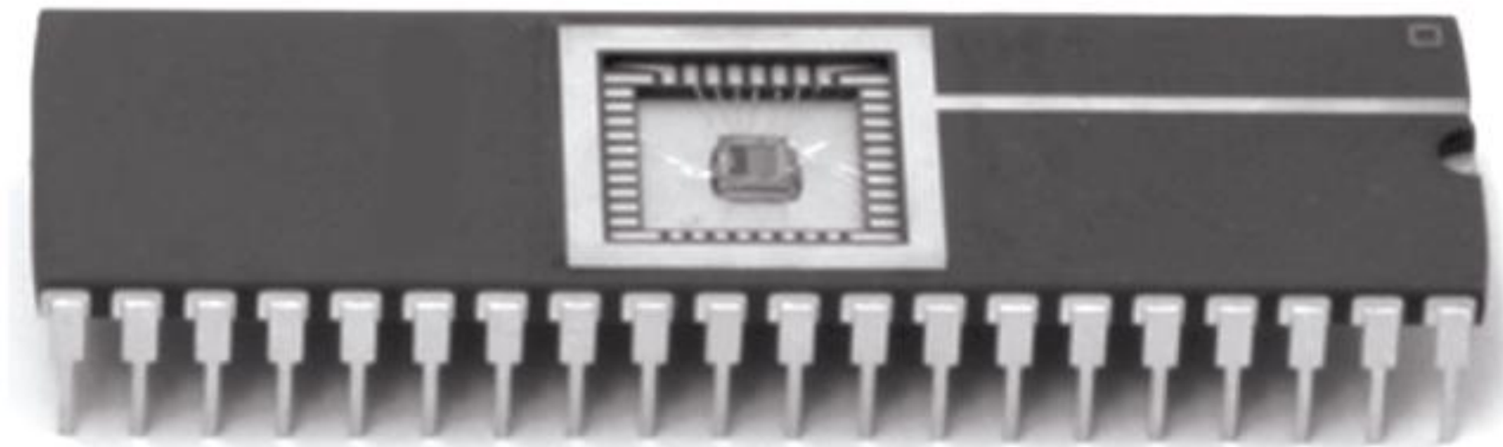
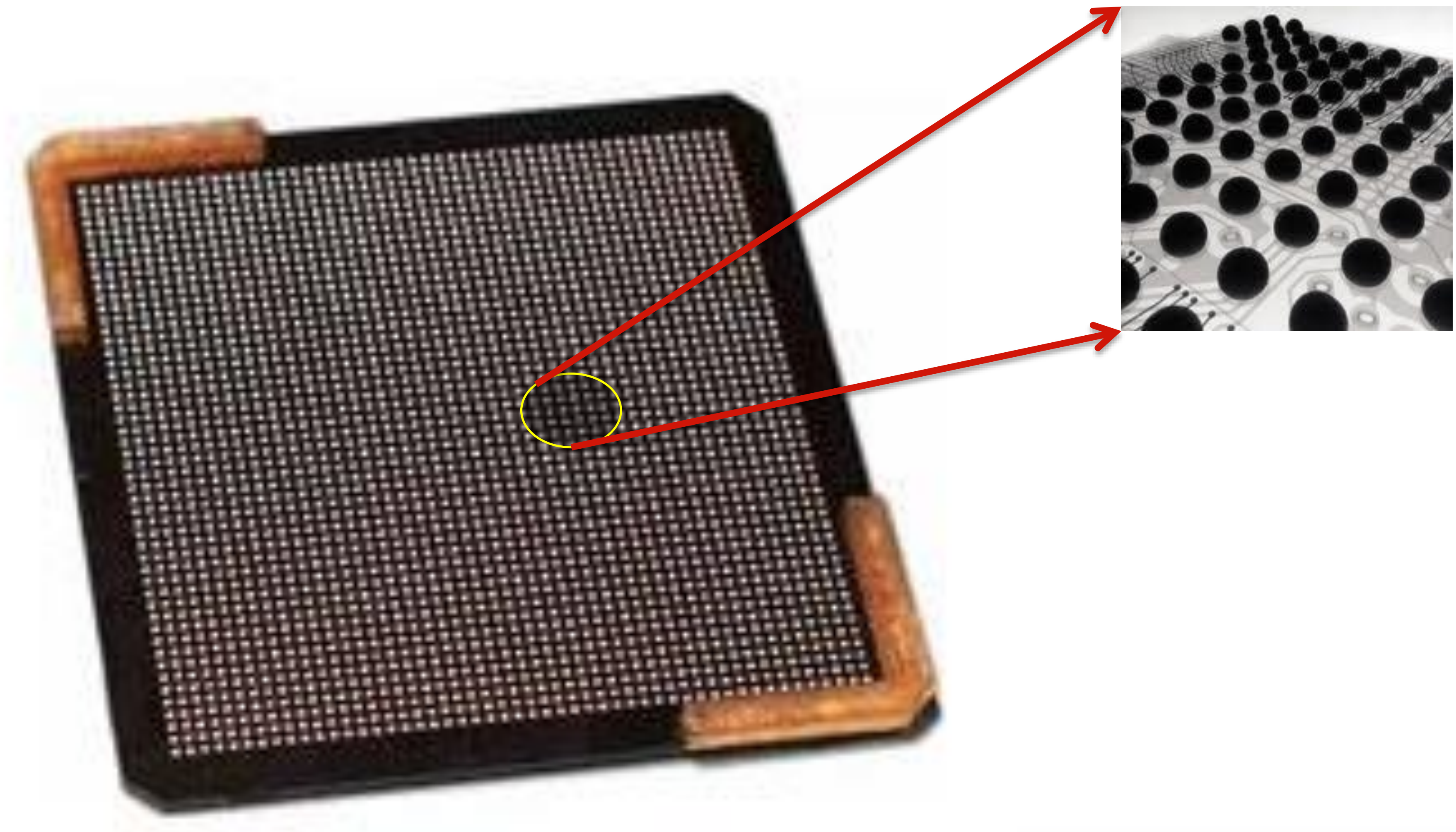


FIG 1.71 Chip in a 40-pin dual-inline package

Ball-Grid Array (BGA)….

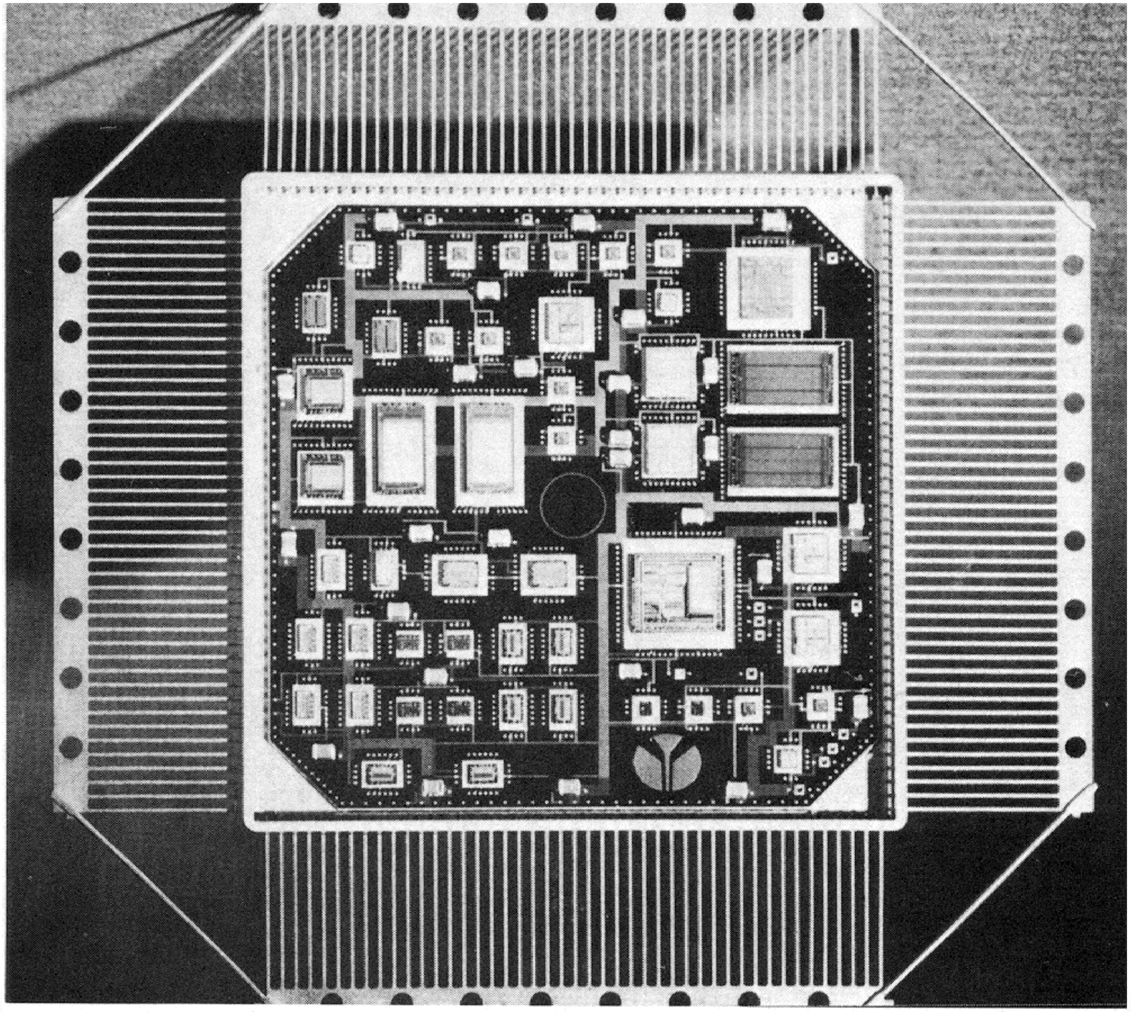


Package Parameters

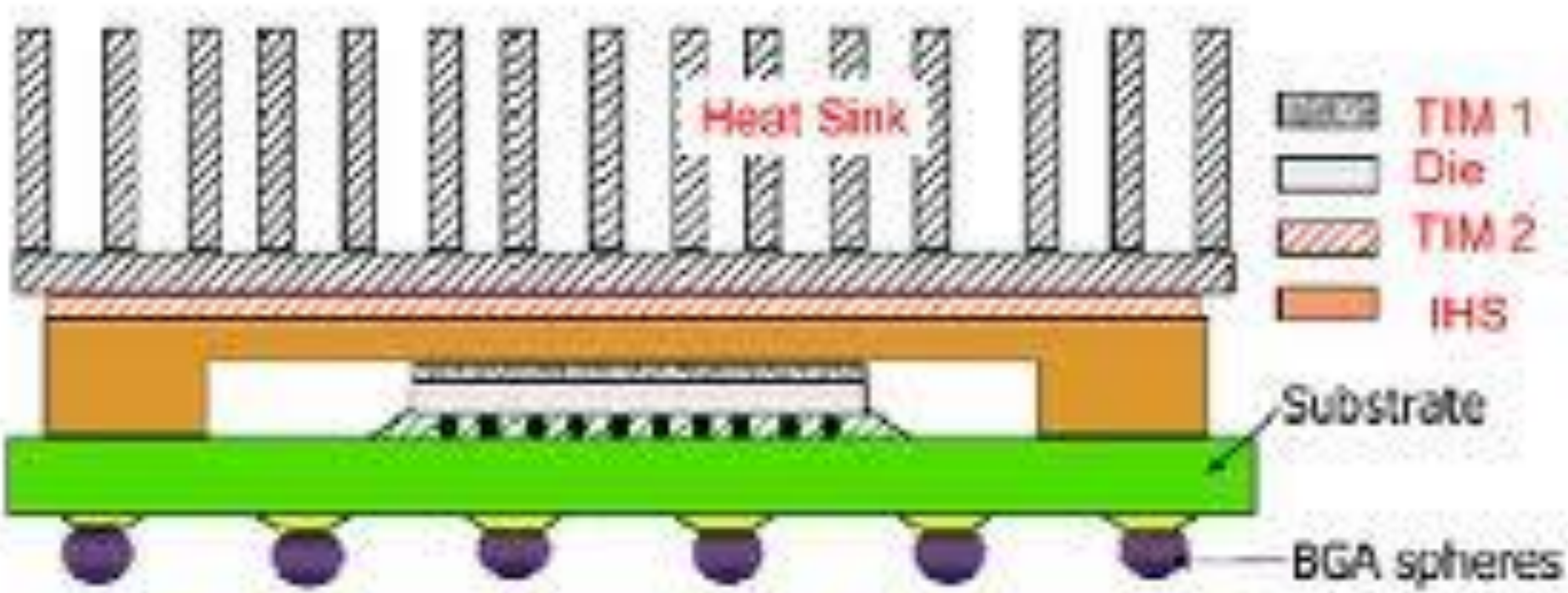
Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

Multi-Chip Modules



Cross-Section of a Packaged Chip with Heat-Sink



Note: heat sink is attached to the back-side of the chip….

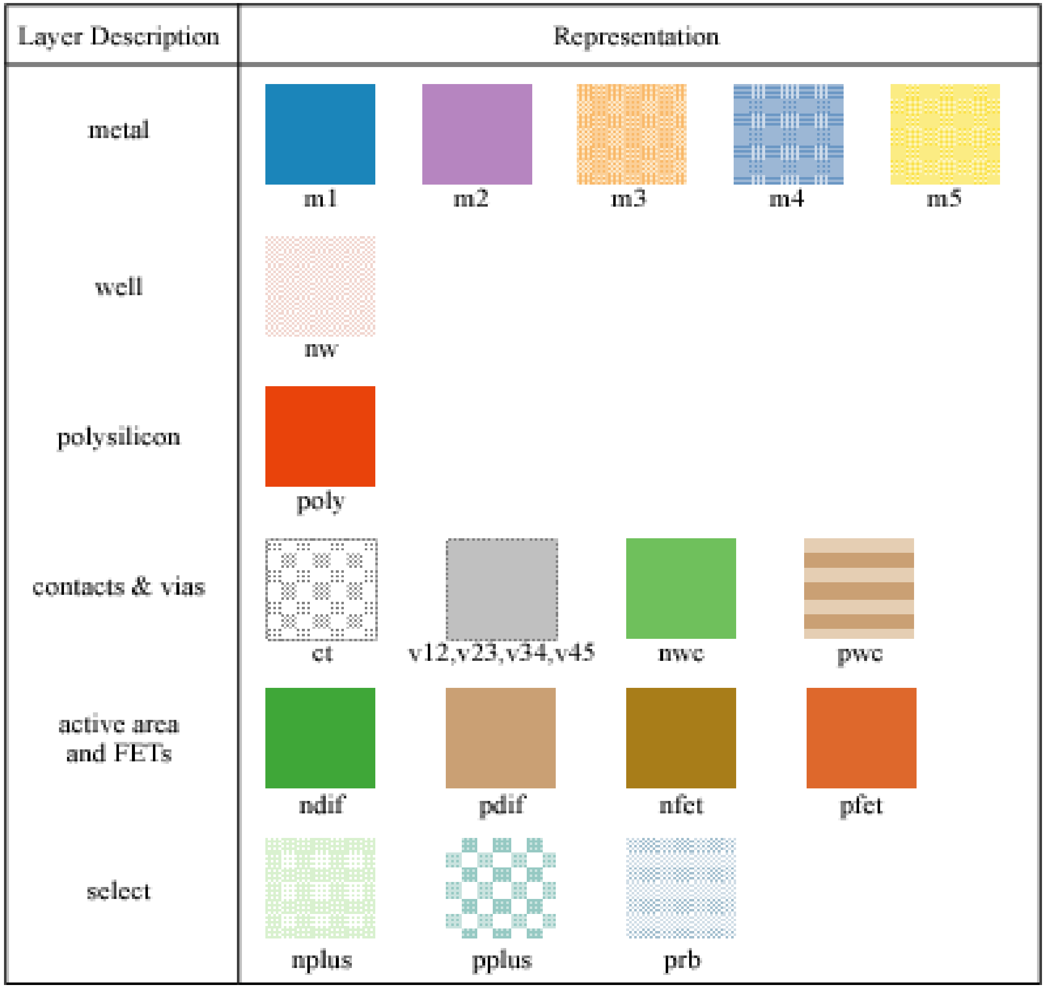
Design Rules….*how small? How close?*

- Interface between designer and process engineer
- Design rules are also determined based on reliability and manufacturability issues
- Guidelines for constructing process masks
- Unit dimension: Minimum poly-Si or metal-gate line width (L)
  - absolute dimensions (micron rules)
    - Used in industry, difficult to migrate from process to process
  - scalable design rules: lambda (λ) parameter
    - Used mostly in academic research, λ = L/2, more conservative….round up dimensions to an integer multiple of λ, but makes process migration easier…by simply changing value of λ

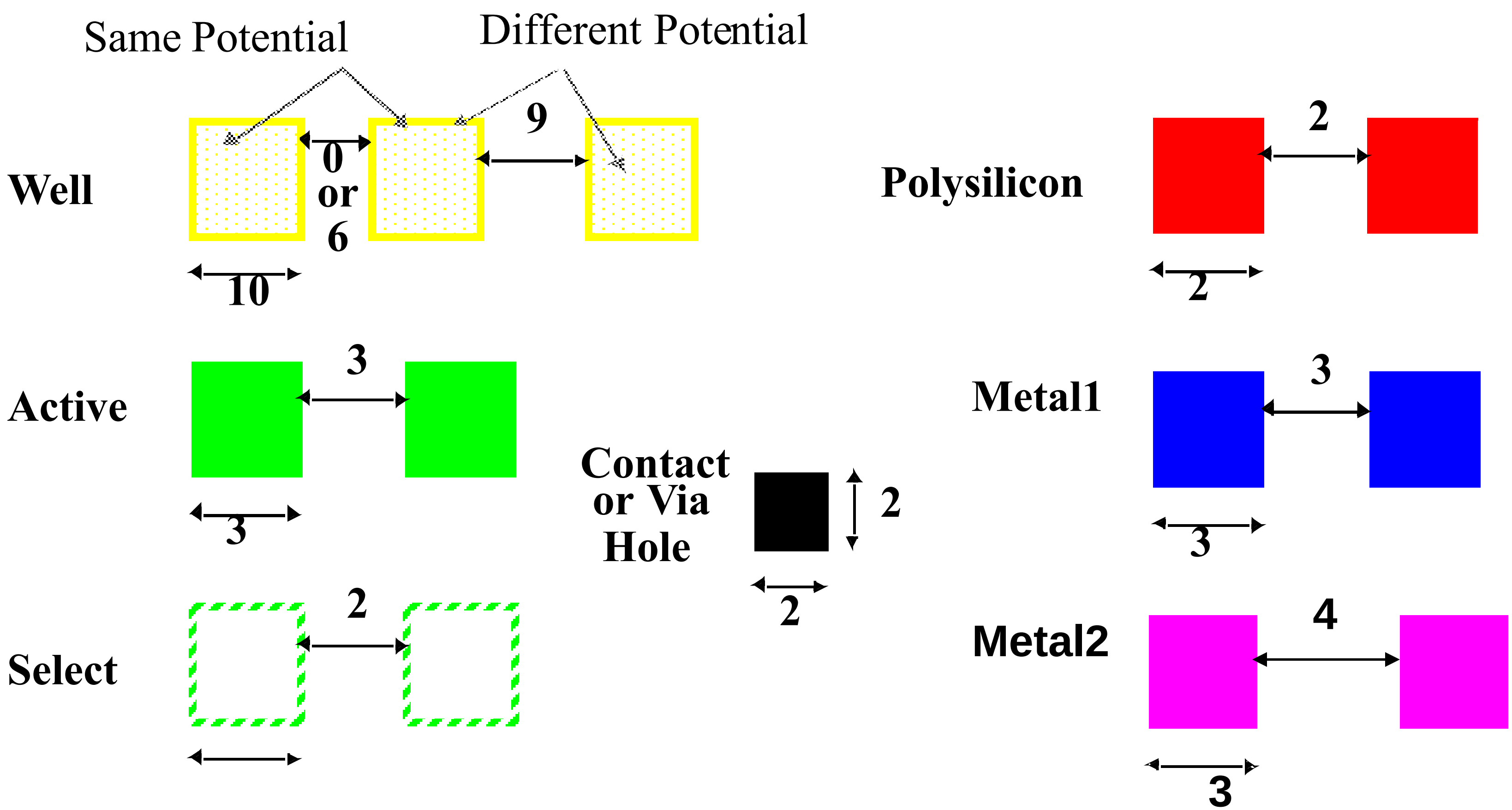
CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

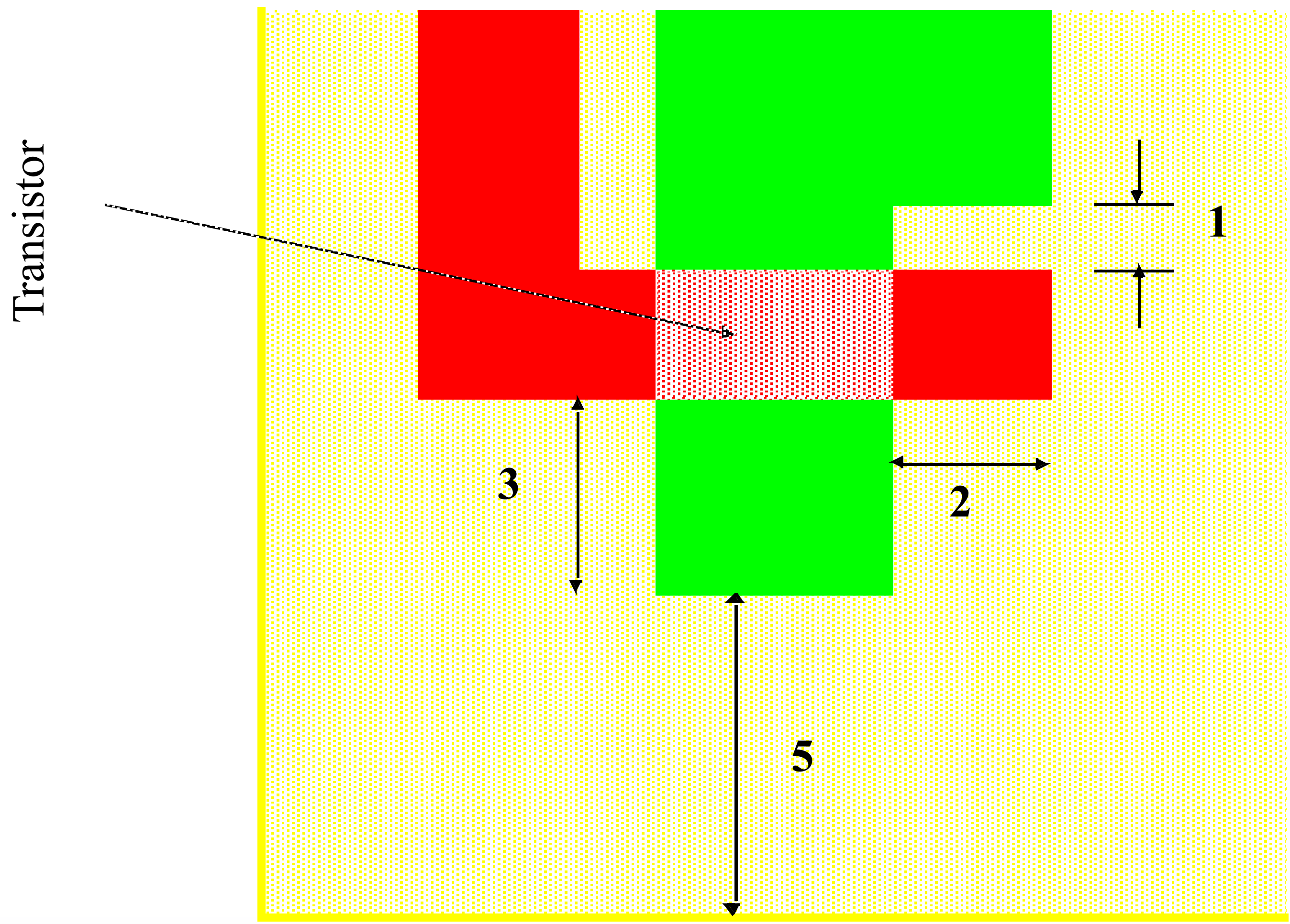
Layers in 0.25 μm CMOS process



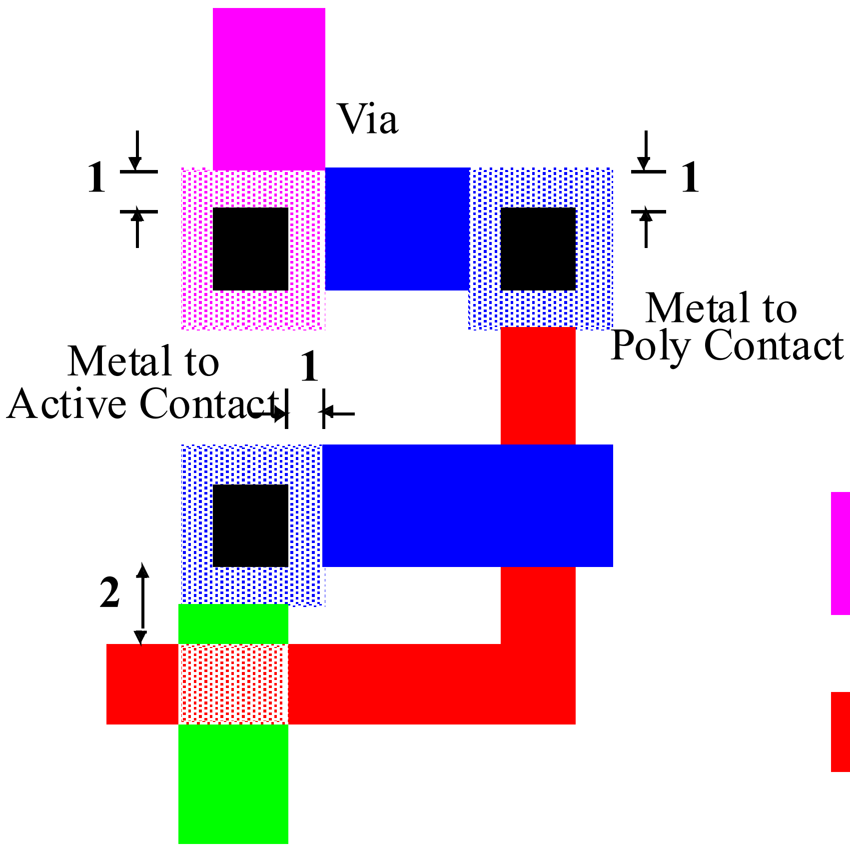
Intra-Layer Design Rules

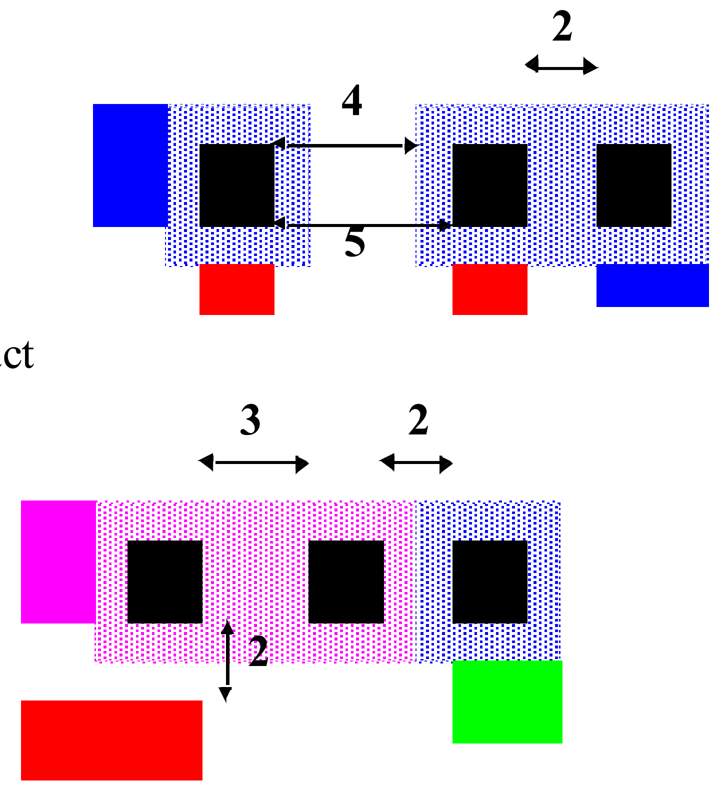


Transistor Layout

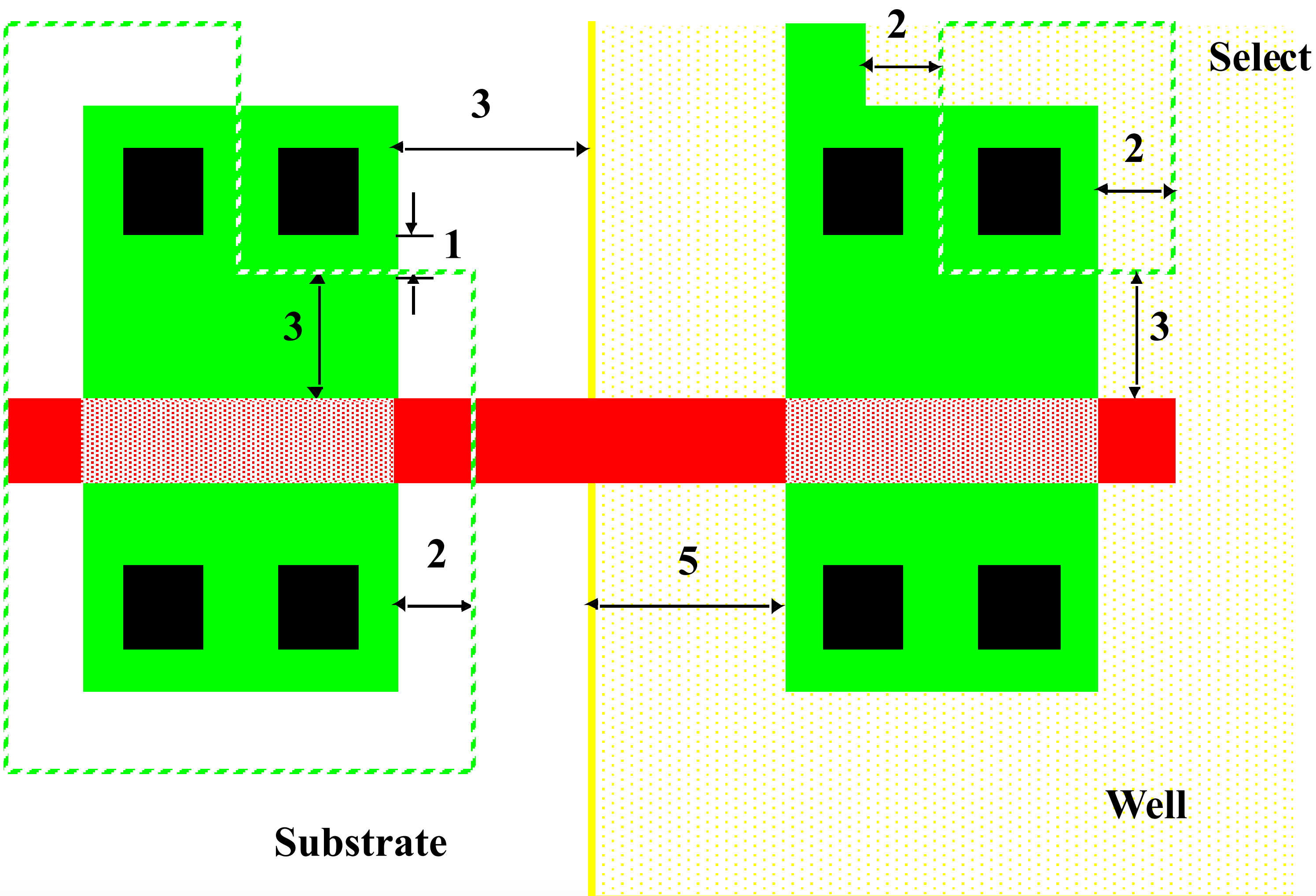


Vias and Contacts

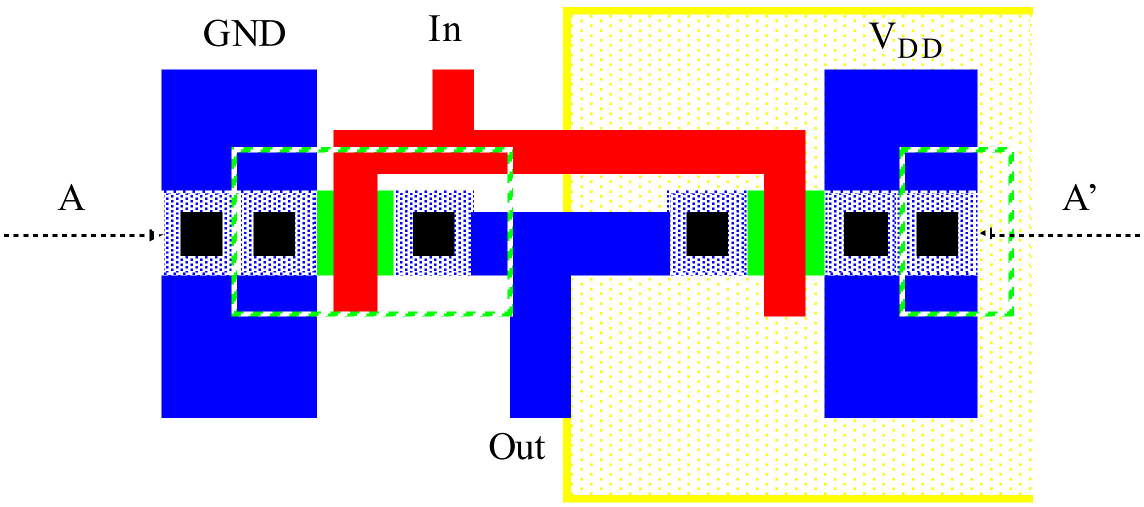




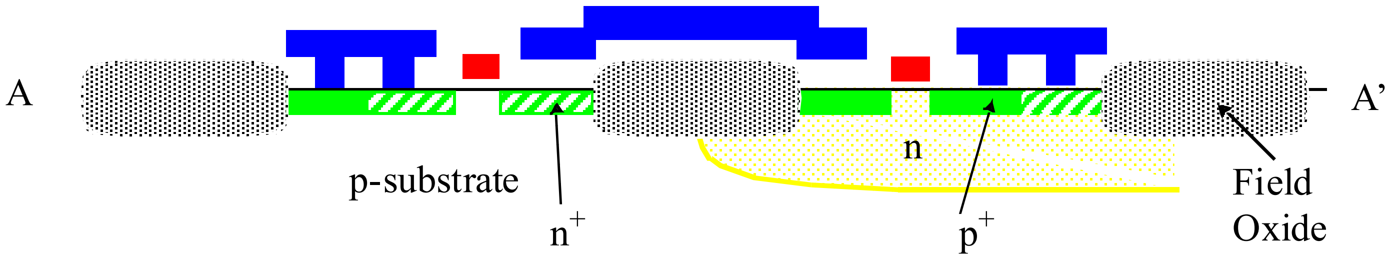
Select Layer….an interface for generating the mask



CMOS Inverter Layout

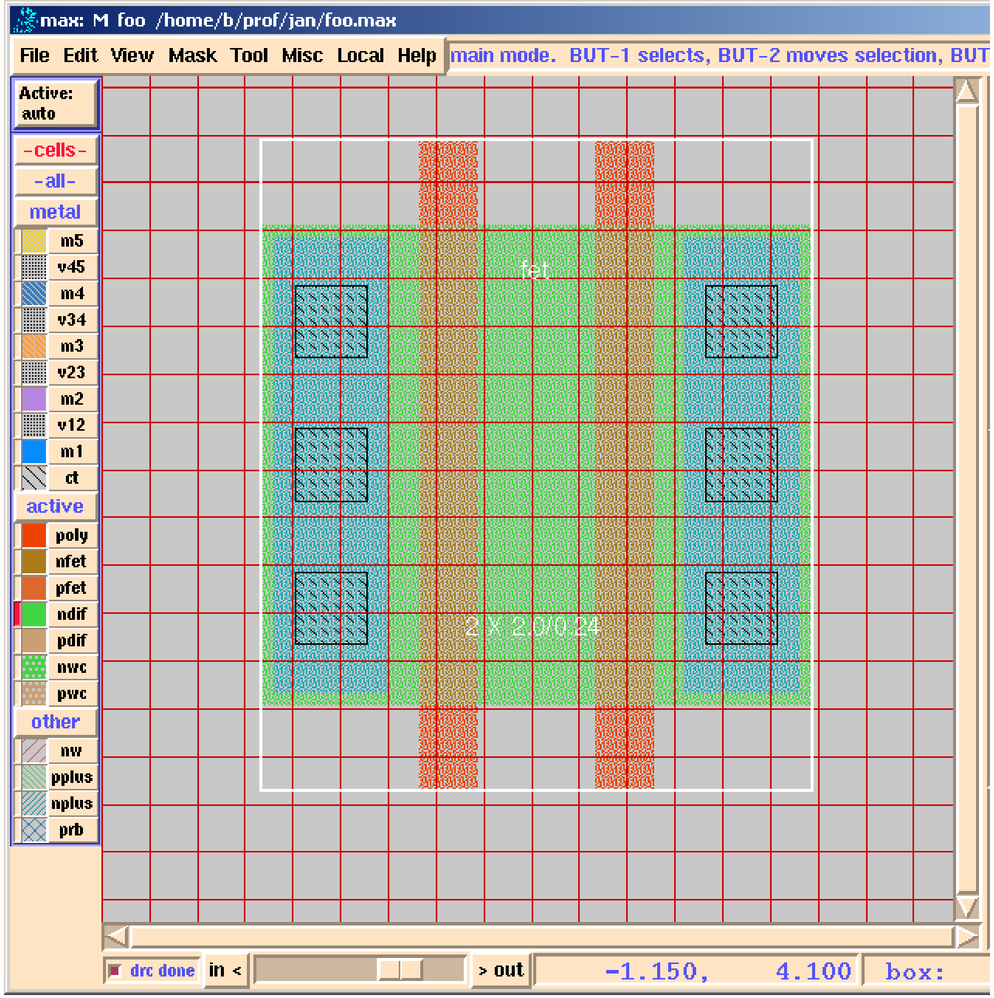


(a) Layout

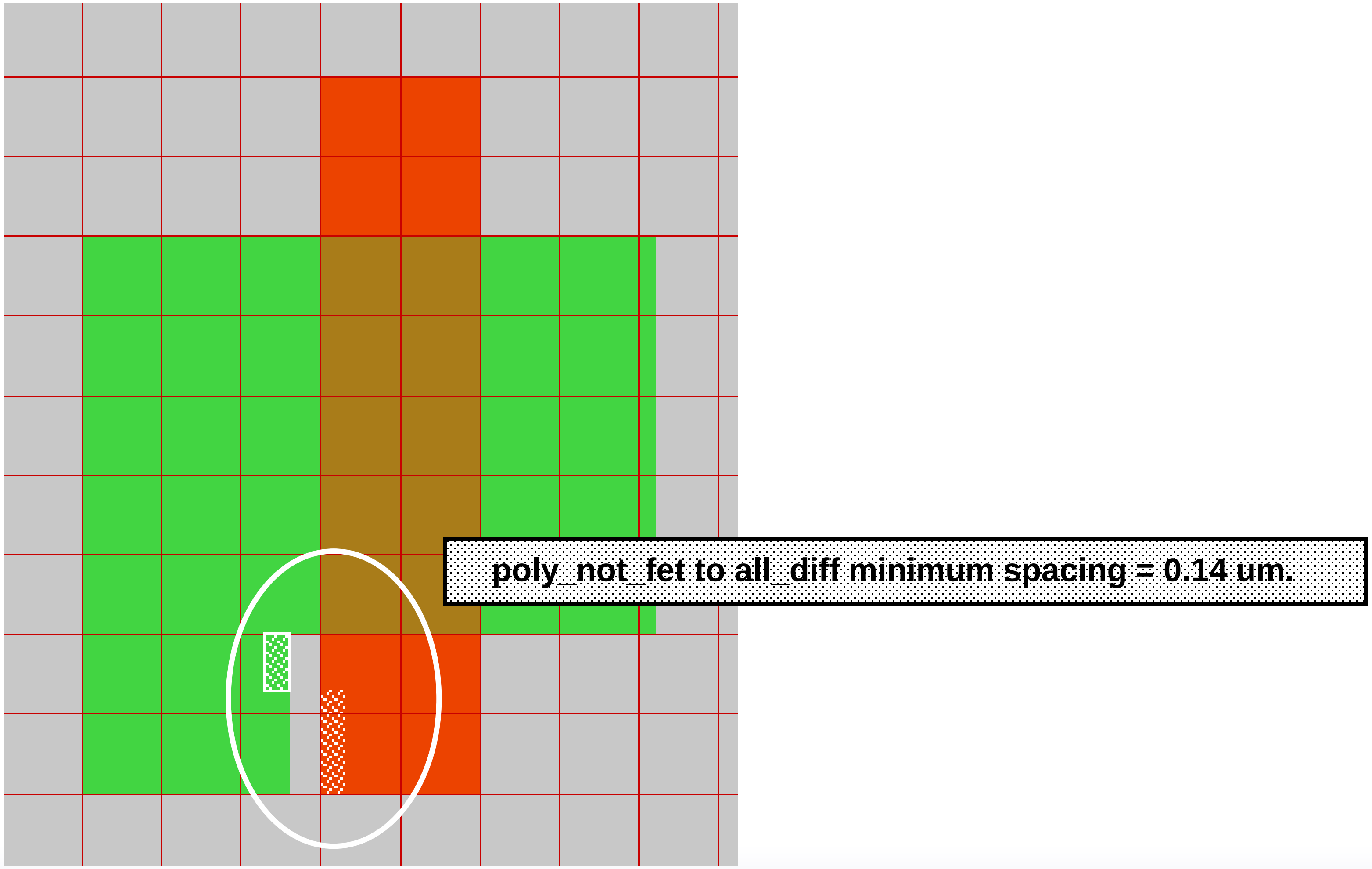


(b) Cross-Section along A-A'

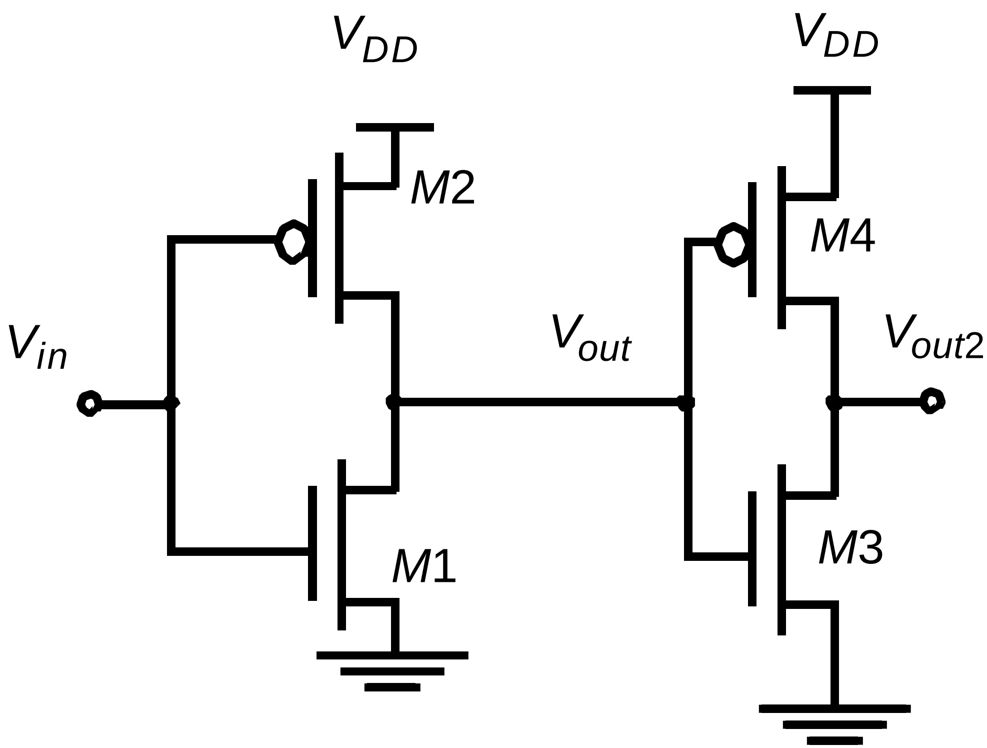
Layout Editor….MAX



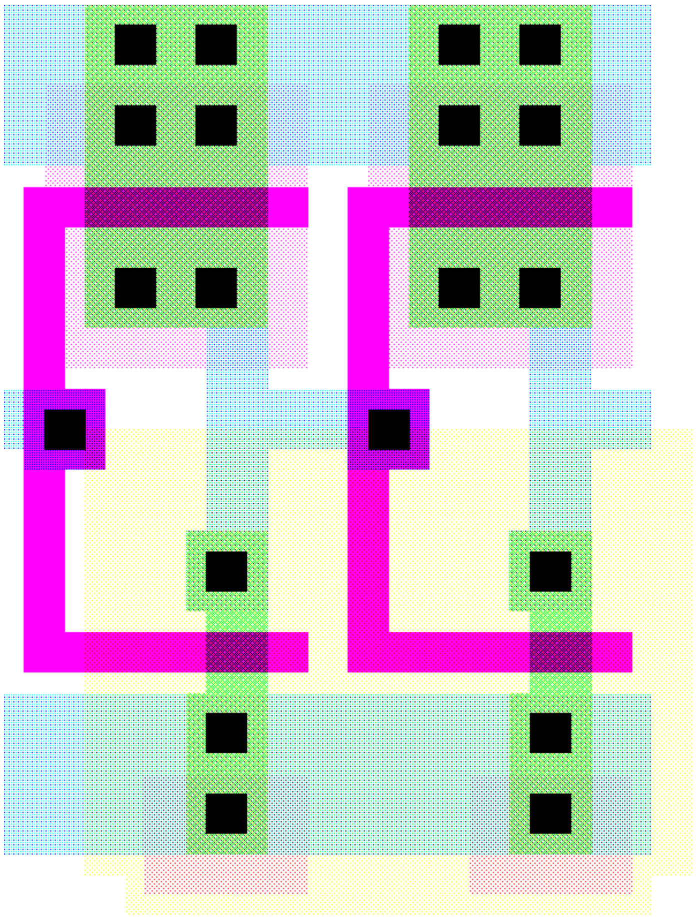
Design Rule Checker



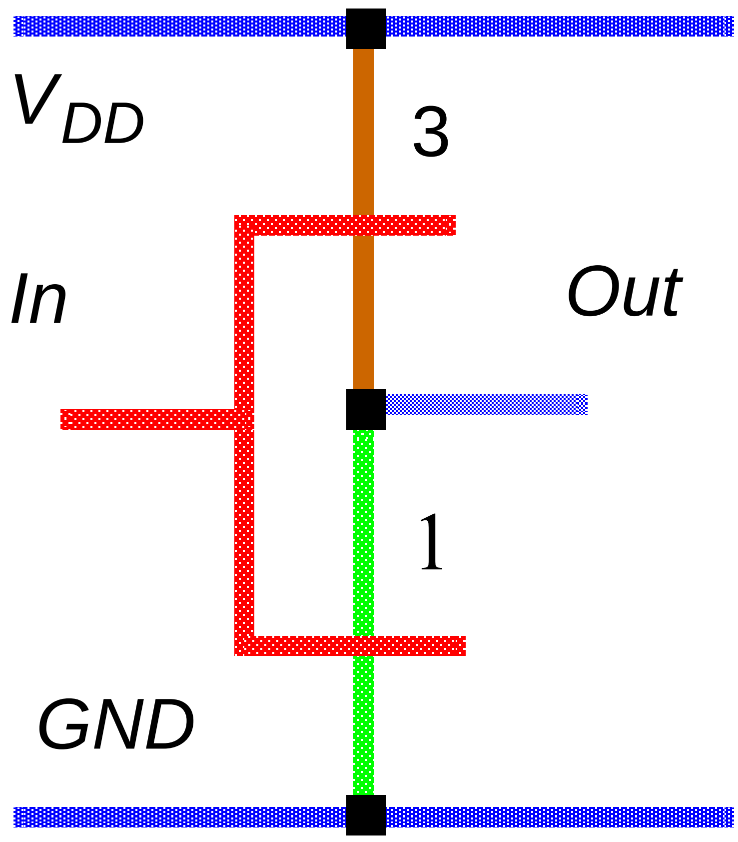
Circuit Under Design



Its Layout View



Stick Diagram…. *Cartoon of a layout*



Stick diagram of CMOS inverter

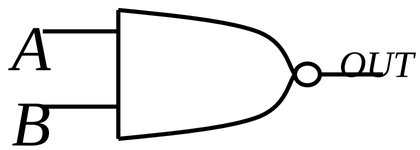
Allows quick layout planning & area estimation without detailed layout

- Dimensionless layout entities
- Only topology is important
- Determine height and width of cell by counting number of wire tracks and multiplying by wire pitch (width+spacing)

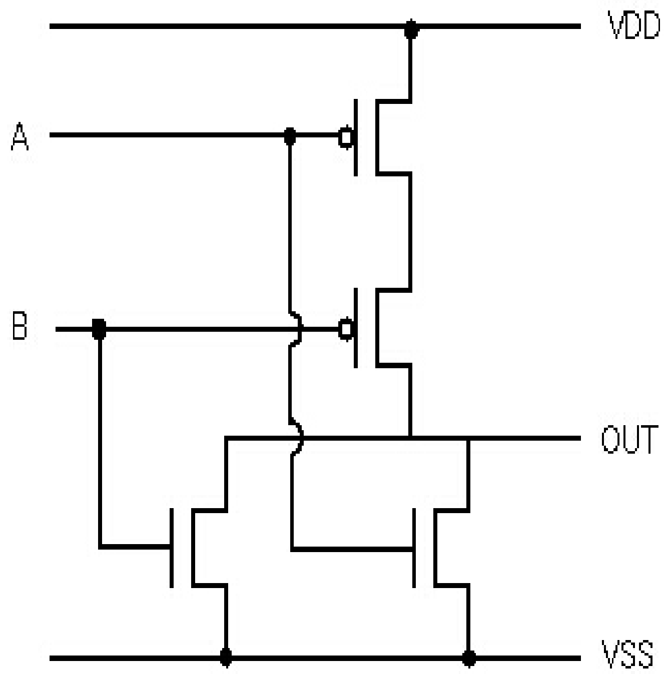
Color codes:

Blue – metal
Red – poly
Black - contact
Brown – p diffusion
Green – n diffusion

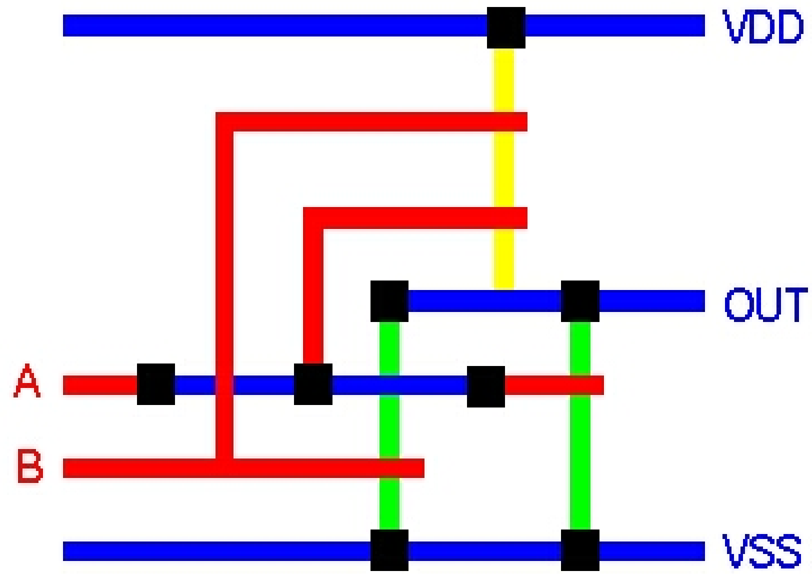
Stick Diagram….2-input NOR



NOR Gate



NOR gate in CMOS



Stick diagram of 2-input CMOS NOR

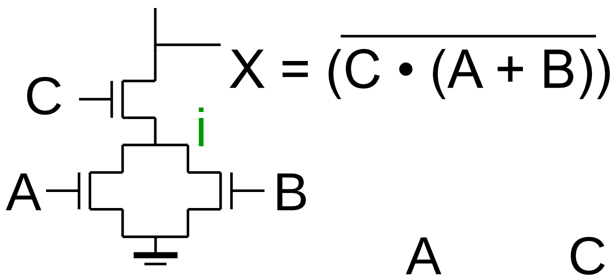
Euler Paths…

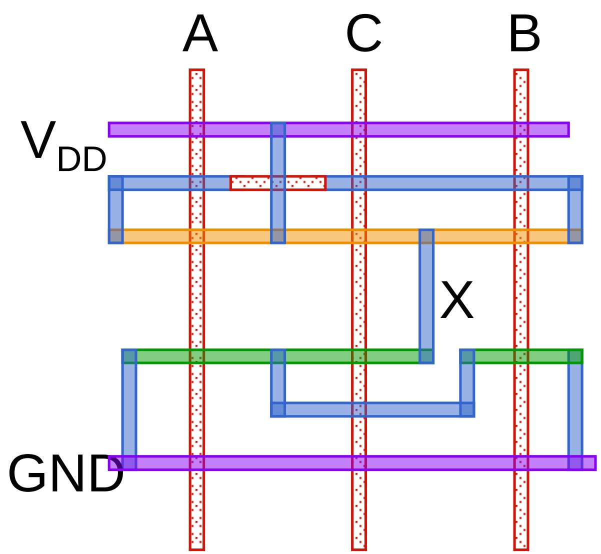
A graph is said to be containing an Euler path if it can be traced in 1 sweep without lifting the pencil from the paper and without tracing the same edge more than once.

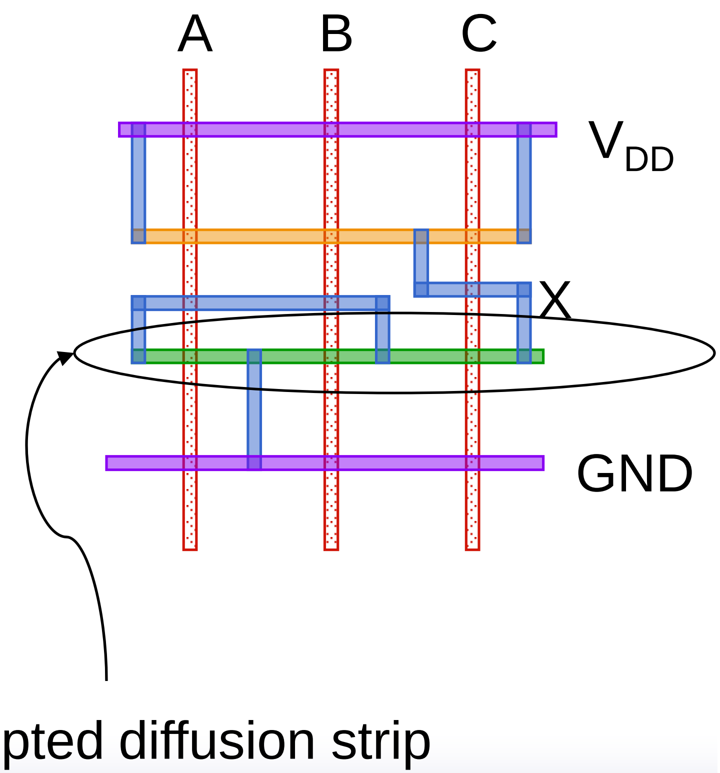
Vertices may be passed through more than once. The starting and ending points need not be the same.

An Euler circuit is similar to an Euler path, except that the starting and ending points must be the same.

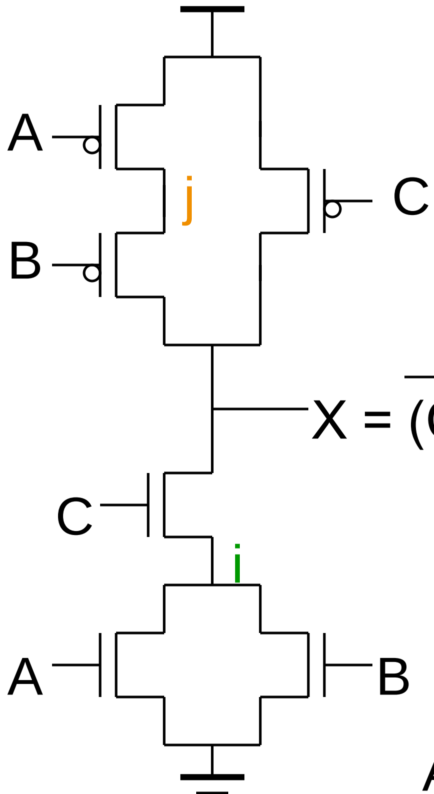
Two Stick Layouts of $\overline{(C \cdot (A + B))}$



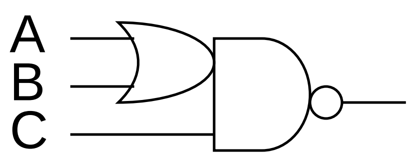


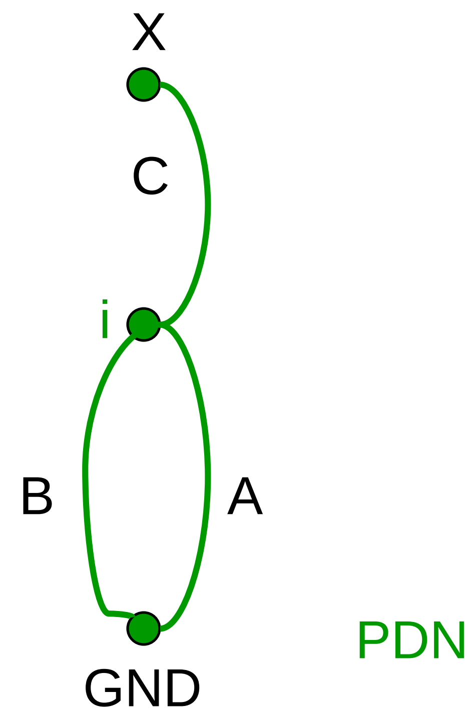


Logic Graph



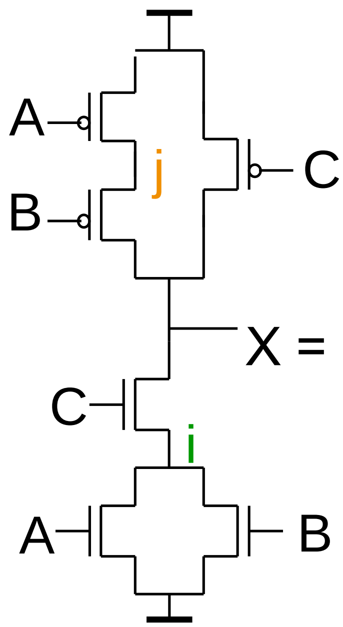
$X = \overline{(C \cdot (A + B))}$



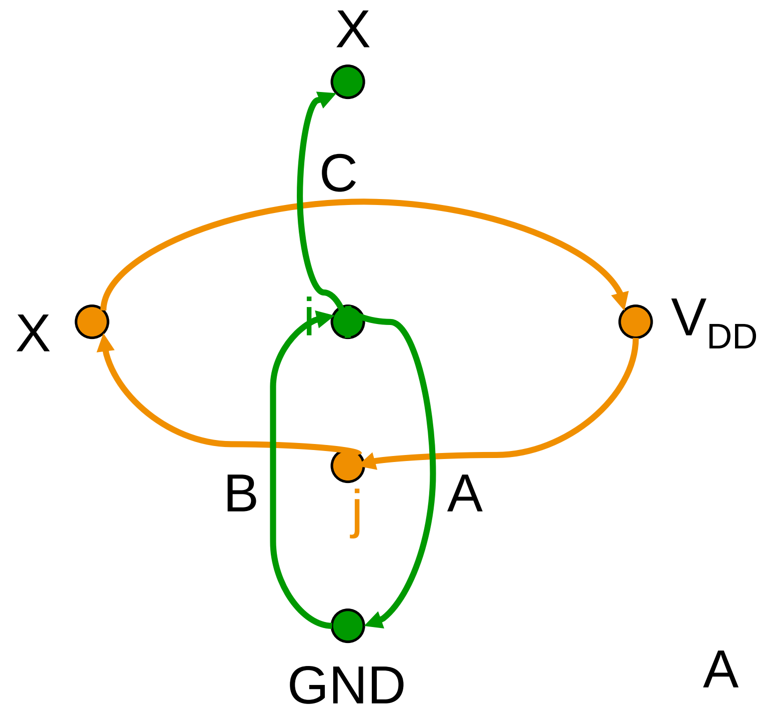


Consistent Euler Path

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.



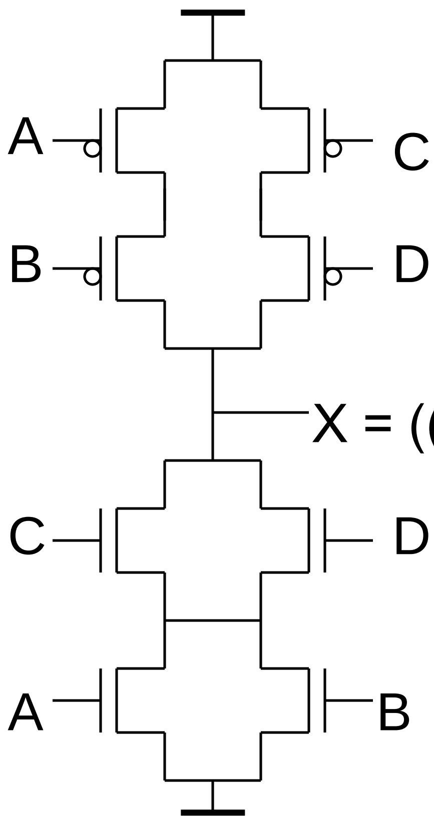
$X = \overline{(C \cdot (A + B))}$



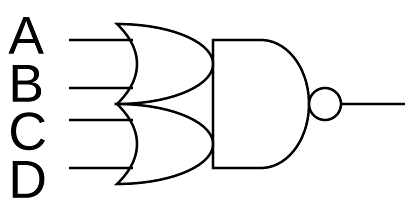
A B C

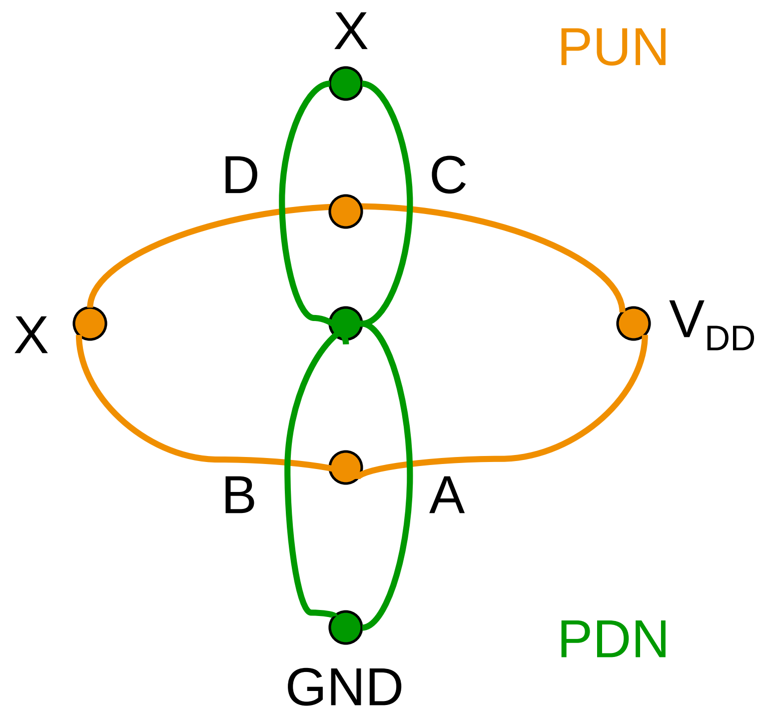
- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same)

Logic Graph

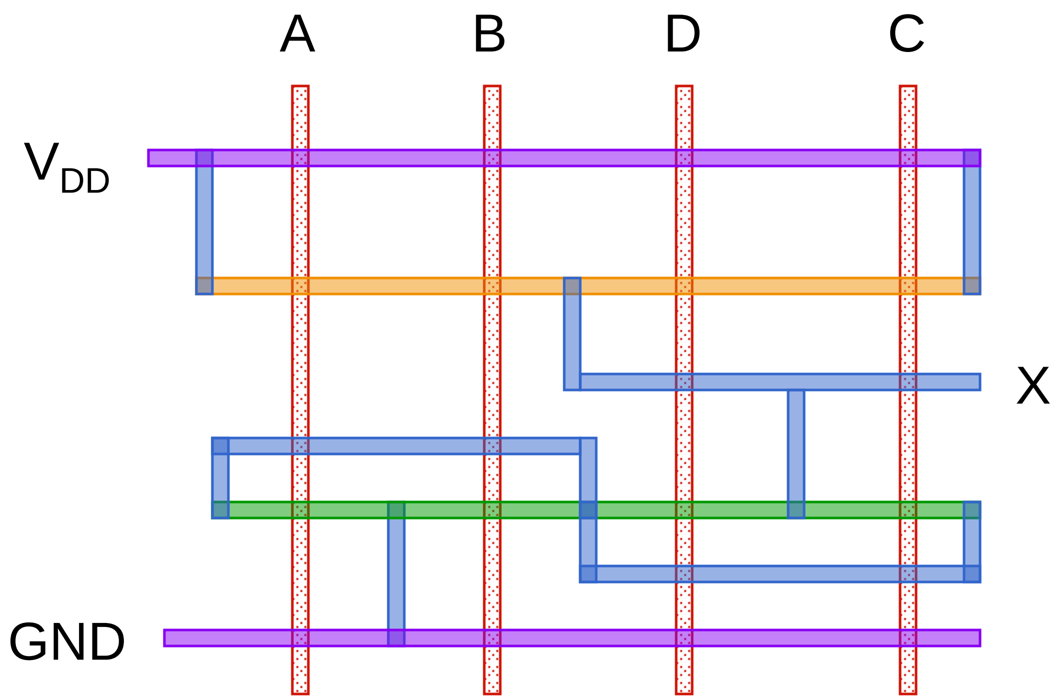


$X = \overline{((A+B)\bullet(C+D))}$





Layout



$$X = (\overline{(A+B)\bullet(C+D)})$$