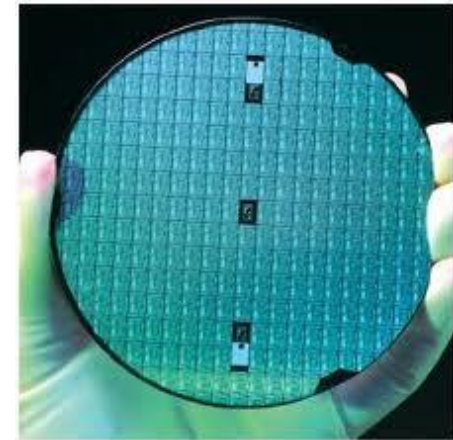
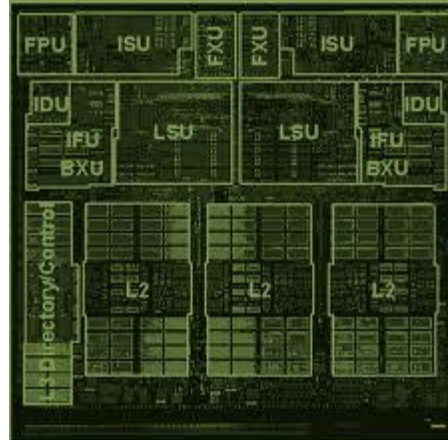
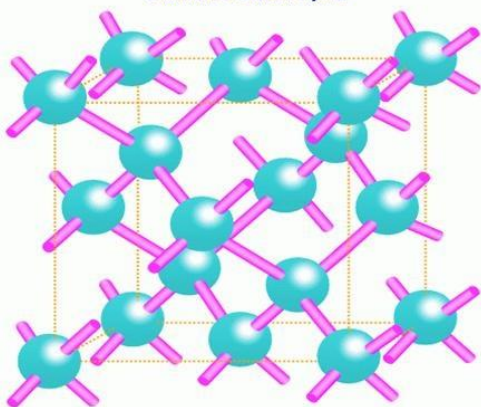


Structure of silicon crystal



ECE 122A

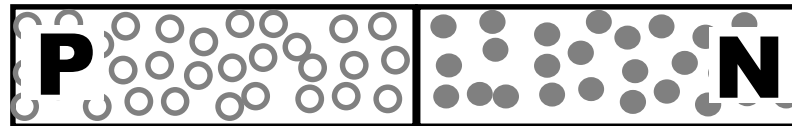
VLSI Principles

Lecture 6

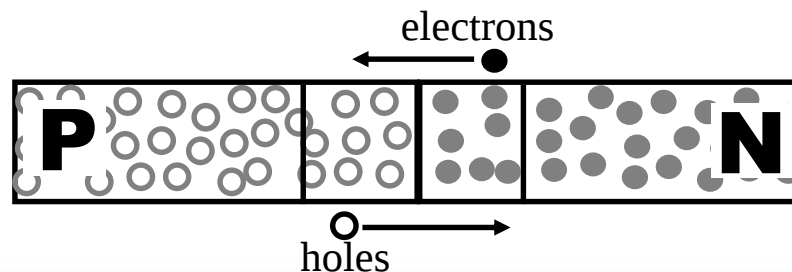
Prof. Kaustav Banerjee
Electrical and Computer Engineering
University of California, Santa Barbara
E-mail: kaustav@ece.ucsb.edu

P/N Junctions

- ❑ What happens when you put two types of semiconductors together?

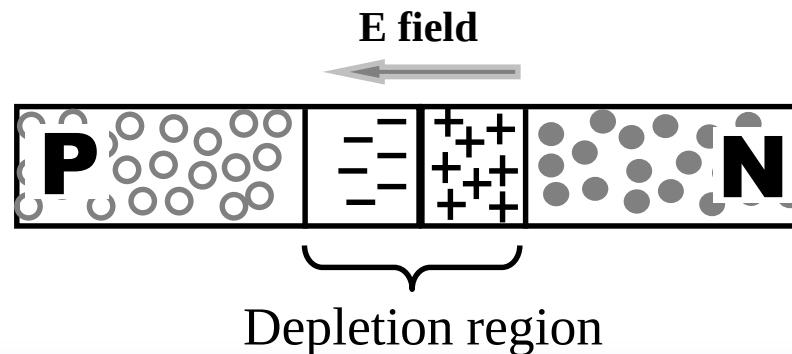


- Large concentration gradient at junction
 - Electrons diffuse from N to P side
 - Holes diffuse from P to N side

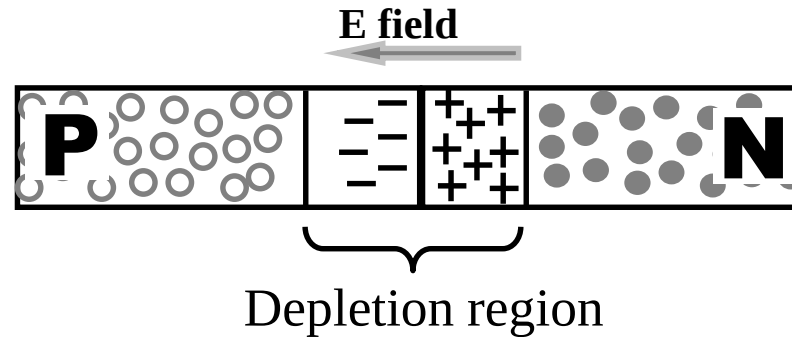


P/N Junctions (2)

- Immobile ions are left behind
 - Electrons leave +ve charged ions on N side
 - Holes leave –ve charged ions on P side
 - Electric field forms, from N to P
 - E-field causes drift in opposite direction as diffusion
 - **Equilibrium!** No current flows

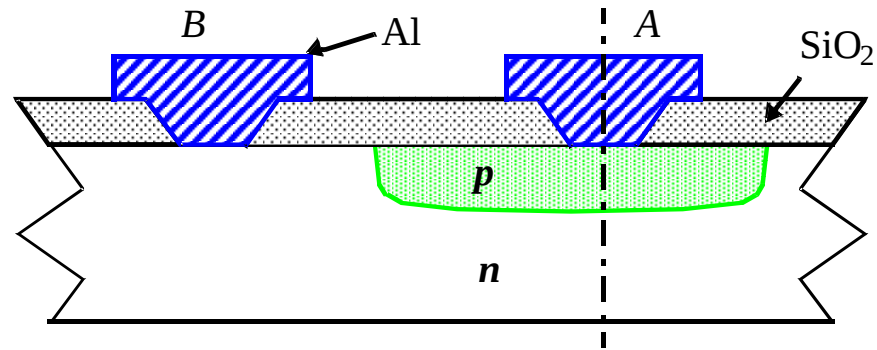


Depletion Region

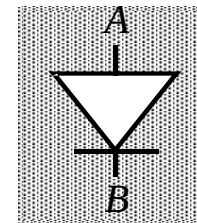
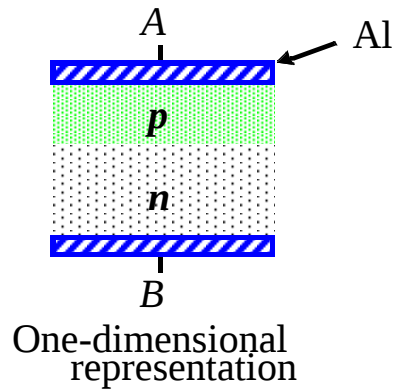


- Depletion region forms around junction
 - “Depleted” of any mobile charges (holes or electrons)
 - Charge in depletion region due to fixed ions
 - Electric field causes a potential difference across junction: known as built-in voltage V_0

The Diode



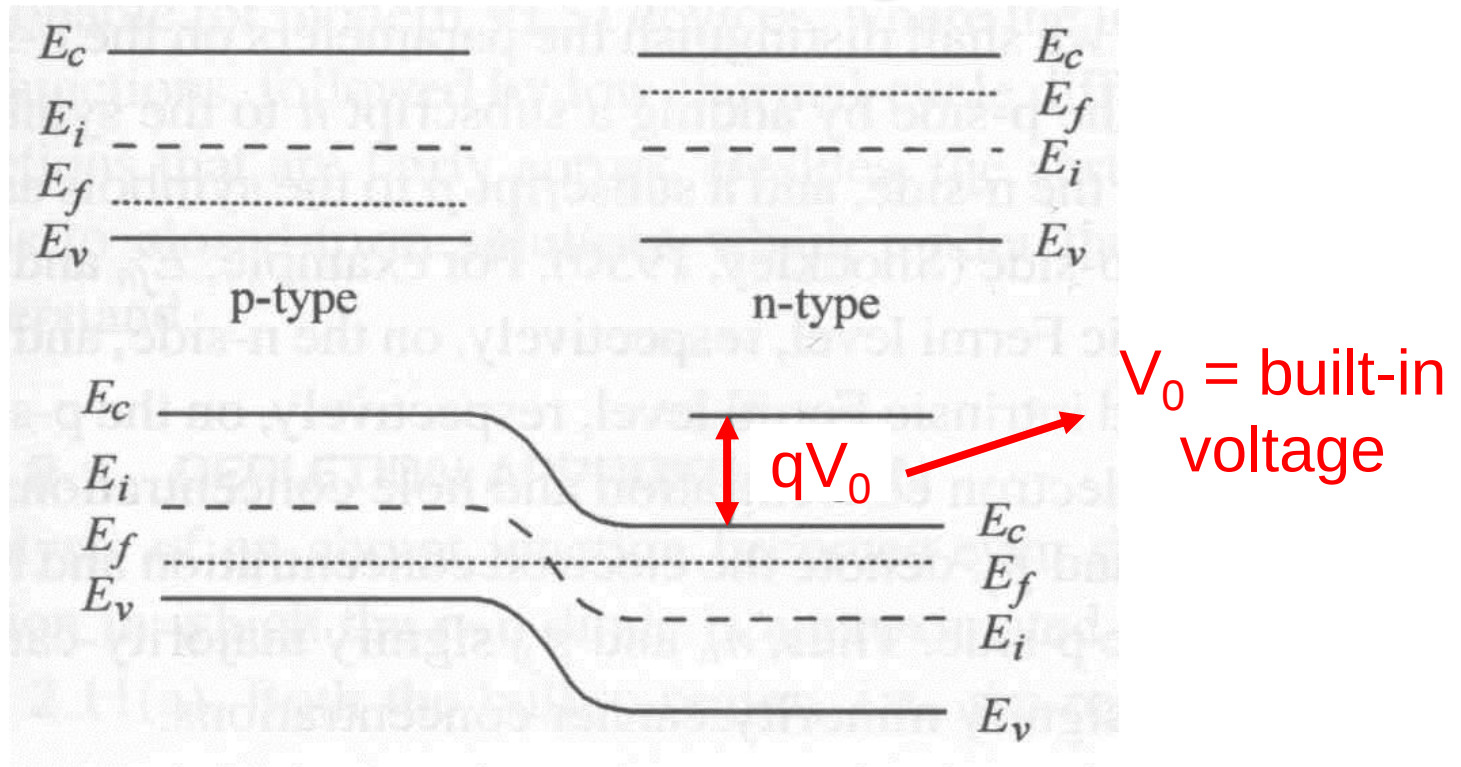
Cross-section of pn junction in an IC process



diode symbol

Mostly occurring as parasitic element in Digital ICs

P/N Junction Band Diagram



- At thermal equilibrium, no net current flow
 - When drift+diffusion currents=0, $\frac{dE_f}{dx} = 0$
- Bands must bend so that Fermi level is constant

PN Junction Equations

$$E_{Fn} - E_{in} = kT \ln\left(\frac{N_D}{n_i}\right) \quad E_{ip} - E_{Fp} = -kT \ln\left(\frac{n_i}{N_A}\right)$$

➤ Built-in potential or contact potential

➤ difference between energy bands on p and n side of the junction)

$$qV_0 = E_{ip} - E_{in}$$

$$V_0 = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Strongly-doped
junction

P/N Junction Example

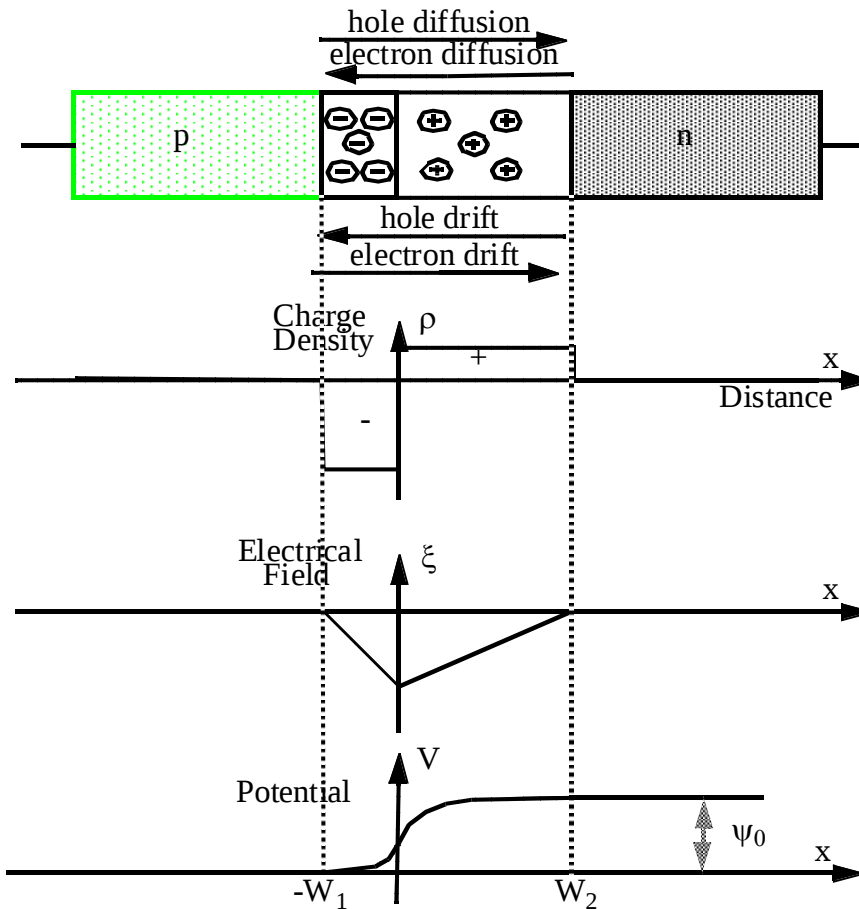
A diode is created from two materials:

- Si doped with 10^{16} cm^{-3} Boron
- Si doped with 10^{17} cm^{-3} Arsenic

1. Find electron and hole concentration on each side of the junction
2. Find position of each Fermi level
3. Find built-in voltage V_0

Depletion Region

which side is more heavily doped?



(a) Current flow.

Drift current equals diffusion current under equilibrium:
zero net current

(b) Charge density.

Charge density higher on p side than n side since $N_A > N_D$

(c) Electric field.

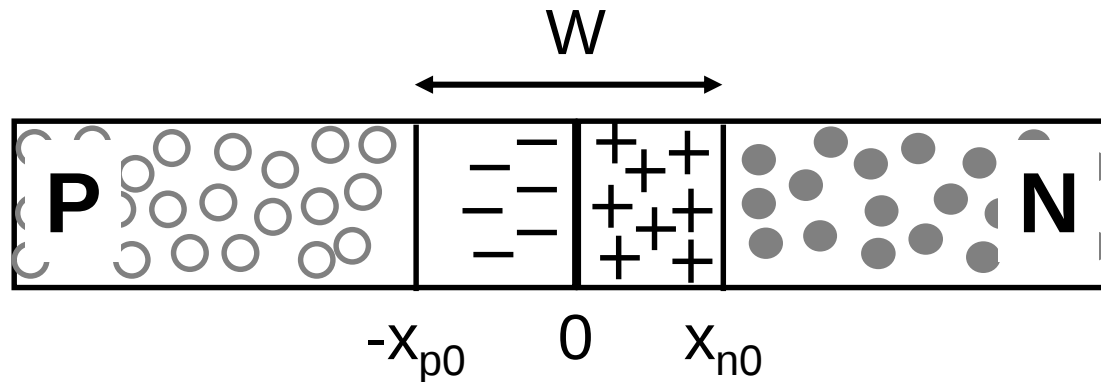
(d) Electrostatic potential.

Note:

$$d\xi/dx = \rho/\epsilon$$

$$\xi = -dV/dx$$

Abrupt PN Junctions



Width of depletion region:

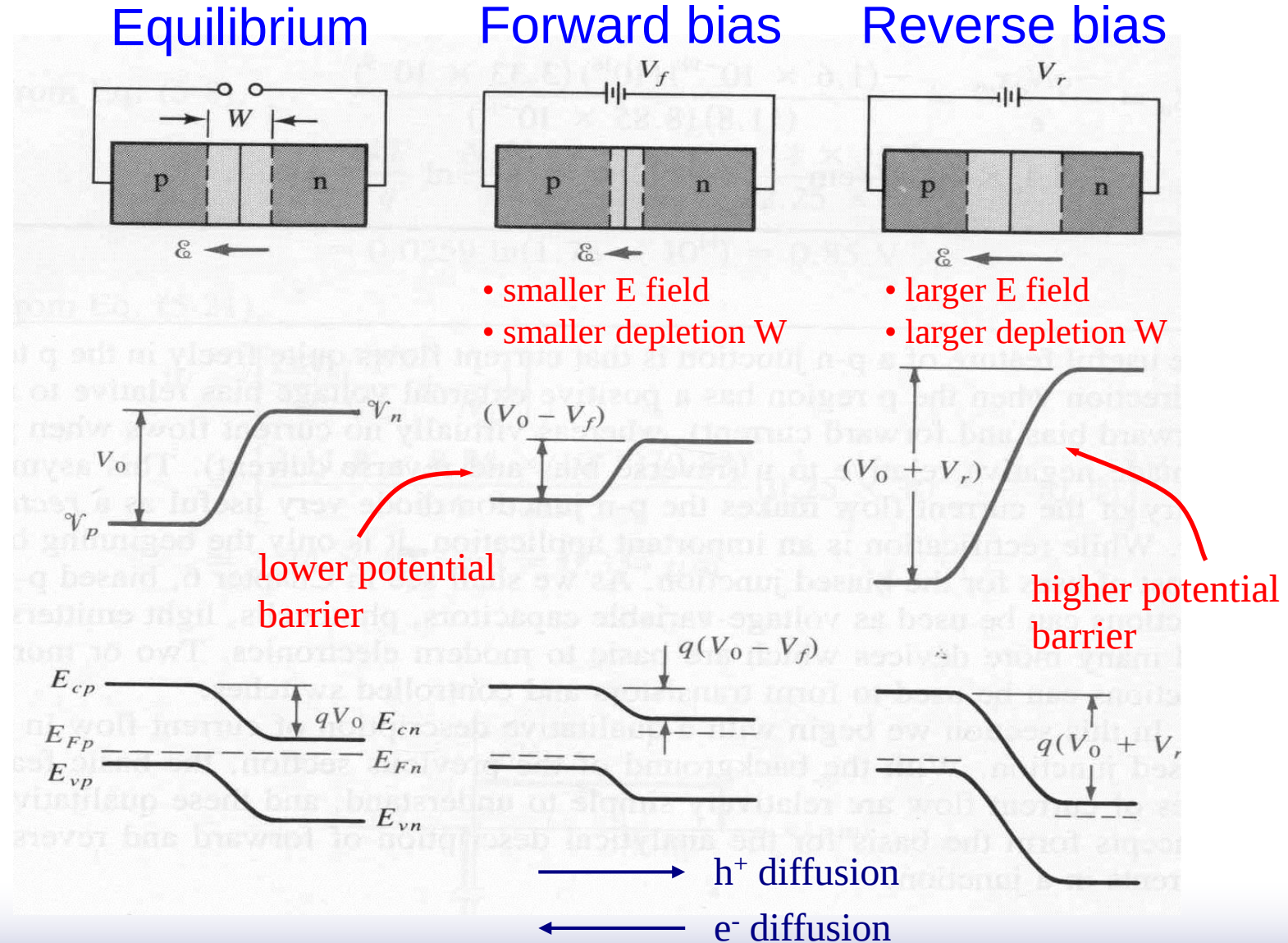
$$W_d = \sqrt{\frac{2\varepsilon}{q} \frac{(N_a + N_d)}{N_a N_d} V_0}$$

Built-in potential $\swarrow$

Try to derive this equation.....

Hint: Start with Gauss's Law...and get to the Poisson's equation ($dE/dx = \rho/\varepsilon$), then apply that to each of the two layers in the depletion region.

Bias Effects on PN Junction



Bias Effect on Depletion Width

- ❑ When biased, electric field in depletion region changes
 - Forward bias: reduces electric field
 - Reverse bias: increases electric field
- ❑ Electric field is a result of uncovered charges. Therefore depletion width must change
 - Forward bias: less charges needed. Depletion width reduces
 - Reverse bias: more charges needed. Depletion region increases.

Bias Effect on Depletion Width

Width of depletion region w/o bias:

$$W_d = \sqrt{\frac{2\varepsilon}{q} \frac{(N_a + N_d)}{N_a N_d} V_0}$$

Width of depletion region with bias V :

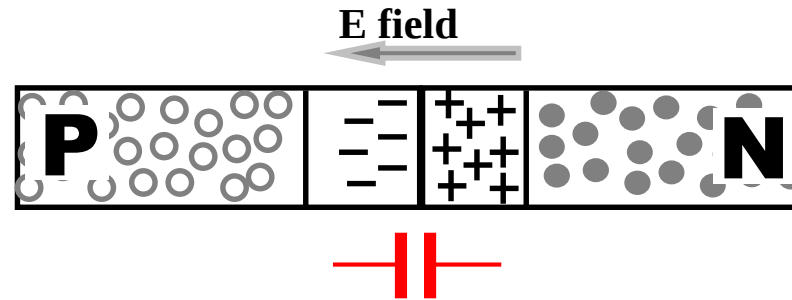
$$W_d = \sqrt{\frac{2\varepsilon}{q} \frac{(N_a + N_d)}{N_a N_d} (V_0 - V)}$$

Note:

If V is +ve (FB), W_d reduces

If V is -ve (RB), W_d increases

Capacitance of P/N Junction



- Separated charges result in depletion region capacitance
- Similar to **parallel-plate** capacitor

Charge in depletion region:

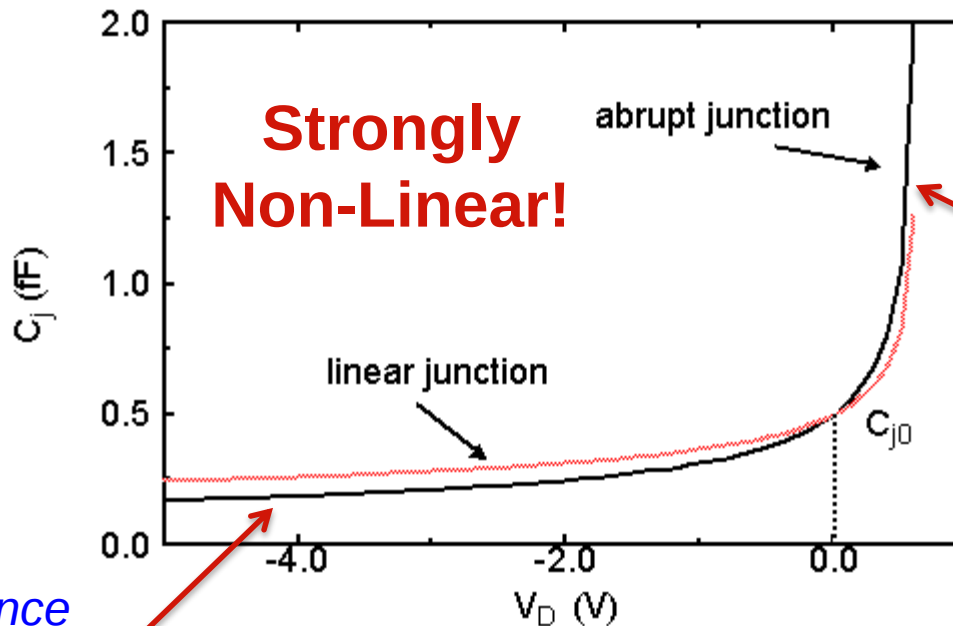
$$Q_j = A \sqrt{2q\epsilon \frac{N_d N_a}{N_d + N_a} (V_0 - V)}$$

Capacitance:

$$C_j = \frac{A}{2} \sqrt{\frac{2q\epsilon}{V_0 - V} \frac{N_d N_a}{N_d + N_a}}$$

Junction Capacitance

A small change in voltage (dV_D) applied to the junction causes a change in the space charge (dQ_j): $C_j = dQ_j/dV_D$ C_j is voltage dependent



Capacitance increases with forward bias (since depletion width decreases)

Capacitance reduces with reverse bias (since depletion width increases)

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

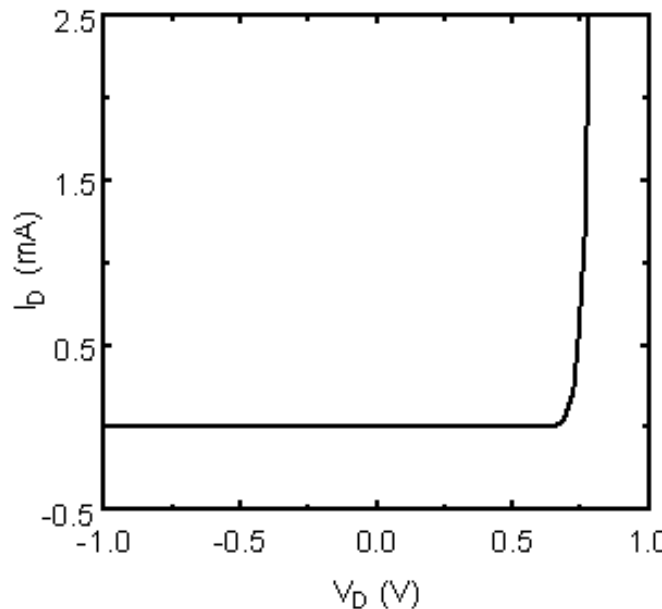
$m = 0.5$: abrupt junction
 $m = 0.33$: linear junction

C_{j0} = cap. under zero bias, m is the grading co-efficient

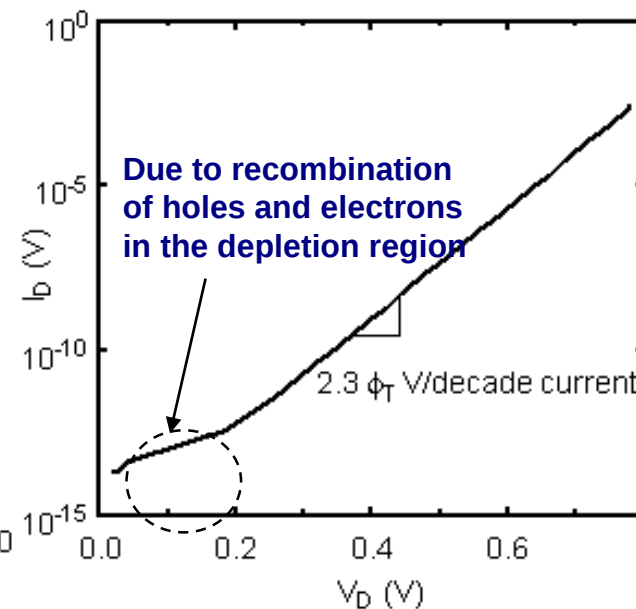
Diode Equation

- **Forward bias**: barrier lowered, diffusion current dominates
- **Reverse bias**: barrier raised, only current is small drift current of minority carriers
- Diode only lets **current flow in one direction**
- **Diode equation**: $I = I_s (e^{qV/kT} - 1)$

Diode Current



(a) On a linear scale.



(b) On a logarithmic scale (forward bias).

Current increases by a factor of 10 every 60 mV

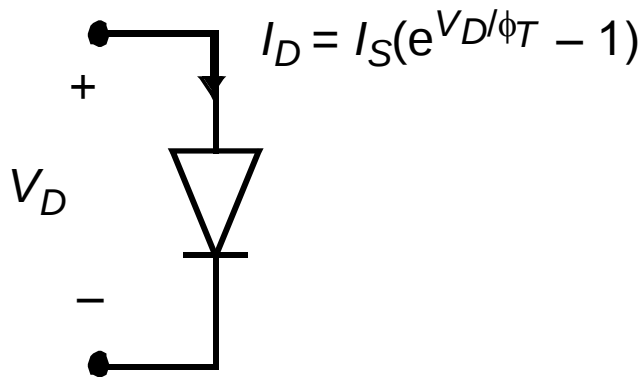
Ideal diode equation:
$$I_D = I_S \left(e^{V_D / \phi_T} - 1 \right)$$

I_D = diode current, V_D = diode bias voltage

I_S = saturation current of diode (constant) proportional to diode area, and function of the doping levels and width of neutral regions....determined empirically (**saturates at large RB**)

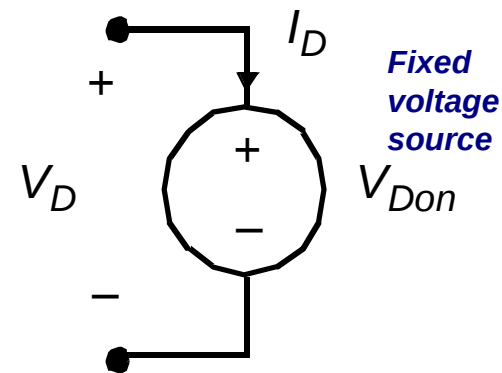
Φ_T = thermal voltage = $kT/q = 26\text{mV}$ at 300K

Models for Manual Analysis



(a) Ideal diode model

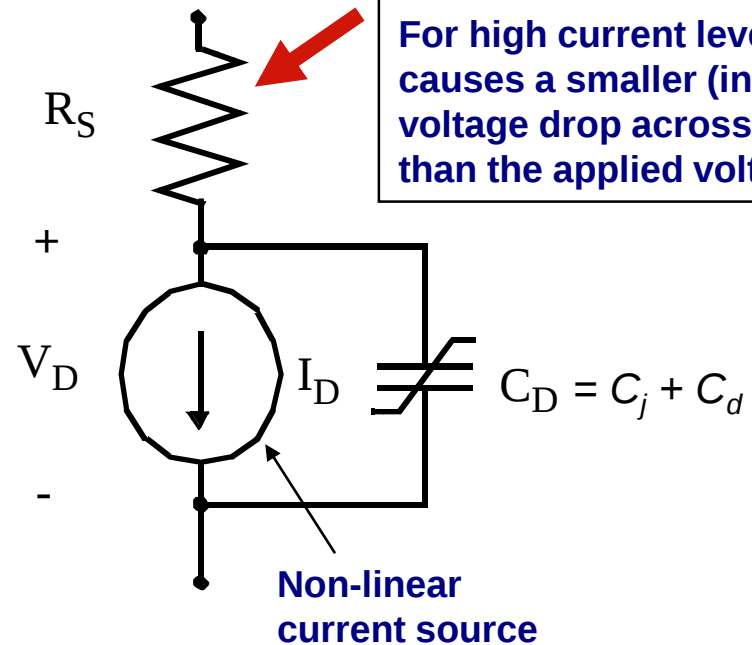
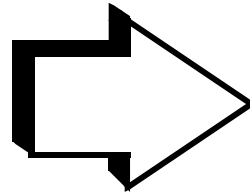
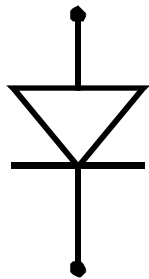
*Strongly non-linear:
prohibits rapid first-
order analysis*



(b) First-order diode model

*A fully conducting diode has a
small range of voltage drop
(between 0.6 – 0.8 V), hence
 V_{Don} can be assumed to be fixed*

SPICE Diode Model



series resistance due to the neutral regions on both sides of the junction

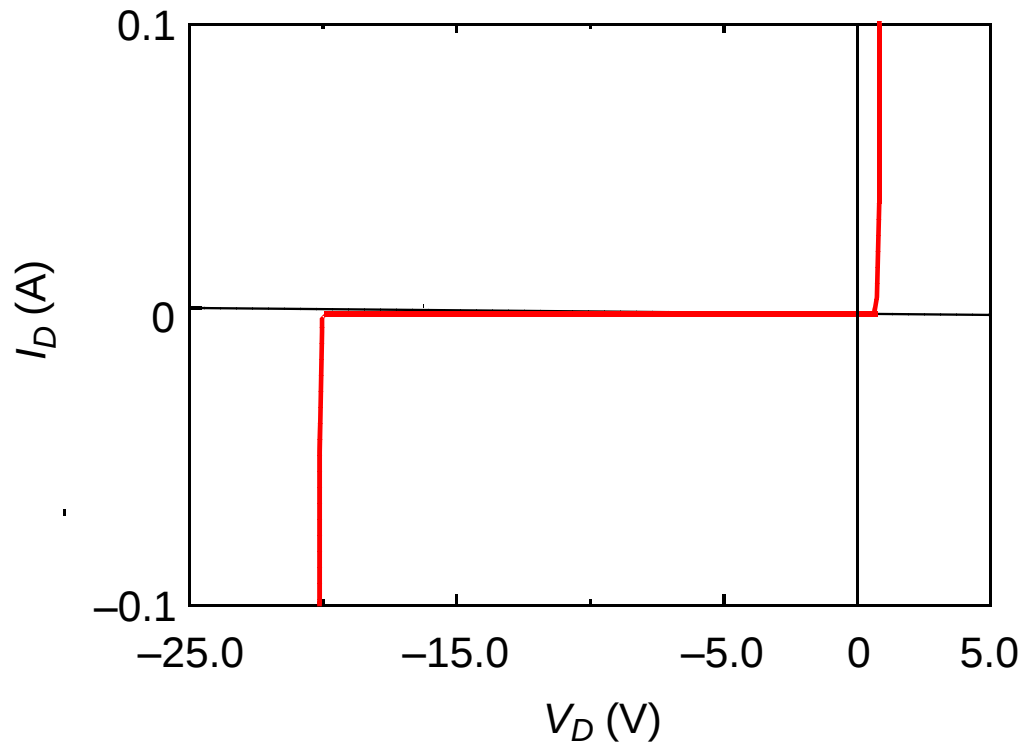
For high current levels, R_S causes a smaller (internal) voltage drop across diode than the applied voltage

$$I_D = I_S \{ \exp[V_D / n\phi_T] - 1 \}$$

See, *The Spice Book* by Vladimirescu, Wiley 1993, for more details...

n is called the emission co-efficient = 1 for most common diodes but can be greater than 1 for others

Secondary Effects



Reverse bias increases electric field across the junction and carriers crossing the junction get accelerated and attain high velocity.

At $E = E_{\text{crit}} = 2 \times 10^5$ V/cm, carriers create e-h pairs on collision with immobile Si atoms.

These carriers in turn create more carriers....

Avalanche Breakdown

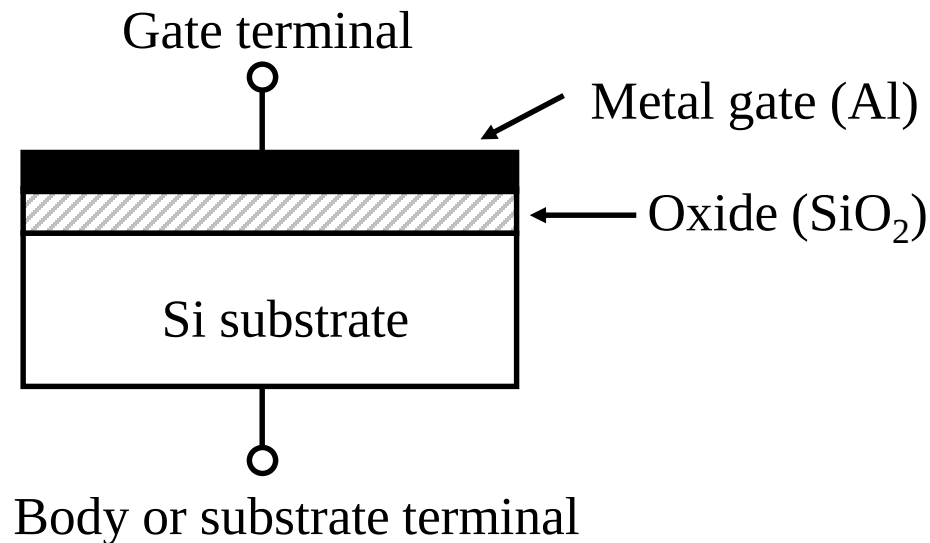
SPICE Parameters

Parameter Name	Symbol	SPICE Name	Units	Default Value
Saturation current	I_S	IS	A	1.0 E-14
Emission coefficient	n	N	-	1
Series resistance	R_S	RS	Ω	0
Transit time	τ_T	TT	sec	0
Zero-bias junction capacitance	C_{j0}	CJ0	F	0
Grading coefficient	m	M	-	0.5
Junction potential	ϕ_0	VJ	V	1

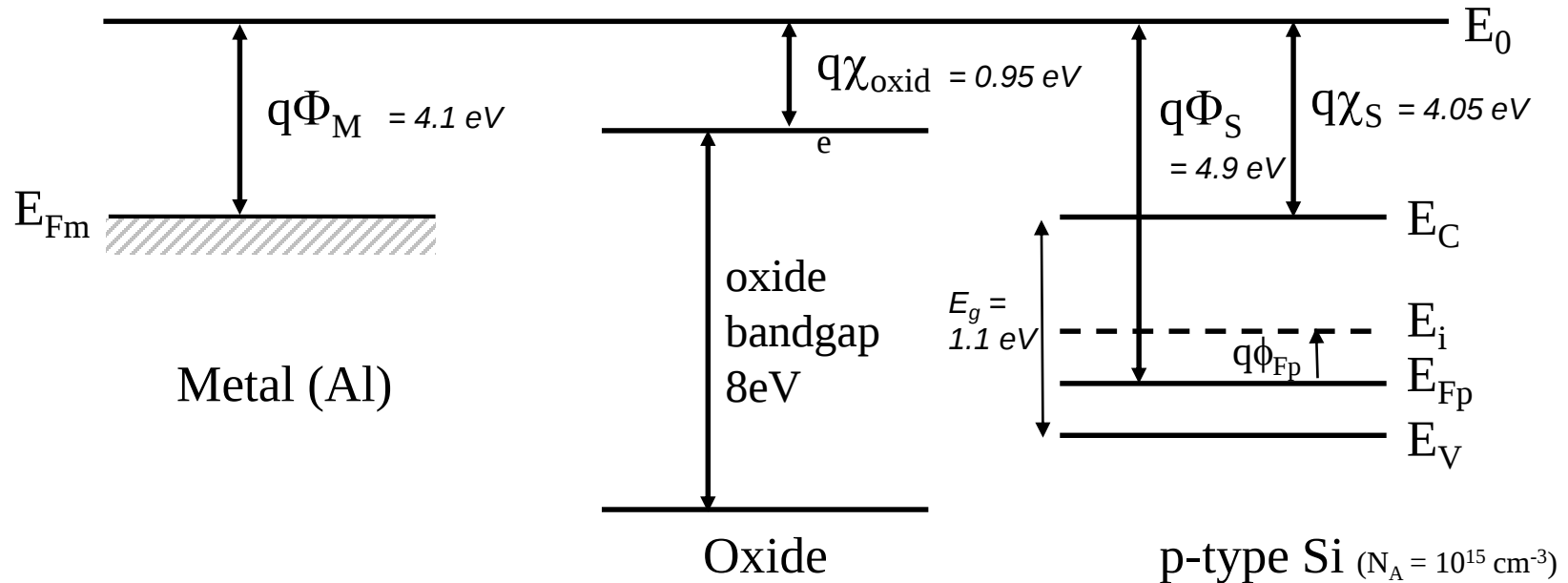
First Order SPICE diode model parameters.

MOS Structure

- MOS: Metal-oxide-semiconductor
 - Gate: metal (or polysilicon)
 - Oxide: silicon dioxide, grown on substrate
- MOS capacitor: two-terminal MOS structure



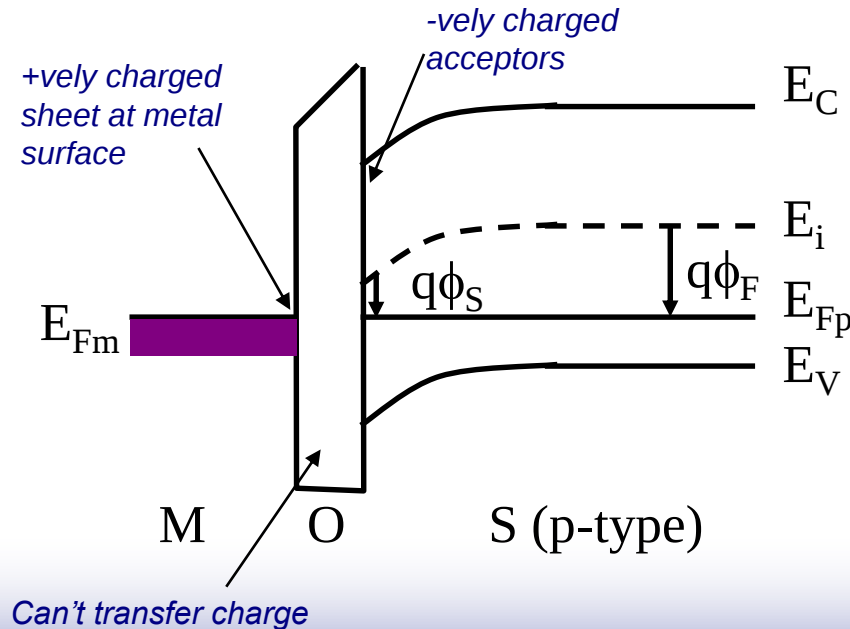
MOS Energy Band Diagram



- **Work function** ($q\Phi_M$, $q\Phi_S$): energy required to take electron from Fermi level to free space
- **Electron affinity** is the potential difference between the conduction band level and vacuum (free-space) level = $q\chi_S$
- **Work function** difference between Al and Si = **0.8 eV**
- **At equilibrium, Fermi levels must line up!!**

MOS Energy Band Diagram

- Bands must bend for Fermi levels to line up
- Amount of bending is equal to work function difference: $q\Phi_M - q\Phi_S$
- Fermi levels equalized by transfer of -ve charge from materials with higher E_F (smaller work functions) across interfaces to materials with lower E_F
- **Part of voltage drop occurs across oxide, rest occurs next to O-S interface**



ϕ_F = Fermi potential
(difference between E_F
and E_i in bulk)

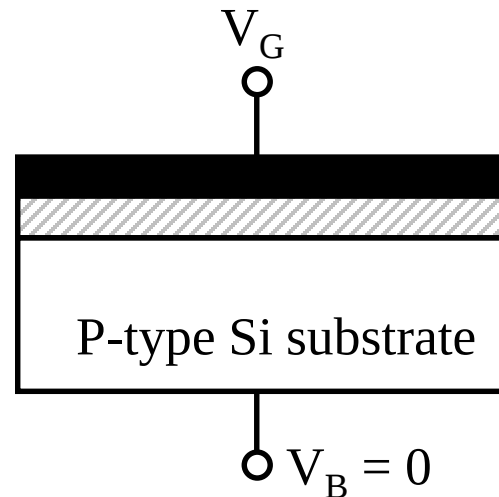
ϕ_S = surface potential

Flat-Band Voltage

- Flat-band voltage
 - Built-in potential of MOS system
 - **Flat Band Voltage:** $V_{FB} = \Phi_m - \Phi_S$
 - Apply this voltage to “flatten” energy bands
 - For the MOS system considered on the previous slide, a –ve voltage applied to the metal w.r.t the Si opposes the built-in voltage on the capacitor and tends to reduce the charge stored on the capacitor plates below its equilibrium value
- Example
 - P-type substrate: $q\phi_{Fp} = 0.2 \text{ eV}$, $q\chi_S = 4.05 \text{ eV}$
 - Aluminum gate ($q\Phi_m = 4.1 \text{ eV}$)
 - What is flatband voltage?

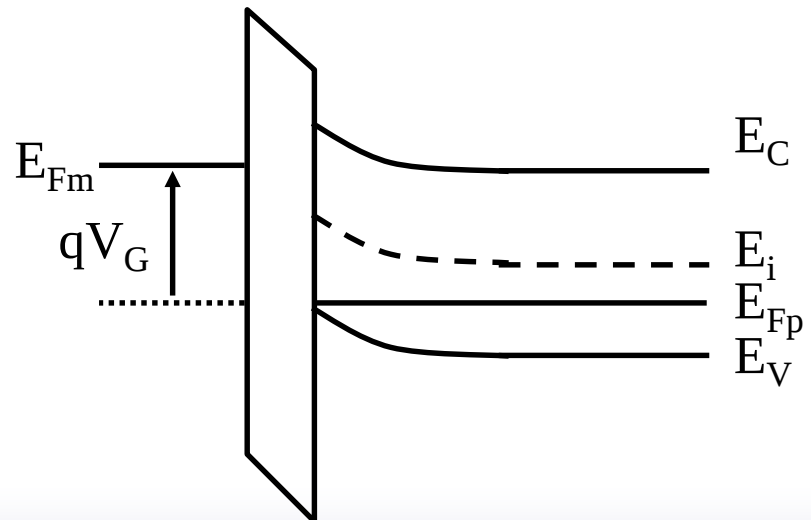
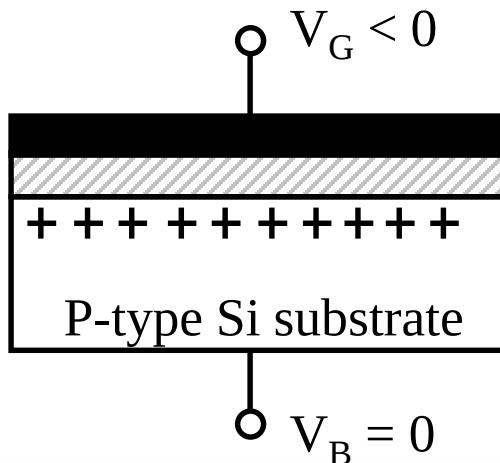
MOS Capacitor Operation

- Assume p-type substrate
- Three regions of operation
 - Accumulation ($V_G < 0$)
 - Depletion ($V_G > 0$ but small)
 - Inversion ($V_G \gg 0$)



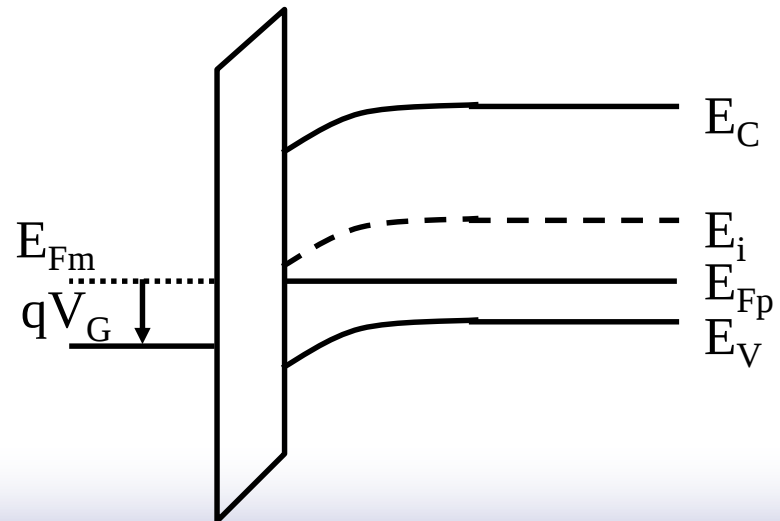
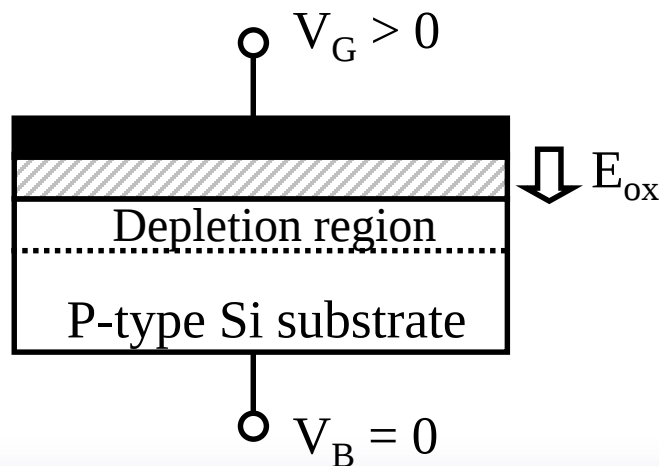
Accumulation

- Negative voltage on gate: attracts holes in substrate towards oxide
- Holes “accumulate” on Si surface (surface is more strongly p-type)
- Electrons pushed deeper into substrate



Depletion

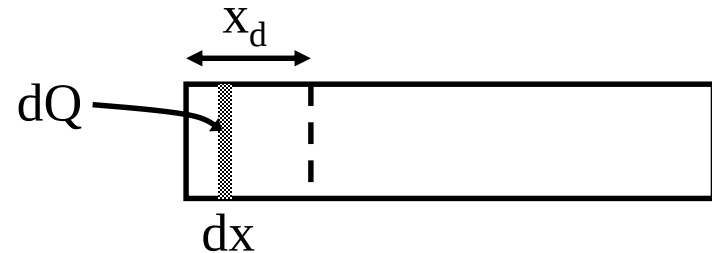
- ❑ Positive voltage on gate: repels holes in substrate
 - Holes leave behind negatively charged acceptor ions
- ❑ Depletion region forms: devoid of carriers
 - Electric field directed from gate to substrate
- ❑ Bands bend downwards near surface
 - Surface becomes less strongly p-type (E_F close to E_i)



Depletion Region Depth

- Calculate thickness x_d of depletion region
 - Find charge dQ in small slice of depletion area

$$dQ = -qN_A dx$$



- Find change in surface potential to displace dQ by distance x_d from the surface (Poisson equation):

$$d\phi = -x \frac{dQ}{\epsilon_{Si}}$$

$$d\phi = xqN_A \frac{dx}{\epsilon_{Si}}$$

Depletion Region Depth (cont.)

- Integrate perpendicular to surface

$$\int_{\phi_F}^{\phi_S} d\phi_S = \int_0^{x_d} \frac{qN_A x}{\epsilon_{Si}} dx$$

$$\phi_S - \phi_F = \frac{qN_A x_d^2}{2\epsilon_{Si}}$$

- Result:

$$x_d = \sqrt{\frac{2\epsilon_{Si} |\phi_S - \phi_F|}{qN_A}}$$

Depletion Region Charge

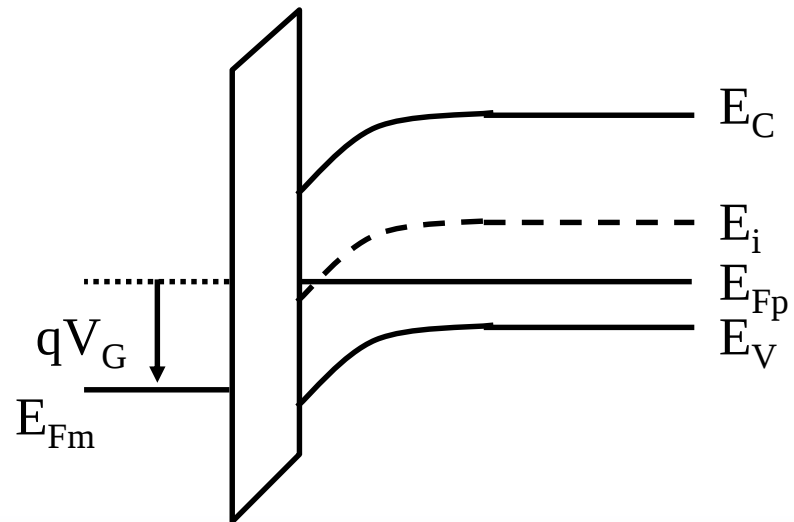
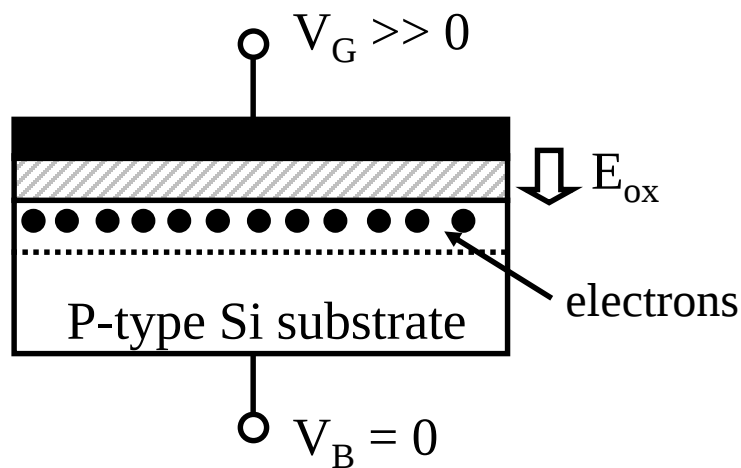
- Depletion region charge density
 - Due only to fixed acceptor ions
 - Charge per unit area

$$Q = -qN_A x_d$$

$$Q = -\sqrt{2qN_A \epsilon_{Si} |\phi_S - \phi_F|}$$

Inversion

- Increase voltage on gate, bands bend more
- Additional minority carriers (electrons) attracted from substrate to surface
 - Forms “inversion layer” of electrons
- Surface becomes n-type

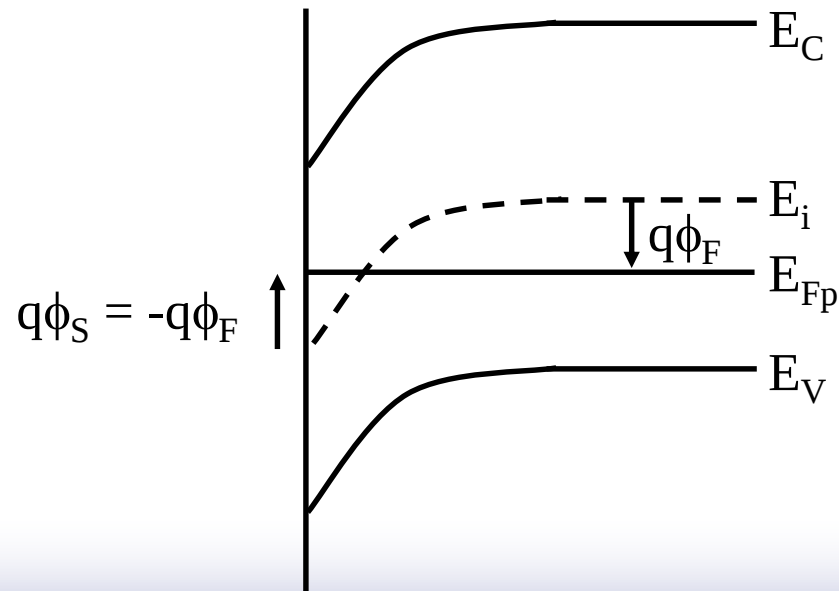


Inversion

- Definition of inversion
 - Point at which density of electrons on surface = density of holes in bulk
 - Surface potential (ϕ_S) is same as ϕ_F , but different sign

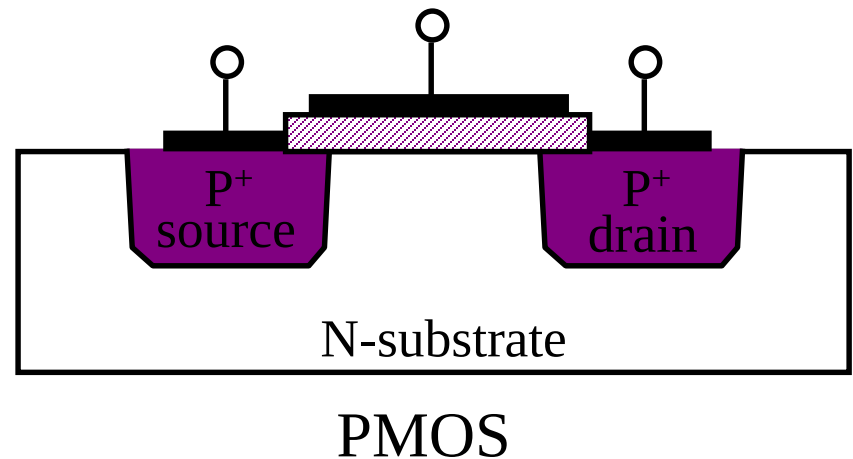
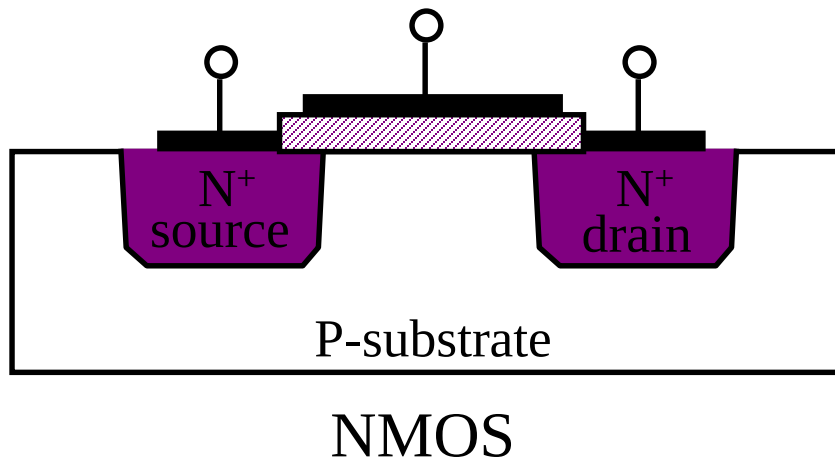
Remember:

$$q\phi_F = E_F - E_i$$



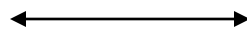
MOS Transistor

- Add “source” and “drain” terminals to MOS capacitor
- Transistor types
 - NMOS: p-type substrate, n^+ source/drain
 - PMOS: n-type substrate, p^+ source/drain

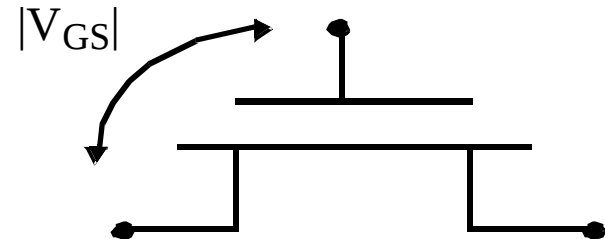
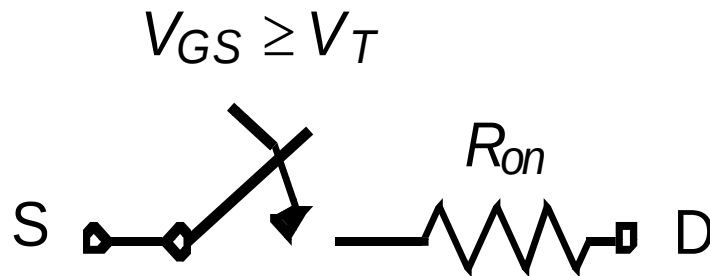


What is a Transistor?

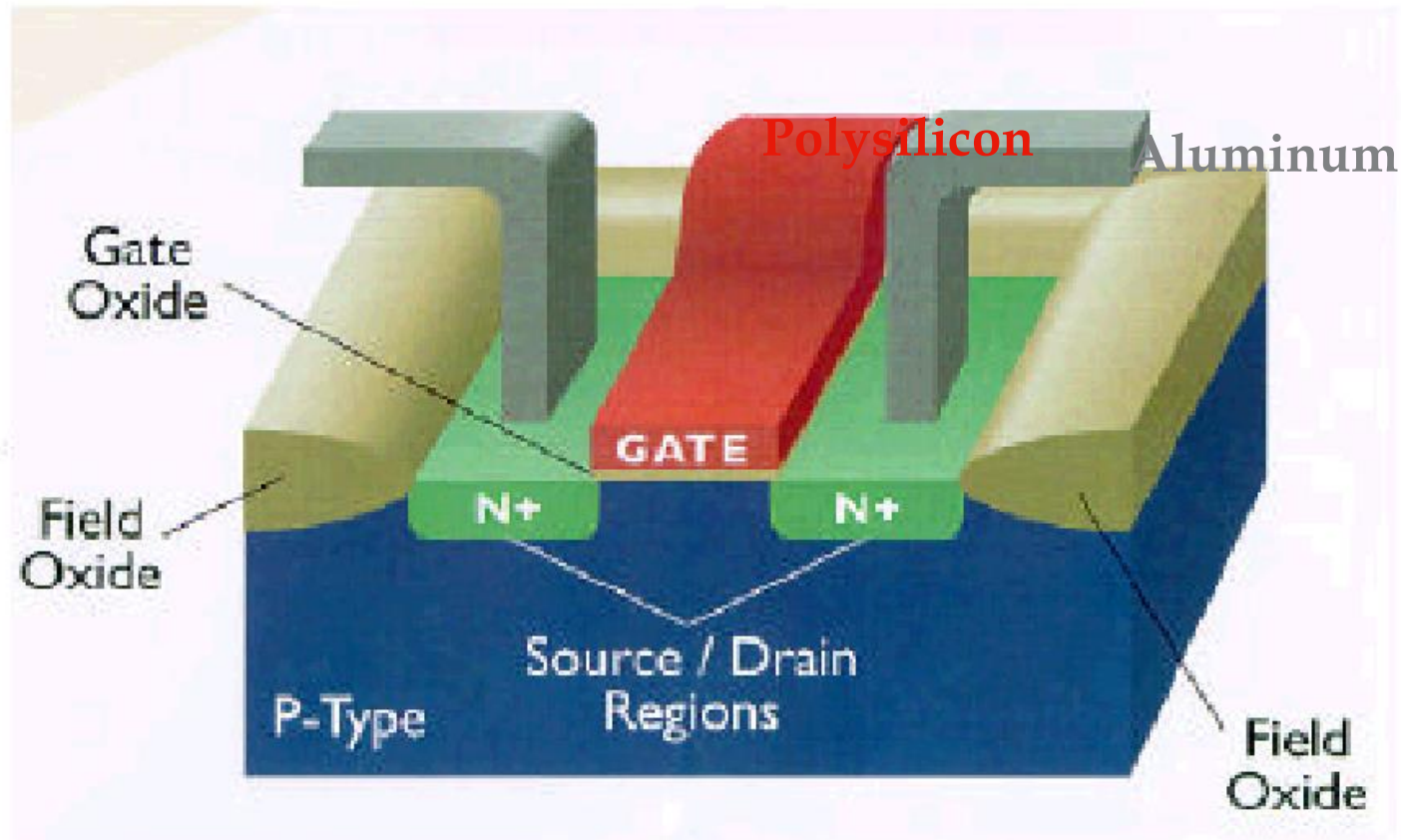
A Switch!



An MOS Transistor

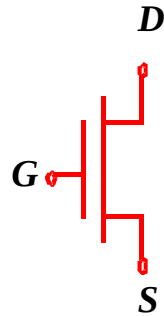


The MOS Transistor

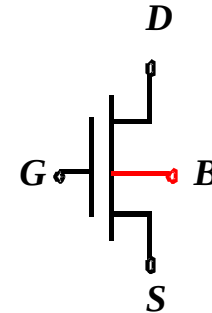
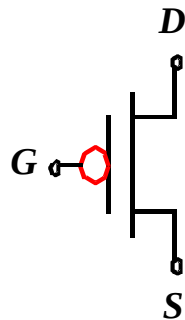


MOS Transistors - Types and Symbols

NMOS



PMOS



NMOS with
Body Contact

For NMOS: Body tied to Gnd

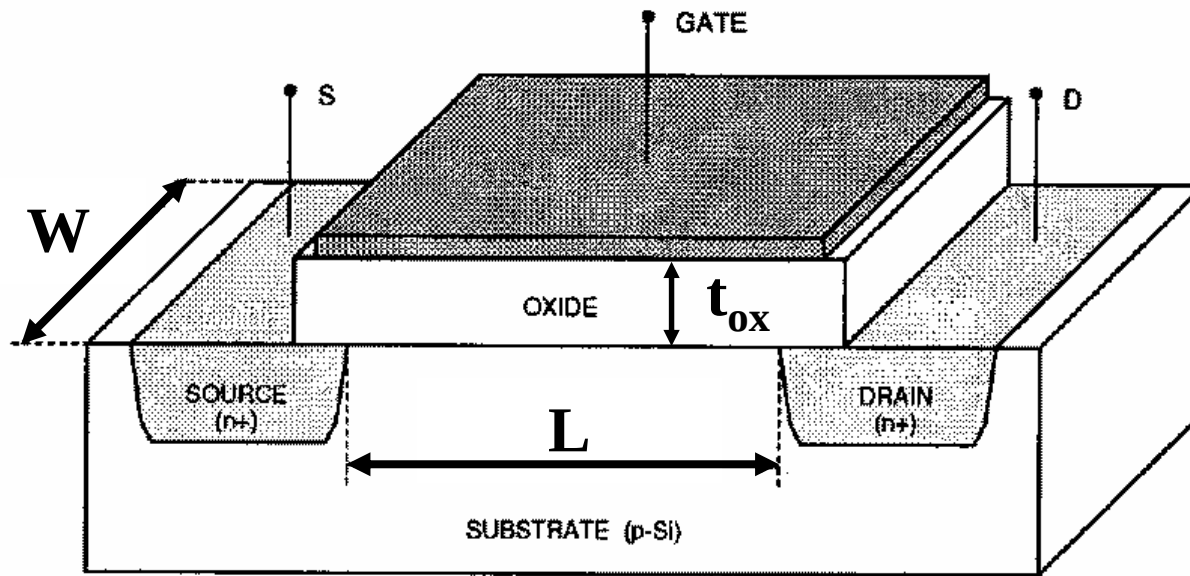
For PMOS: Body tied to Vdd

Why?

MOS Transistor

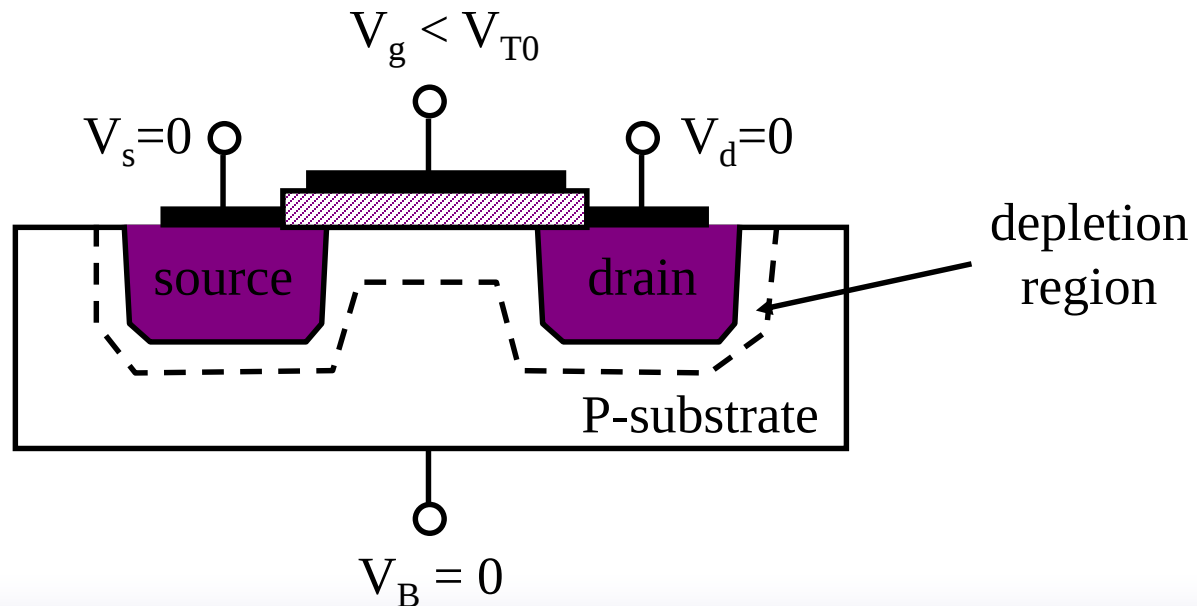
□ Important transistor physical characteristics

- Channel length L
- Channel width W



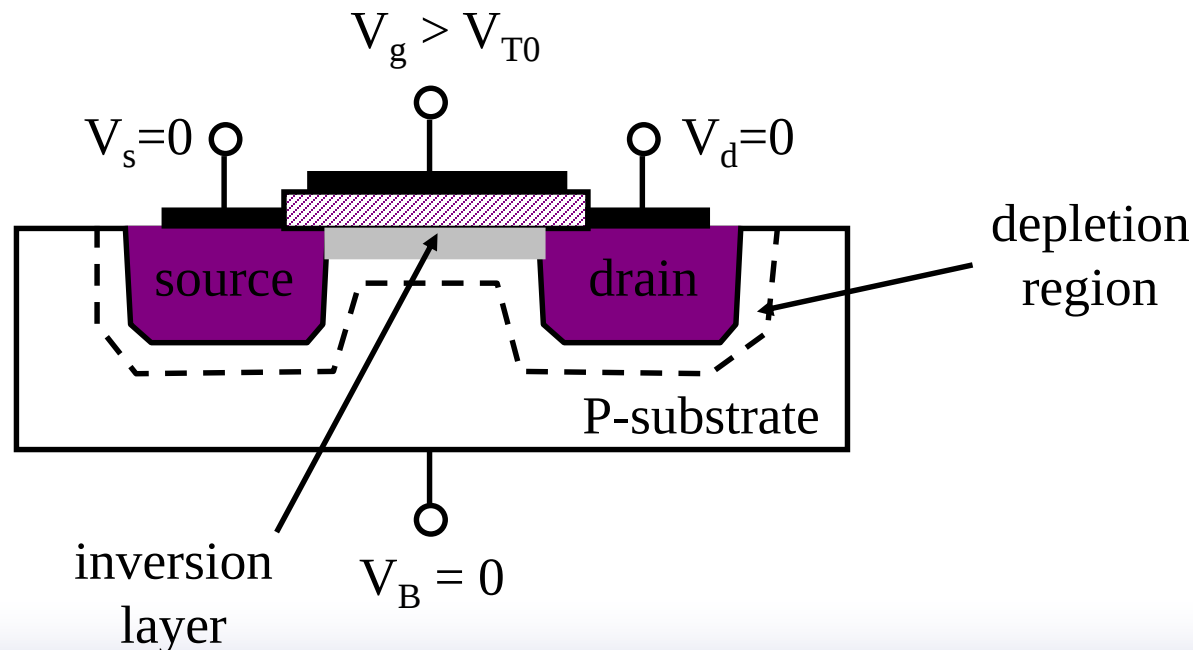
MOS Transistor Operation

- ❑ Simple case: $V_D = V_S = V_B = 0$
 - Operates as MOS capacitor
- ❑ When $V_{GS} < V_{T0}$ (but positive), depletion region forms
 - No carriers in channel to connect S and D
- ❑ V_{T0} is known as the *threshold voltage*

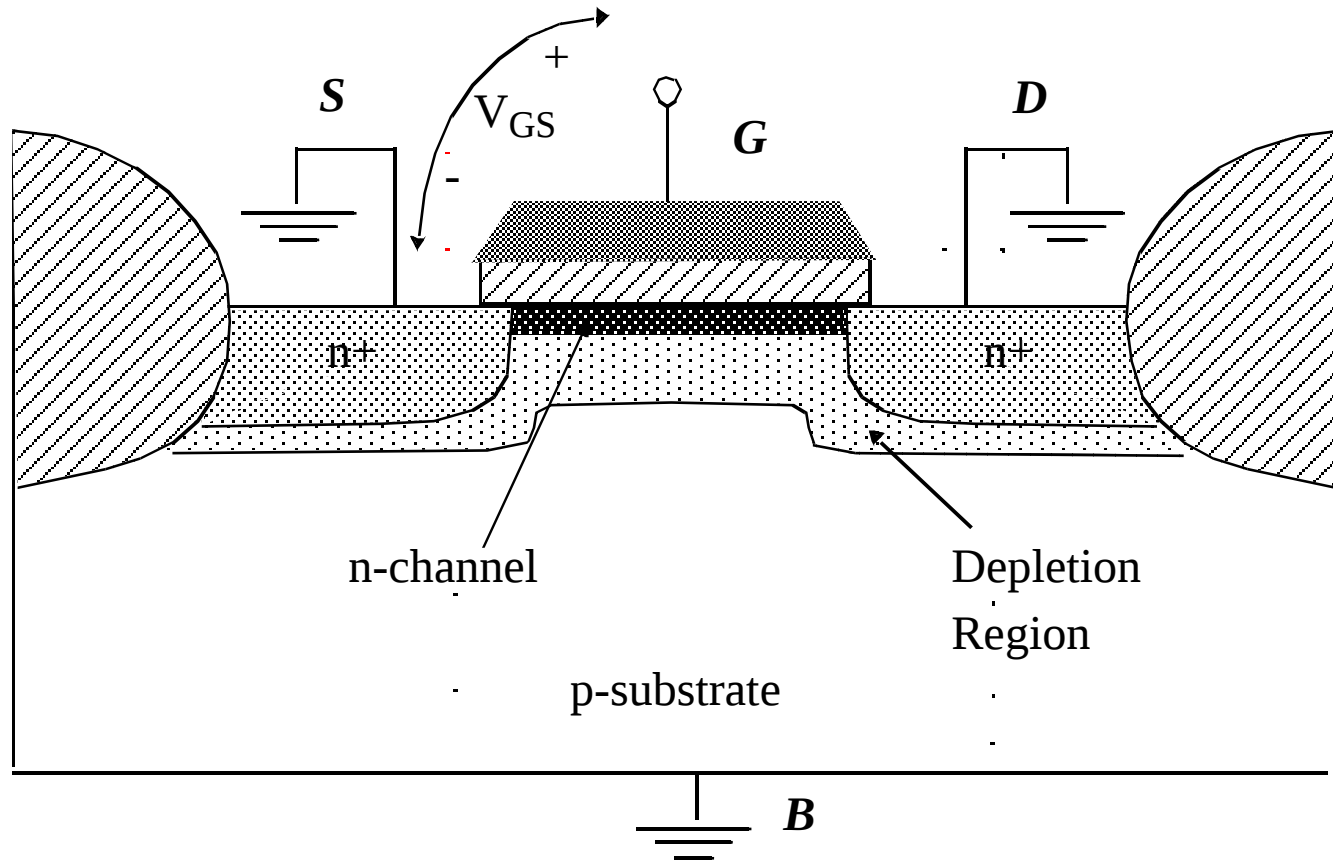


MOS Transistor Operation

- When $V_{GS} > V_{T0}$, inversion layer forms
- Source and drain connected by conducting n-type layer (for NMOS)



Threshold Voltage (V_{T0}): Concept



Note: gate is insulated from the substrate...hence no dc current flows through the oxide...channel is capacitively coupled to the gate through the electric-field in the oxide....that's how it gets the name MOS-FET (field effect transistor)

Physical Parameters that Affect V_{T0}

- ❑ Threshold voltage (V_{T0}): voltage between gate and source required for inversion
 - NMOS Transistor is “off” when $V_{GS} < V_{T0}$
- ❑ Components:
 - Work function difference between gate and channel (Flat-band voltage)
 - Gate voltage to change surface potential
 - Gate voltage to offset depletion region charge
 - Gate voltage to offset fixed charges in gate oxide and in silicon-oxide interface

Threshold voltage (1)

- Work function difference $q\Phi_{GC}$ between gate and channel
 - Represents built-in potential of MOS system
 - For metal gate: $\Phi_{GC} = \Phi_M(\text{metal-gate}) - \Phi_F(\text{substrate}) = \Phi_{ms}$
 - For poly gate: $\Phi_{GC} = \phi_F(\text{poly-Si-gate}) - \phi_F(\text{substrate})$

$$V_{T0} = \Phi_{GC} + \dots$$

Threshold voltage (2)

- First component accounts for built-in voltage drop
- Now apply additional gate voltage to achieve inversion: change surface potential by $-2\phi_F$ (note that ϕ_F is negative for p-type substrate)

$$V_{T0} = \Phi_{GC} - 2\phi_F + \dots$$

Threshold voltage (3)

- Offset depletion region charge, due to fixed acceptor ions
- Calculate charge at inversion ($\phi_S = -\phi_F$)

- From before: $Q = -\sqrt{2qN_A\epsilon_{Si}|\phi_S - \phi_F|}$

- So: $Q_{B0} = -\sqrt{2qN_A\epsilon_{Si}|-2\phi_F|}$

Depletion charge is negative....why? (acceptor ions after accepting electrons are -ve)

- For non-zero substrate bias ($V_{SB} \neq 0$):

$$Q_B = -\sqrt{2qN_A\epsilon_{Si}|-2\phi_F + V_{SB}|}$$

- Due to larger depletion region

Threshold voltage (3, cont.)

- To offset this charge, need voltage $-Q_B/C_{ox}$
- C_{ox} = gate capacitance per unit area
 - $C_{ox} = \epsilon_{ox}/t_{ox}$
 - t_{ox} = thickness of gate oxide (normally in Å)

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_B}{C_{ox}} + \dots$$

Threshold voltage (4)

- Finally, correct for non-ideal fixed charges
 - Fixed positive charged ions at boundary between oxide and substrate. Density = N_{ox}
 - Due to impurities, lattice imperfections at interface
 - Positive charge density $Q_{ox} = qN_{ox}$
 - Correct with gate voltage = $-Q_{ox}/C_{ox}$
- Final threshold voltage formula (for NMOS):

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

Threshold voltage, summary

- If $V_{SB} = 0$ (no substrate bias):

$$V_{T0} = \Phi_{GC} - 2\phi_F - \frac{Q_{B0}}{C_{ox}} - \frac{Q_{ox}}{C_{ox}}$$

- If $V_{SB} \neq 0$ (non-zero substrate bias)

$$V_T = V_{T0} + \gamma \left(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|} \right) \quad \text{For uniform body doping....}$$

- Body effect (substrate-bias) coefficient:

$$\gamma = \frac{\sqrt{2qN_A\epsilon_{Si}}}{C_{ox}} \quad \begin{array}{l} + \text{ for NMOS} \\ - \text{ for PMOS} \end{array}$$

For modern FETs with retrograde doping, V_T varies ~linearly with V_{SB}

- Threshold voltage increases as V_{SB} increases!
(easy to explain with a band diagram....)