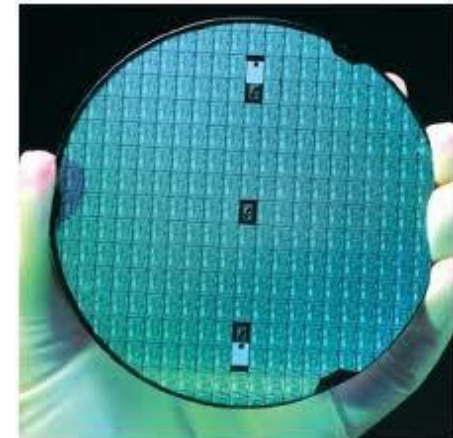
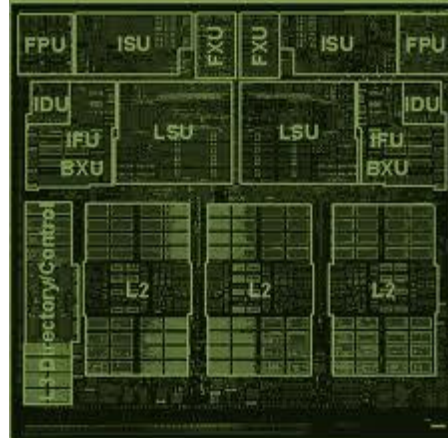
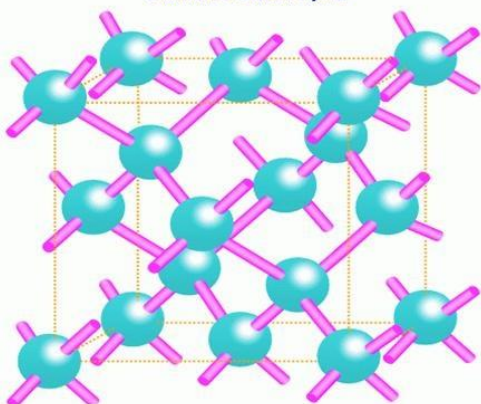


Structure of silicon crystal



ECE 122A

VLSI Principles

Lecture 1

Prof. Kaustav Banerjee
Electrical and Computer Engineering
University of California, Santa Barbara
E-mail: kaustav@ece.ucsb.edu

Why VLSI?

□ Difficult to imagine life without **integrated circuits**....

□ Applications in:

- AI
- Consumer Electronics
- Computing
- Communication
- Medical/Health
- Entertainment
- Energy
- Aerospace
- Automobile
- Military



Electronics inside a BMW...

http://www.bmw.com/com/en/insights/technology/technology_guide/articles/digital_motor_electronics.html

Digital Motor Electronics (DME).

The comprehensive management system for your engine: Digital Motor Electronics (DME) **controls all key aspects of the engine's operation**, ensuring optimum reliability, maximum performance and the lowest possible fuel consumption and emissions.

By managing key engine functions, Digital Motor Electronics (DME) **guarantees optimum reliability, maximum performance and the lowest possible fuel consumption and emissions**. Its sensors continually all factors affecting the operation of the engine. The data is then evaluated by a microprocessor and translated into commands for the fuel injection and ignition systems.

The DME system **receives up to 1,000 separate items of data input per second**, including engine speed, air intake volume, air temperature and density, coolant temperature, throttle position, accelerator position and vehicle speed.

DME verifies all incoming data by comparing it with the reaction of the rest of the system. If a defective sensor delivers unrealistic data, DME replaces this with preset standard values. If a spark plug fails, DME immediately cuts fuel flow to this cylinder in order to prevent engine damage.

DME **looks after the electrical power system too, with sensors measuring the charge and condition of the battery as well as current electrical power consumption**. By maintaining optimum battery charge levels and thus avoiding flat batteries, it prevents damage to the battery and guarantees maximum battery life, thereby helping to ensure the engine always starts readily.

BMW introduced the world's first Digital Motor Electronics system in the BMW 732i in 1979.



BMW Z4 Roadster



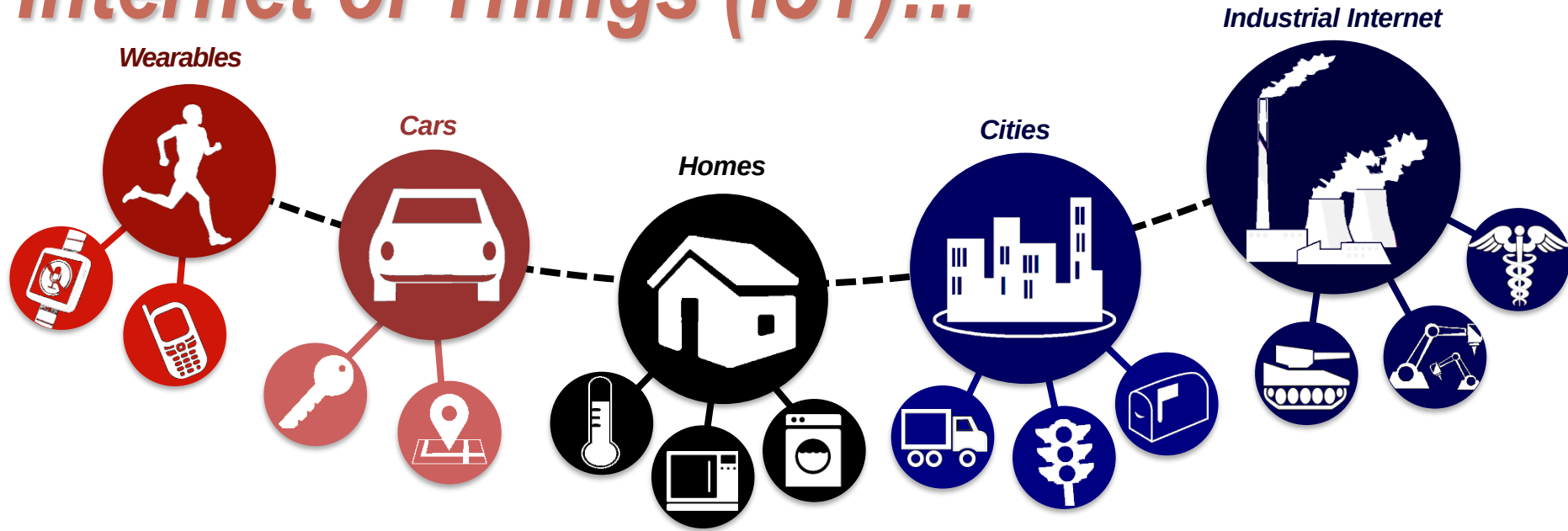
VLSI inside...

Hard drive of a PC



Digital Mobile Phones

Internet of Things (IoT)...



- 1990s' fixed Internet wave connected 1 billion users
- 2000s' mobile wave connected another 2 billion
- The IoT has the potential to connect 28 billion “things” by 2020
— **The third wave of Internet development**

Bottom Line:

To enable IoT - need low power sensors and ICs....

What is VLSI?

- ❑ Very Large Scale Integrated ~~Circuits~~ Systems
- ❑ **Very-large-scale integration (VLSI)** is the process of creating *integrated systems* by combining *billions* of transistors into a single chip.

1971: Intel 4004

**2300 Transistors...with CPU, memory
and input/output controls**



2008: Intel® Xeon® Processor MP X7460--**1.9 Billion Transistors!!!**

For details on Intel Microprocessors:

<http://www.intel.com/pressroom/kits/quickreffam.htm>

Amazing Transistor Scaling....

- *If transistors were people*



2300
Average Music Hall
capacity



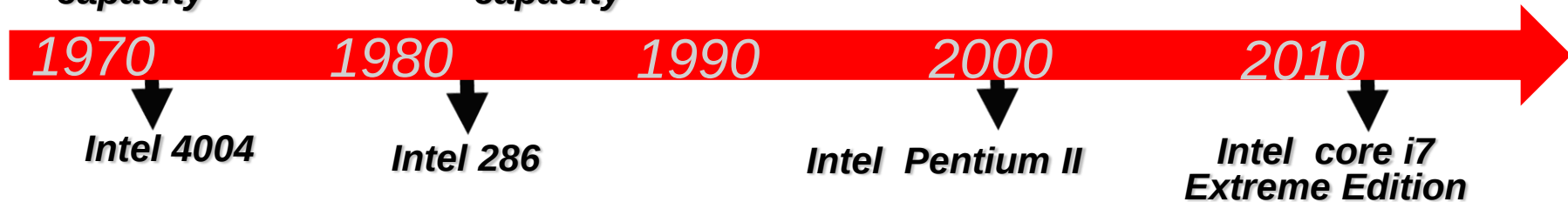
134000
Large stadium
capacity



32 Million
Population of Tokyo



1.3 Billion
Population of China



Now imagine 1.3 Billion people in the original music hall!!!!

Why Scaling?

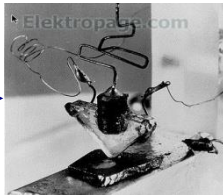
- Higher number of devices in chip
- Faster operation
- More functionality and lower cost

Scaling Challenges

- Higher power consumption
- Severe short-channel effects
- Higher leakage

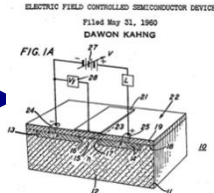
History...

First point contact Transistor,
Shockley, Brattain, Bardeen
Bell Labs



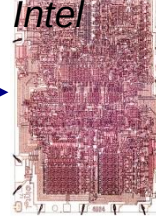
1959

First FET, Kahng
Bell Labs



1964

First Microprocessor,
Intel

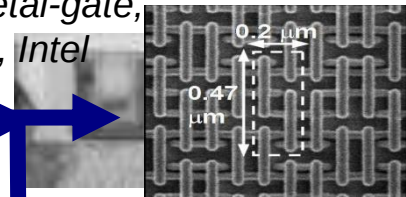


1998

First FinFET,
C. Hu, Berkeley



High-k Metal-gate,
32nm, Intel



2007

2011

FinFET SRAM

1948

1960

1970

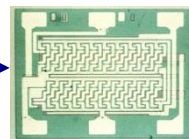
1999

2009

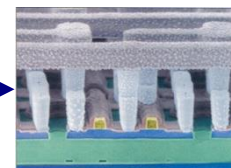
2015



First IC,
Jack Kilby, TI
Robert Noyce,
Fairchild

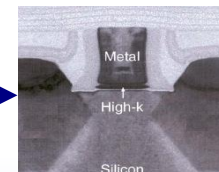
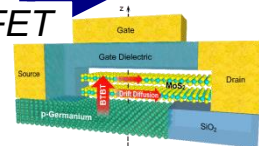


First MOS IC,
Robert Norman



First SOI IC,
IBM

First 2D-TFET
UCSB



High-k Metal-gate,
45 nm, Intel

2011: 3D Transistor



Introducing the world's first 3-D transistors ready for high volume manufacturing

ARCHITECTURE AND SILICON

- Microarchitecture
- Silicon Technology

PRODUCTS TECHNOLOGIES

MANUFACTURING

RESEARCH

STANDARDS

SECURITY

Unprecedented Combination of Performance and Energy Efficiency

Unprecedented Combination of Performance and Energy Efficiency

22nm EXPLAINED

Watch Mark T. Bohr Intel Senior Fellow explain 22nm >

INTRODUCING THE WORLD'S FIRST 3-D TRANSISTOR READY FOR HIGH-VOLUME MANUFACTURING

3-D, 22nm: New Technology Delivers An Unprecedented Combination of Performance and Power Efficiency

Intel is introducing a new 3-D transistor technology for future microprocessor families: 3-D transistors manufactured at 22nm. These new transistors enable Intel to continue to relentlessly pursue Moore's Law and to ensure that the pace of

QUICK LINKS

- 32nm
- Silicon Technology
- Intel Microarchitecture code-name Sandy Bridge

ElectronicsWeekly.com

Other Companies may join Intel with 22 nm FinFET, says IMEC chief.

Salary Survey 2011

ElectronicsWeekly.com

JONATHAN LEE RECRUITMENT

Take part in our Salary Survey and help nature nurture salary levels

Other companies may join Intel with 22nm Finfets, says Imec chief.

David Manners
Monday 23 May 2011 19:26

Other companies besides Intel may adopt Finfet at the 22nm generation of process technology, according to Luc van den Hove, President of Imec, Europe's foremost microelectronics research establishment.

"Some companies may adopt Finfet at the second generation of 22nm," van den Hove told EW in Brussels today.

Share the content

Related Jobs

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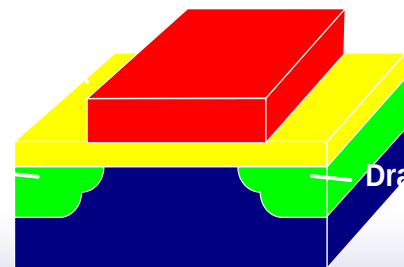
Most Viewed

Li-Fi flickers to challenge Wi-Fi
Posted: 10:11 29 Jul 2011

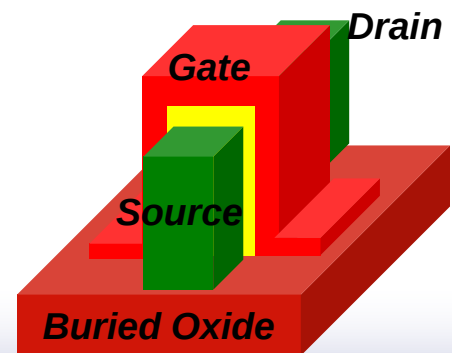
TSMC to ramp 14nm finfets in

Resources

Senior Verification Engineer/ Lead - Semiconductors - Germany - JB5383 Europe/Germany Eneg

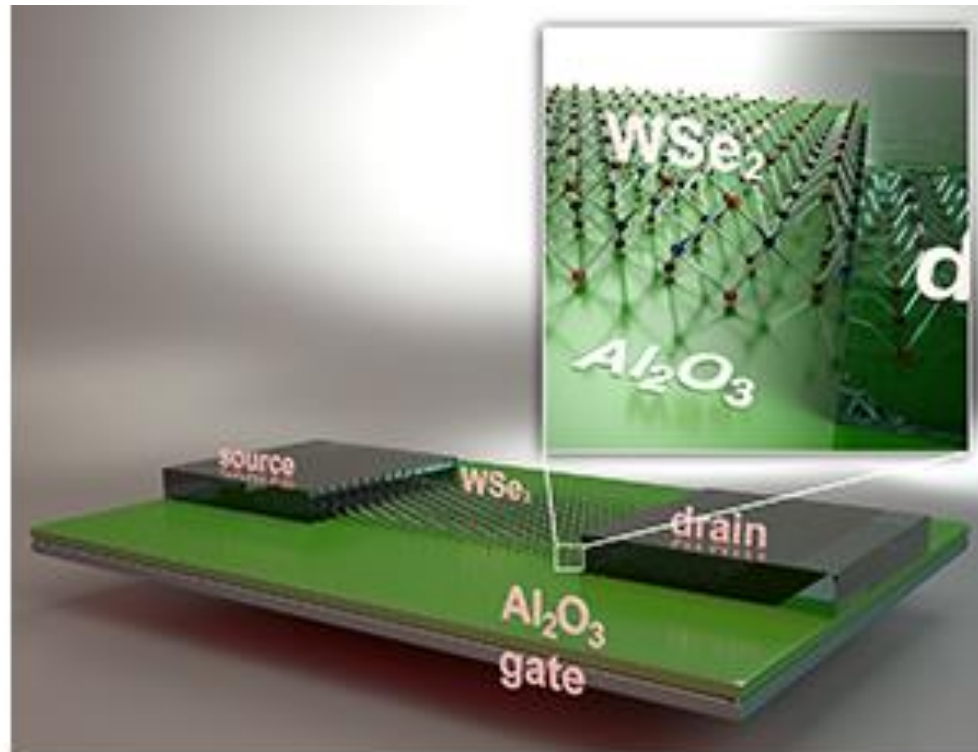


Planar MOSFET



FinFET

2013: Ultimate Thin-body Transistors (first monolayer n -type WSe_2 FET)



Schematic view of a back-gated field effect transistor fabricated by UCSB researchers using monolayer tungsten diselenide (WSe_2) channel material. Credit: Peter Allen, UCSB

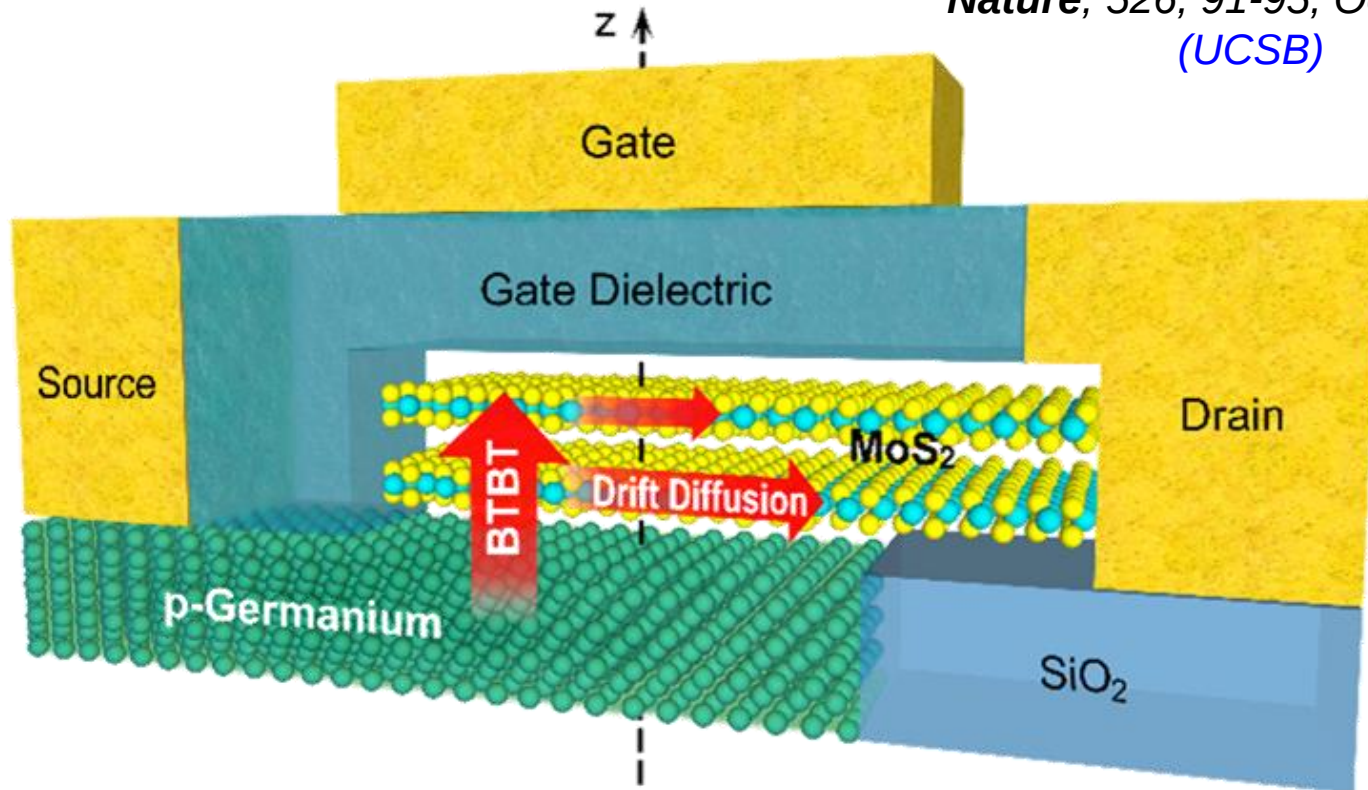
Read more:

<https://www.sciencedaily.com/releases/2013/06/130621095713.htm>

10

2D-TFET: A fundamentally different transistor

Nature, 526, 91-95, Oct 1, 2015
(UCSB)



**World's Thinnest Channel Transistor with
Subthermionic SS!!**

Read More: Flat transistor defies the limit.... can potentially reduce chip power by ~90%!!

2018: Kinetic Inductor Invented!

Nature Electronics 1, 46-51, 2018
(UCSB)



The Last Barrier To Ultra-Miniaturized Electronics Is Broken, Thanks To A New Type Of InductorForbes, March 8, 2018

Highest inductance-density materials ever made....

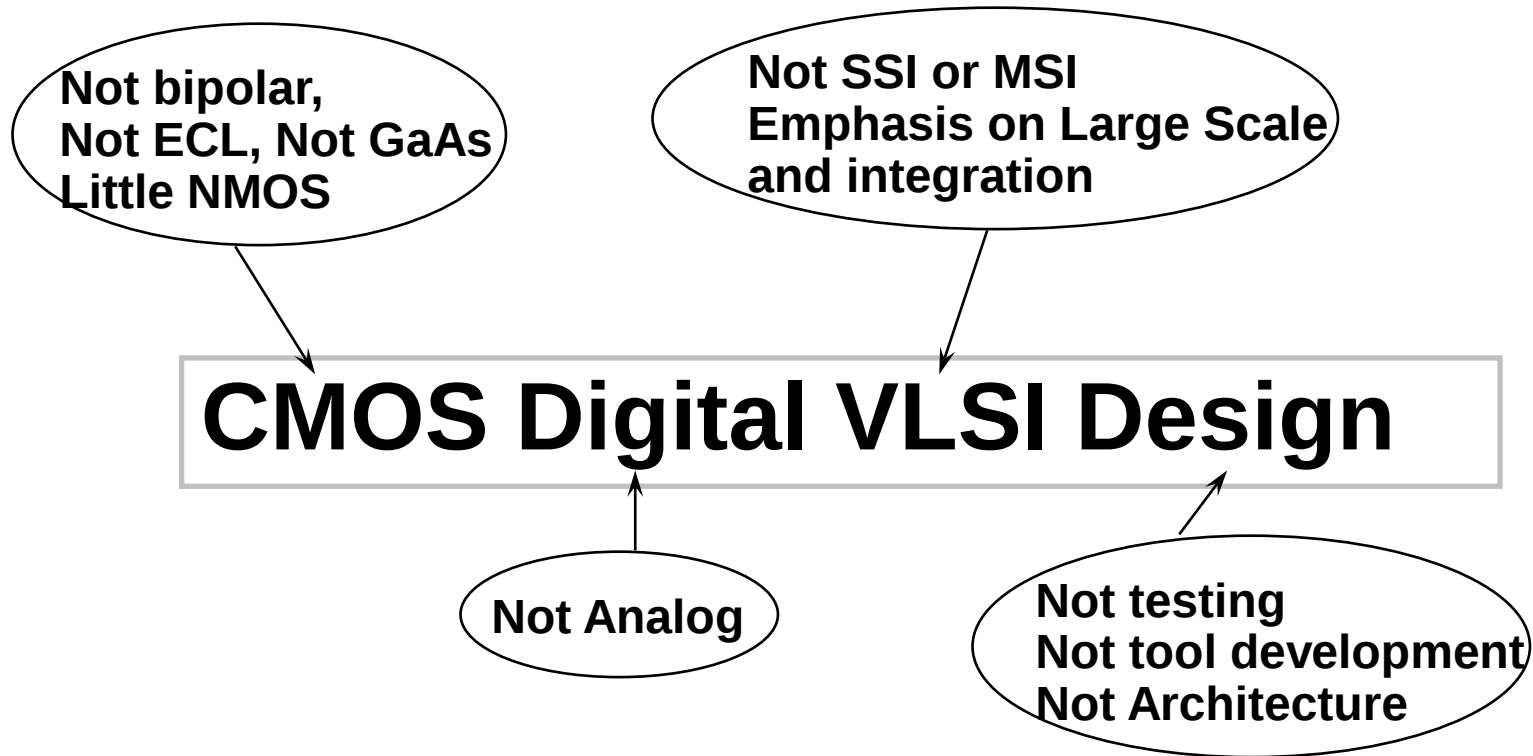
Inductor design not limited by laws of electromagnetic induction anymore!!!

<https://www.forbes.com/sites/startswithabang/2018/03/08/breakthrough-in-miniaturized-inductors-to-revolutionize-electronics/#13c4e515779e>

Who should be taking this course?

- Those interested in pursuing a career in *nanoelectronics, neuromorphic/quantum computing, bioelectronics etc*: transistor design, circuit design, or computer-aided design
- Those interested in exploring “*emerging devices and technology*” driven circuit/system design
- Those interested in passing the *ECE PhD Screening Exam* in the VLSI & CMOS Design Area
- Those interested in finding a *lucrative position in the semiconductor industry* as an IC device/design/technology engineer
 - ❖ *In the past, students recruited by Apple, Intel, Google, AMD, IBM, TI, SanDisk, nVidia, Marvel, Global Foundries, Maxim, Micron Technology, Qualcomm, Mentor Graphics, and other IC companies have found the course invaluable...*

About this course.....



What to expect out of the course...

❑ **The course is:**

- To learn **transistor level design** of logic gates, components
- to learn **practical aspects** of design including design trade-offs

❑ **The course is not:**

- A tutorial to build expertise in CAD tools, or
- A forum to demonstrate architecture skills, or
- A test of your logic design expertise, or
- An exercise to design a microprocessor.

❑ **Course time is short: < 20 classes**

- A **lot of self-study** is expected
- Homeworks could be time consuming—but key component of this course – not simply a follow up of the lectures!
- Project is a major commitment and calls for a lot of hard work!

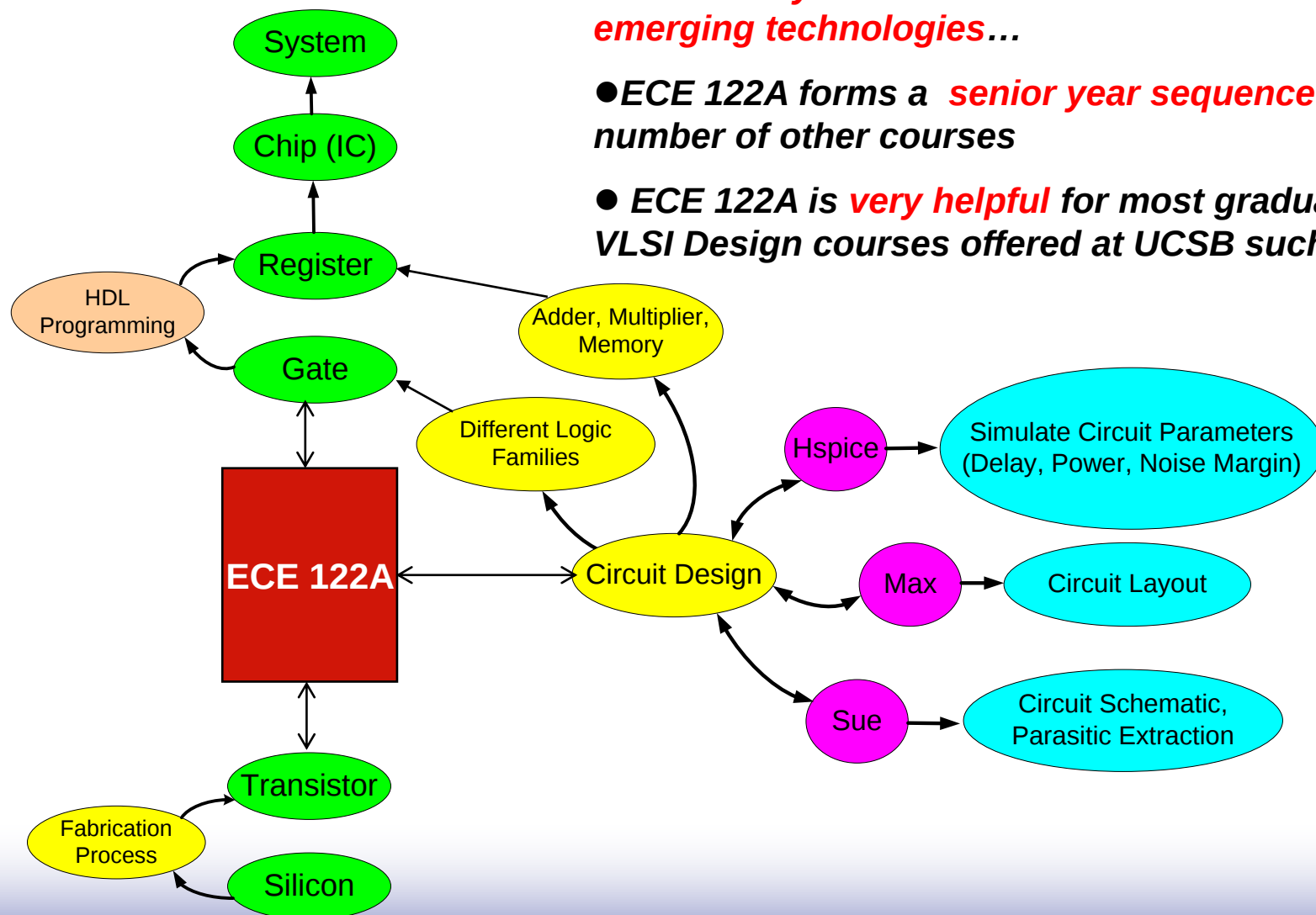
❑ **This is not a class just to improve your GPA!**

Why take this course?

- This is what you will need to do anything meaningful in **circuits/systems** research as well as to explore **emerging technologies**...

- ECE 122A forms a **senior year sequence** with a number of other courses

- ECE 122A is **very helpful** for most graduate level VLSI Design courses offered at UCSB such as **ECE 225**



What are we going to cover?

- ❑ **Introduction to digital integrated circuits.**
 - **CMOS devices** and manufacturing technology. CMOS inverters, **gates** and **interconnects**. **Circuit characterization**: delay, noise margins, and power dissipation. **Combinational** and **sequential** circuits. **Arithmetic operations** and **memories**
- ❑ **What will you learn?**
 - **Understanding, designing, and optimizing digital circuits** with respect to different quality metrics: area, speed, power dissipation, and reliability using analytical methods and circuit simulation
 - **Practical aspects of IC design**: impact of manufacturing variations (device level variations) on circuit level metrics, effect of device and interconnect parasitics on circuit performance
 - **Learn to use various IC design tools**: Layout, Extraction, Circuit simulation

Textbook and References

❑ Textbook

- *CMOS VLSI Design: A Circuits and Systems Perspective*
(Fourth Edition, 2011)
 - by Neil H. E. Weste and David Harris
 - Addison Wesley Publishing Company

❑ Supplementary Text:

- *Modern Semiconductor Devices for ICs*
(First Edition, 2010)
 - by Chenming Hu
 - Prentice Hall Publishing Company

❑ Lecture Notes: Combination of slides + discussion

- Only slides will be posted on the class web page

❑ Reference Materials and Recommended Reading

- Will be posted on the class web site:

Class Home Page:

https://web.ece.ucsb.edu/courses/ECE122/122_F22Banerjee/

Prerequisites

- ❑ Logic Design (ECE 152A or equivalent)
- ❑ Combinational and clocked logic, gates, latches, flip-flops, etc.
 - Logic reduction: K-maps
 - ❑ Fundamentals of EE
 - ❑ Resistance, capacitance, inductance, power/energy
- ❑ Circuit Analysis (both analytical and simulation based)
 - ❑ at the level of ECE 10-ABC
- ❑ Semiconductor and Device Physics (basics will be covered in this course)
 - ❑ Energy band diagrams, p/n junctions, MOS transistors

....Most important prerequisite is your desire to learn and excel!!

Homework, Exams, Grading (1)

- ❑ **Homeworks:** will be posted on the class home page
 - Weekly HW/Lab assignments
 - Late homework will be penalized (20% per day), submission (beyond the second day) will get ZERO grade
 - Solutions will be Posted on the class web site a week after the due date
 - Homework assignments require Lab work
 - All Labs MUST be completed for passing
 - **Will count towards 20% of the final grades**
- ❑ **Exams**
 - Midterm Exam: **Will count towards 20% of the final grades**
 - FINAL Exam: **Will count towards 40% of the final grades**
- ❑ **Final Project:** must complete to pass
 - Will be posted on class home page
 - **Will count towards 20% of the final grades**
- ❑ **No “make-up” homework, exams, labs**

Homework, Exams, Grading (2)

❑ Project

- You may work as part of a team (not more than 2), yet graded individually
 - Your grade = Performance in Final Lab Exam + project report
- The project report MUST summarize the contribution of both students

❑ Final grades

- Distribution of grades depends on class performance
- Standard grading techniques will be applied (histograms, curves)-
-- same criteria for all students
 - ❑ *No incomplete grade (no exceptions)*

Preparation for the course

- ❑ Computing environment and tools
 - Setup computer account, and the compute environment
 - Familiarize with the schematic and layout editors (**SUE, MAX**)
 - Familiarize with extractor (**CALIBER-Mentor Graphics**)
 - Familiarize with the circuit simulator (**HSPICE**)
 - **Tutorials** on these tools are posted on the class web page
- ❑ Theory
 - Review logic design (ECE 152A)
 - Review basic device physics (I will provide some tutorial material to help you)
- ❑ Project
 - You may start formalizing your project team

A few hints

- ❑ Discussion & Lab: Tuesdays 8:00-10:50AM - PLEASE ATTEND!!
 - First half to be used for **problem solving** – to help with the homeworks
 - Second half will focus on the **labs/project**
- ❑ Homework
 - **Most important** part of the course....
 - Spend most of the time thinking, planning, and exploring on your own
 - Discussions are encouraged but **refrain from extracting the answers** from the TAs or other students
 - Show your work on the homework! **Thought process is more important than final answer** → partial credit given
 - Use simulators for verification of your design
- ❑ Difficult to take notes?
 - Note down important points, not essays...all slides will be posted
 - Read topics from your favorite book BEFORE and AFTER the class
- ❑ Actively participate in the class discussion
 - Don't be afraid if you are wrong
- ❑ Question everything, even the books!

Class Calendar

Lectures	Homework	Covered Topics	Lab & Project	
09/22 Lecture 1	Homework 1 (9/23) Digital Design Review Due 10/3	Boolean Algebra Combinational Circuit Sequential Circuit Moore’s Law	Lab 1 Environment Setup and Practice 9/27 Due 10/6	
09/ 27 Lecture 2				
09/ 29 Lecture 3				
10/ 04 Lecture 4	VLSI Processing Video I & II Homework 2 (10/03) CMOS and Pass Transistors Due 10/11	CMOS Implement Pass Transistor Transmission Gate Multiplexer Finite-State-Machine Euler Path	Lab 2 HSpice, CMOS Sizing 10/04 Due 10/13	
10/06 Lecture 5				
10/11 Lecture 5 (cont’d)				
10/13 Lecture 6	Homework 3 (10/11) Semiconductor Physics Due 10/18	Carrier Statistics Current in Semiconductor PN Junction MOS Capacitor	Lab 3 Static CMOS 10/11 Due 10/20	
10/18 Lecture 7				
10/20 Lecture 8	Homework 4 (10/18) MOSFET Due 10/25	Threshold Voltage Body Bias Current Saturation Device Parasitics Adders/Multipliers	Lab 4 Inverter 10/18 Due 10/27	
10/ 25 Lecture 9				
10/27 Lecture 10	Homework 5 (10/25) Inverter, CMOS Sizing, Interconnect, CMOS Inverter Due 11/1	CMOS Inverter Logical Effort Interconnect - RLC Elmore Delay	Final Project Starts from 11/04	
11/ 01 Lecture 11				
11/03 Midterm				
11/08 Lecture 12				
11/10 Lecture 13	Homework 6 (11/04) Logic Design Styles Due 11/11	Ratioed Logic Pass Transistor Logic Dynamic Logic		
11/15 Lecture 14				
11/17 Lecture 15				
11/22 Lecture 16				
11/ 29 Lecture 17	Homework 7 (11/11) Sequential Logic and Memory Due 12/ 01	Sequential Logic DRAM SRAM Flash		
12/ 01 Any Remaining topics+ Review				
Final Exam: 12/08 (Thursday) 4:00 – 7:00 PM				
Project Report Due: 12/04 (Sunday, 5 PM)				