UNIVERSITY OF CALIFORNIA, SANTA BARBARA
Department of Electrical and Computer Engineering

ECE225 *High-Speed Digital IC Design*

Homework #2

Due Date: Feb 15 by 5:00pm

1. ***Reading Assignment:*** Chapter 4 and 9 of the book:
   Digital Integrated Circuits: A Design Perspective (2nd Edition), Jan M. Rabaey et al., Prentice Hall, 2003.

2. Using the references provided (and your own literature search), discuss and analyze the effects of variability on interconnect parasitic (R-L-C) extraction procedures. Describe the state-of-the-art in this arena. List all relevant publications. What needs to be accomplished to account for variations during the extraction process? (see paper from Intel by Labun on extraction of C).

3. Multi-core designs are being adopted for future generations of high-performance ICs including microprocessors (see www.intel.com). For multi-core architectures, which alleviate power dissipation problems, interconnects are going to play a key role in determining the design and performance of such ICs. Write a report detailing the main philosophy behind multi-core designs and its various challenges. In particular, discuss the role of interconnects. Include a comprehensive list of all previous and related works in the literature. Discuss (and quantify, if possible) various implications of interconnect variations on multi-core architectures.