ECE 225
High-Speed Digital IC Design
Lecture 13

Low-power Dynamic Circuits:
low-power and high-performance design, keeper sizing issues, variation-tolerant keeper design

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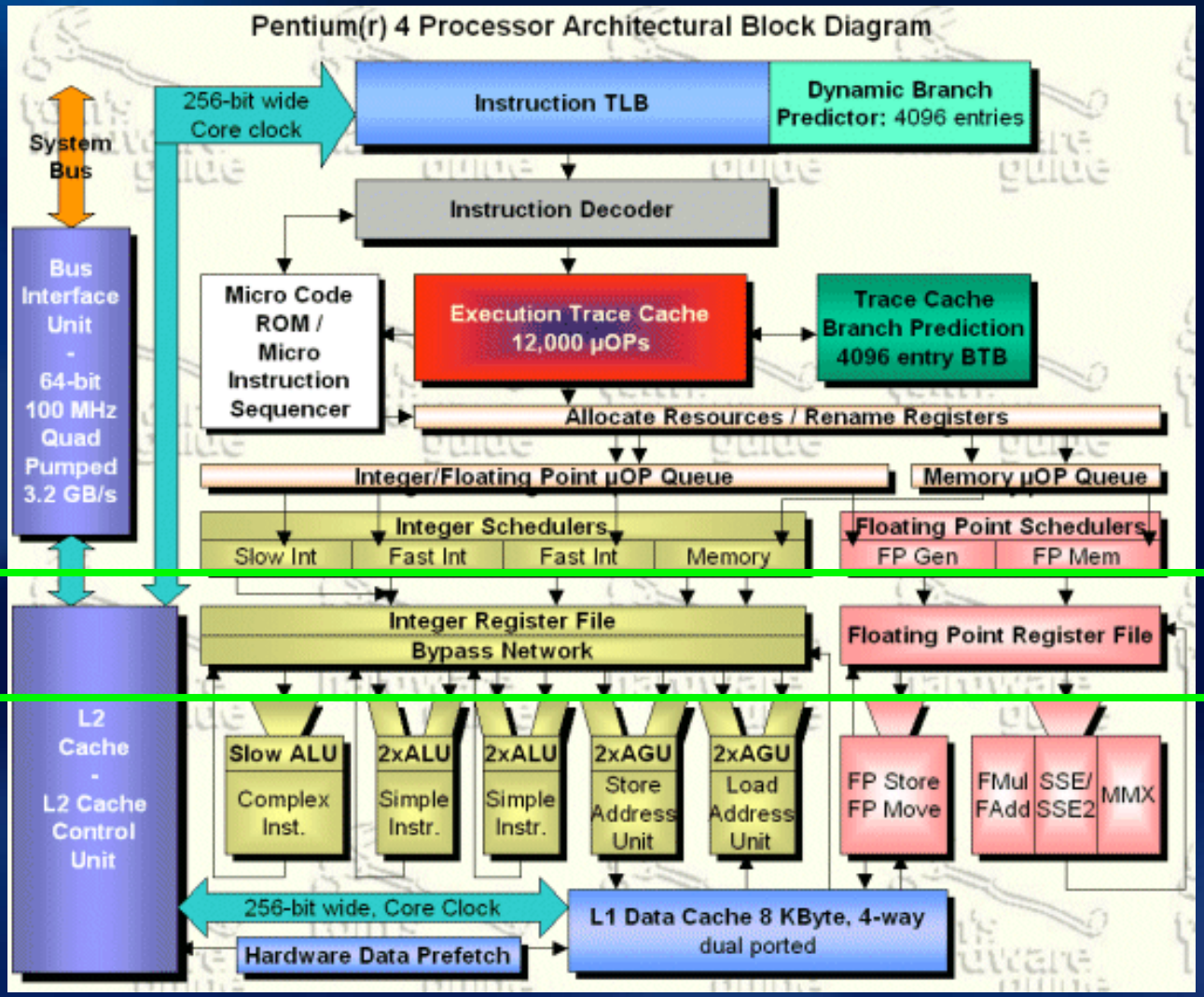
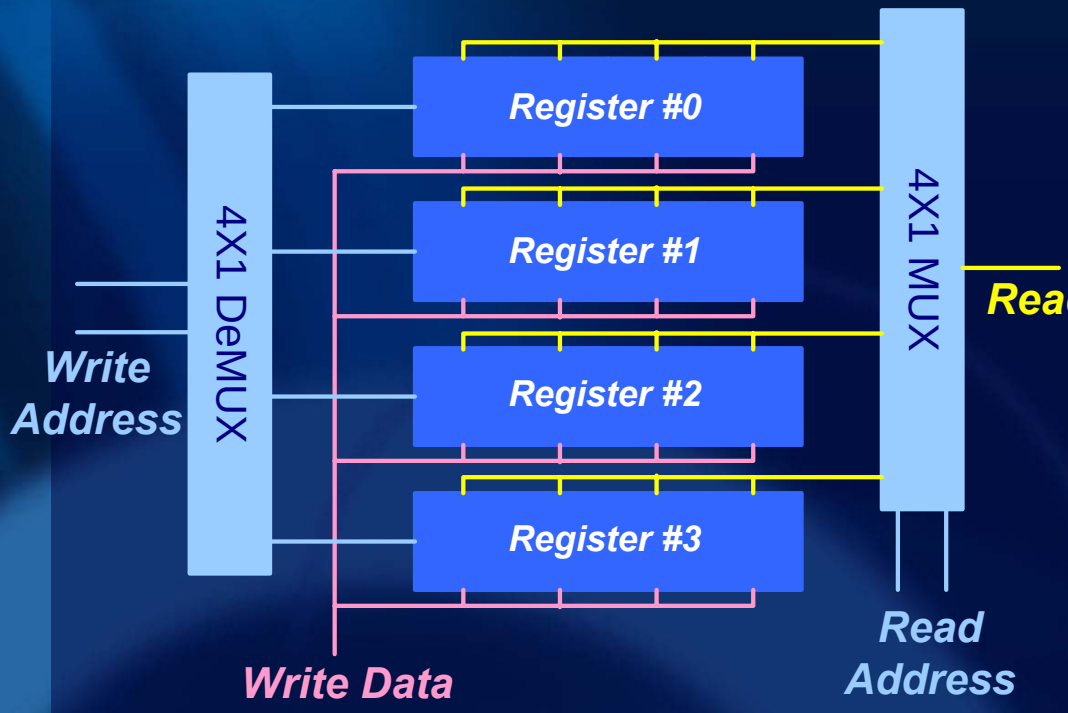
Motivation



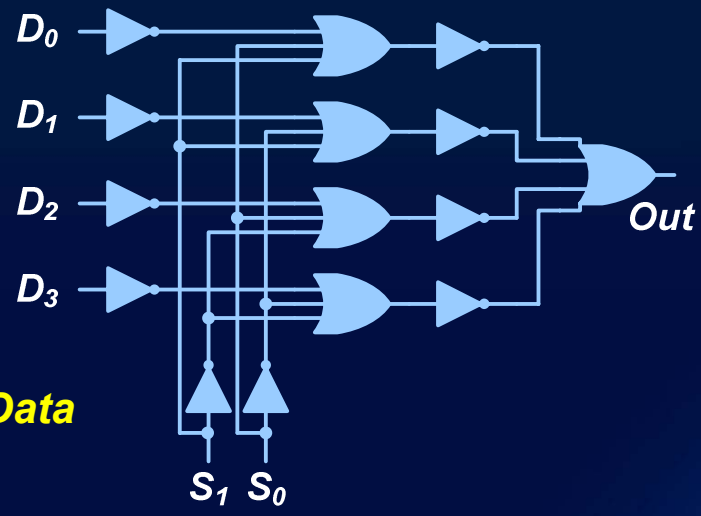
[Intel Inc.]

- **Register files are critical modules in computer architecture**

Motivation



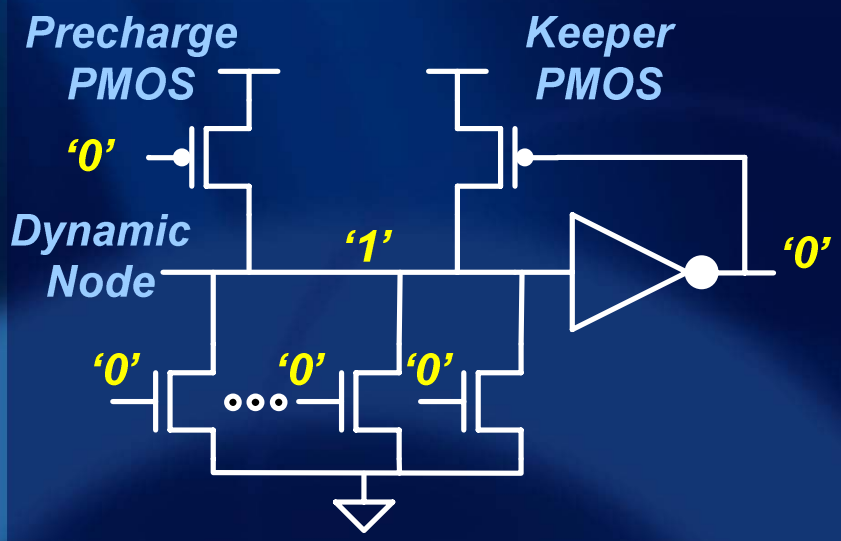
A Simple register File



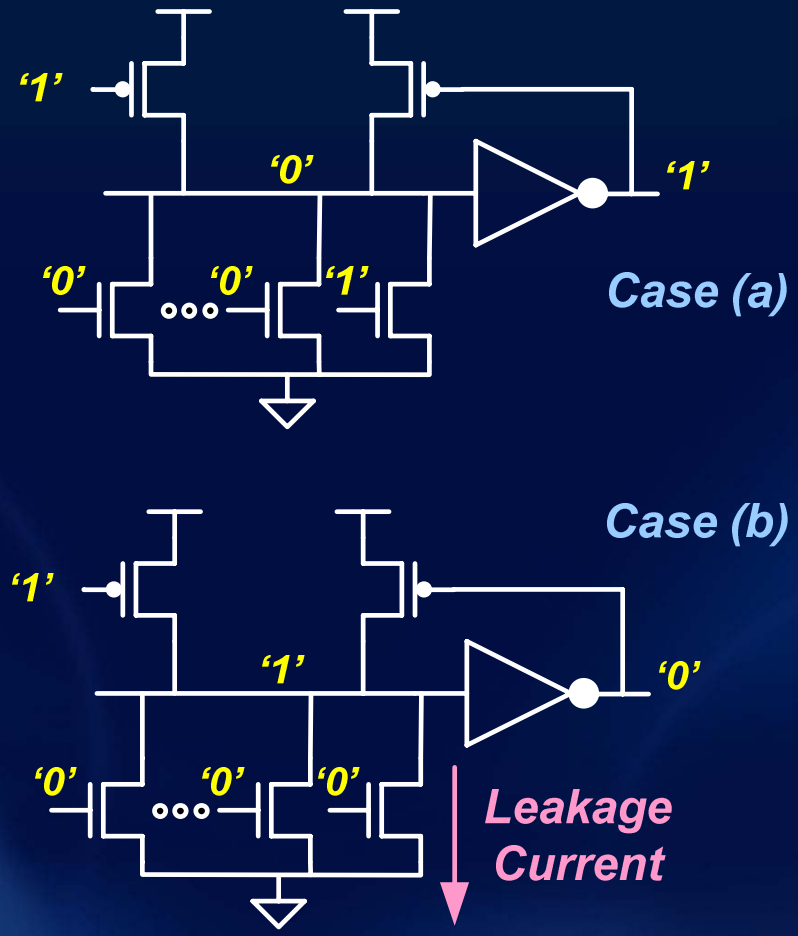
4X1 MUX

- Dynamic gates are preferred gate style in high-performance designs.
- Address decoder and multiplexers are realized using dynamic OR gates.

Motivation



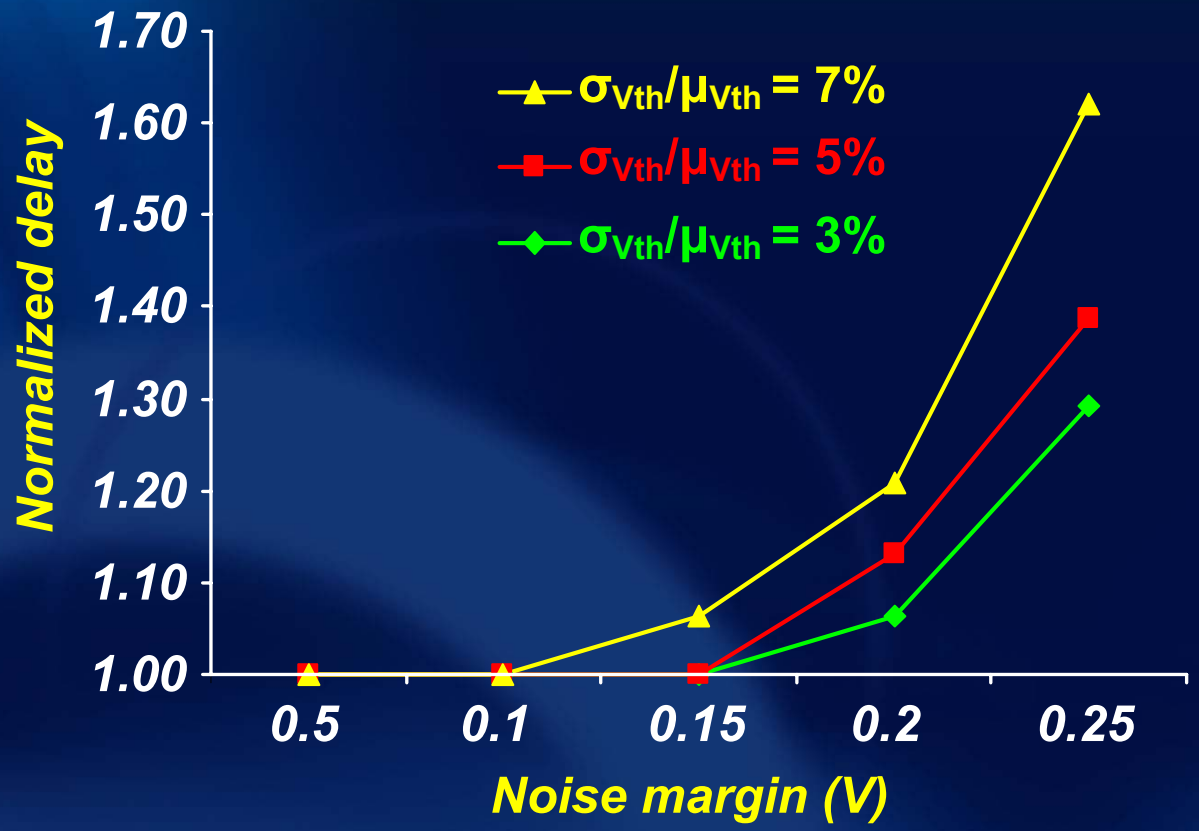
Precharge Phase



Evaluation Phase

- **Pre-charge and evaluation phases for dynamic gates**

Motivation

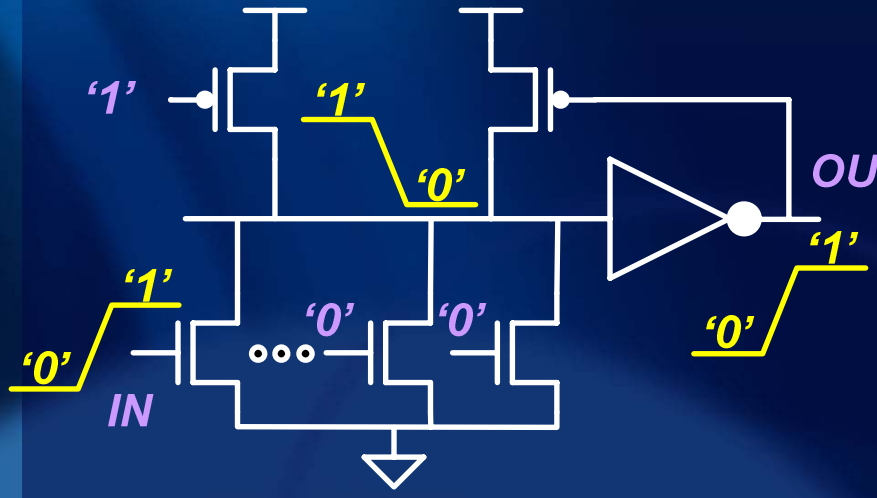


- **Trade-off between performance and robustness for traditional keeper.**

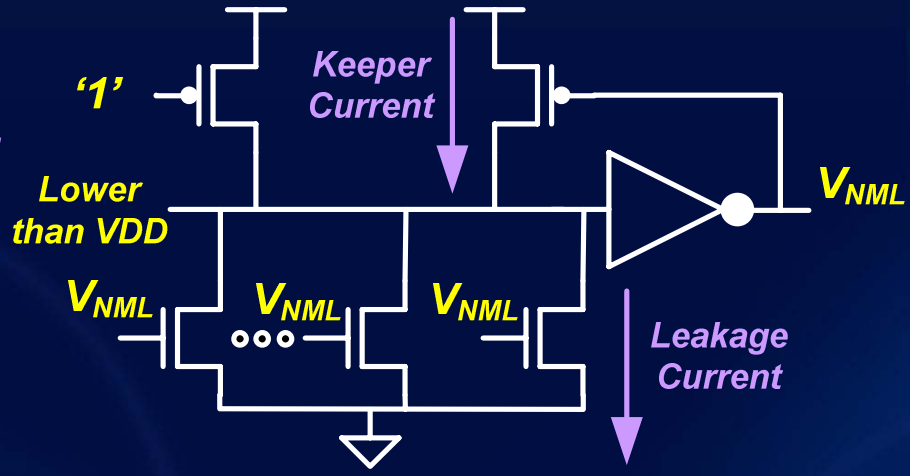
Outline

- Introduction
- Keeper Sizing
- Proposed Keeper
- Simulation Results
- Conclusions

Introduction



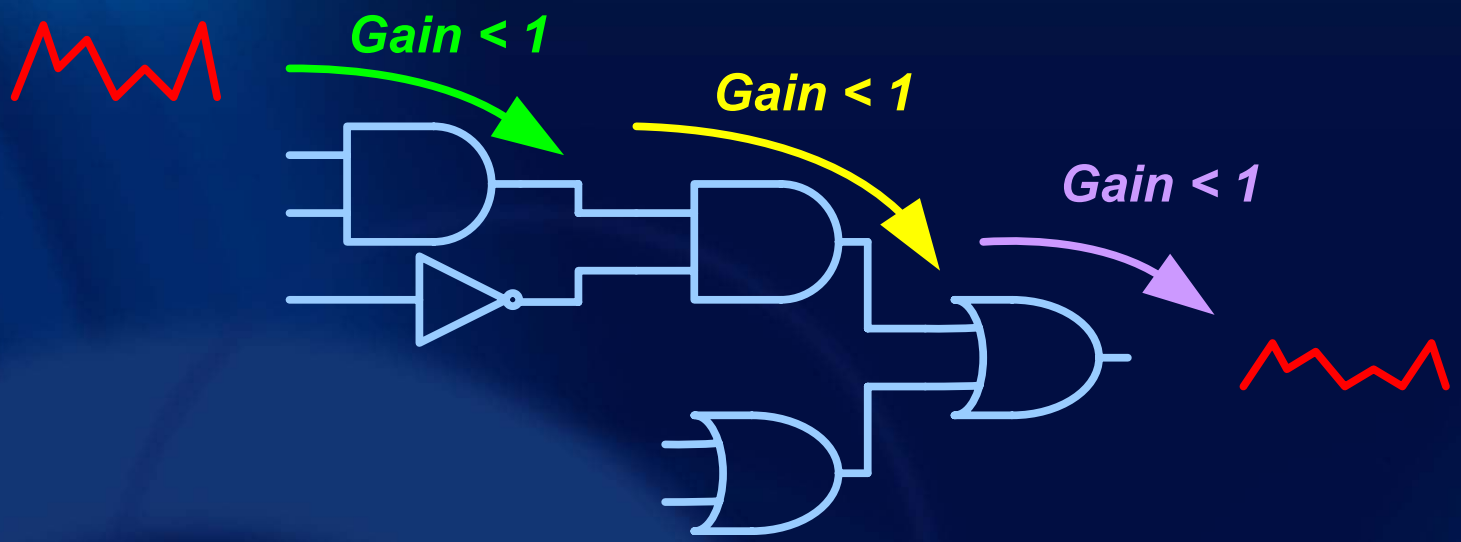
Delay of dynamic gate



Noise margin (Unity Noise Gain)

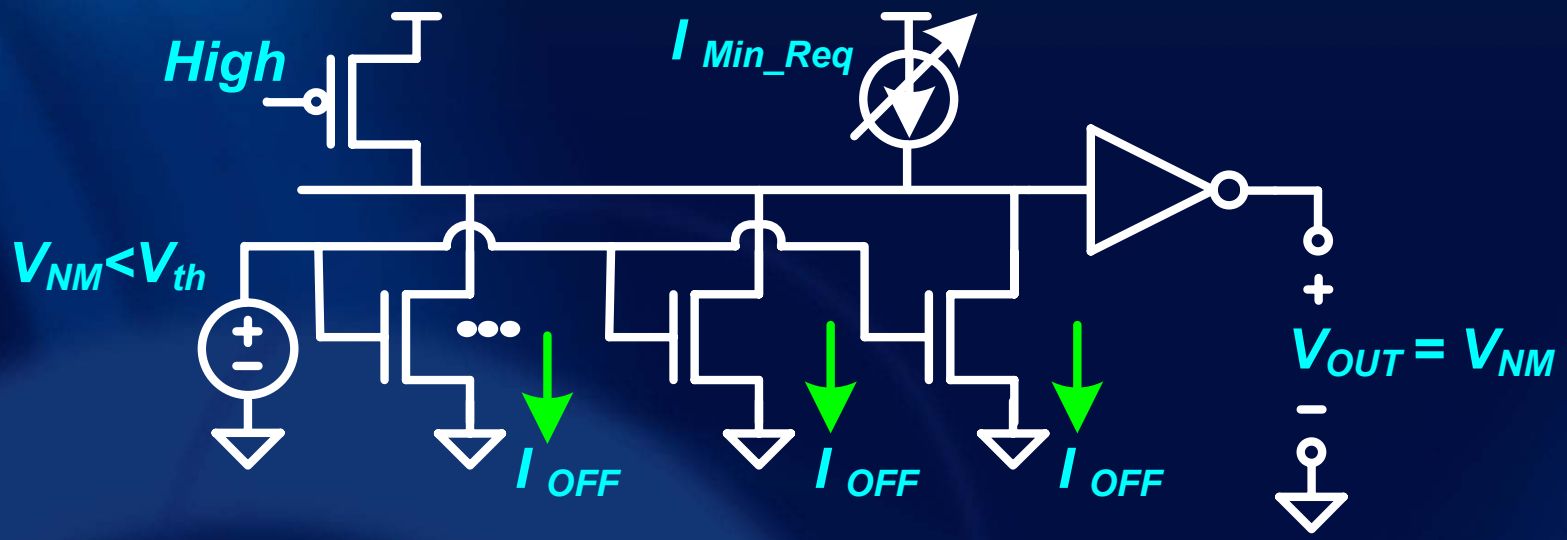
- Worst case delay occurs when only one input switches
- Unity Noise Gain (UNG) is the voltage level that when applied to all inputs, results in same output voltage.
- Trade-off between performance and robustness.

Introduction



- Noise margin definition is based on the fact that noise signal must not be amplified in a chain of logic gates.
- In this work we focus on correlated variation of threshold voltage.
- Impact of random variation can be considered by targeting a slightly higher noise margin.

Keeper Sizing

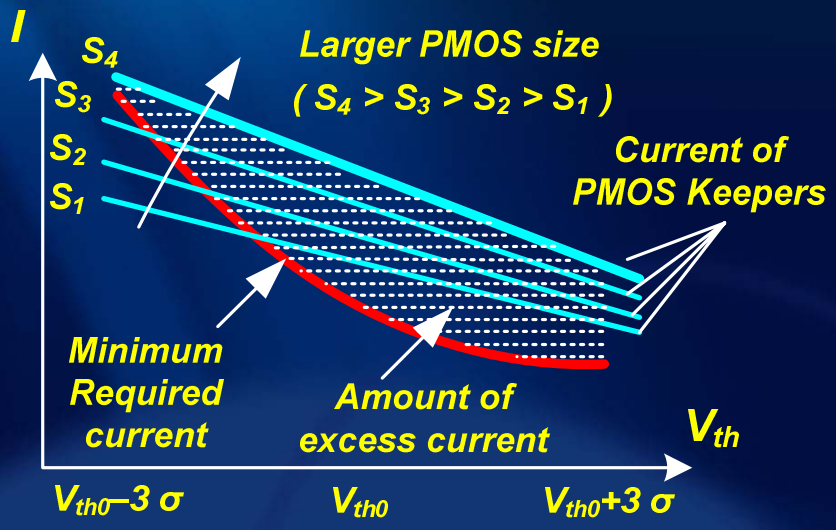


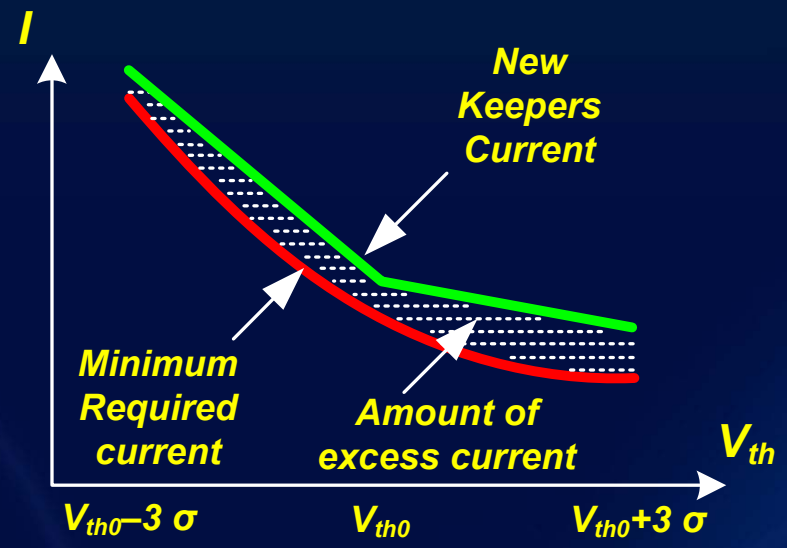
- *Minimum required current (* ideal keeper):

  smallest amount of current that must be injected to dynamic node to guarantee a particular level of UNG.

- Minimum required current is a strong function of V_{th} variation of pull down network transistors.

Keeper Sizing



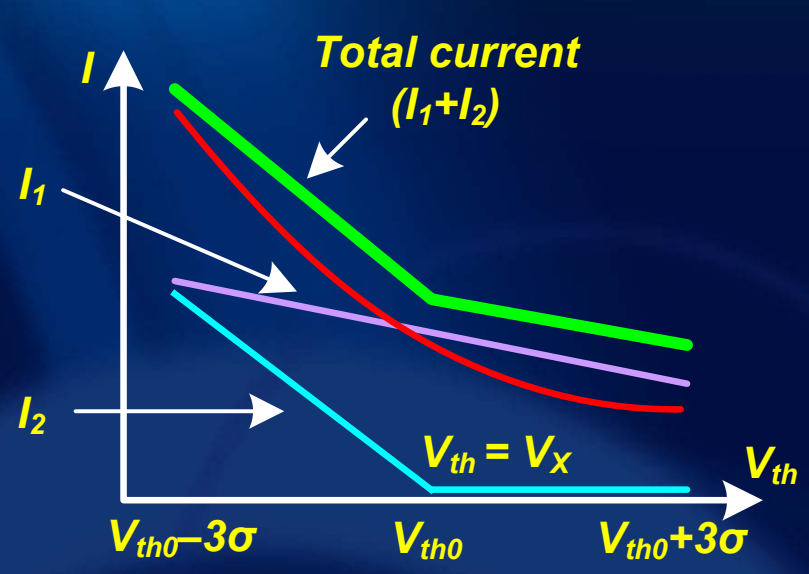


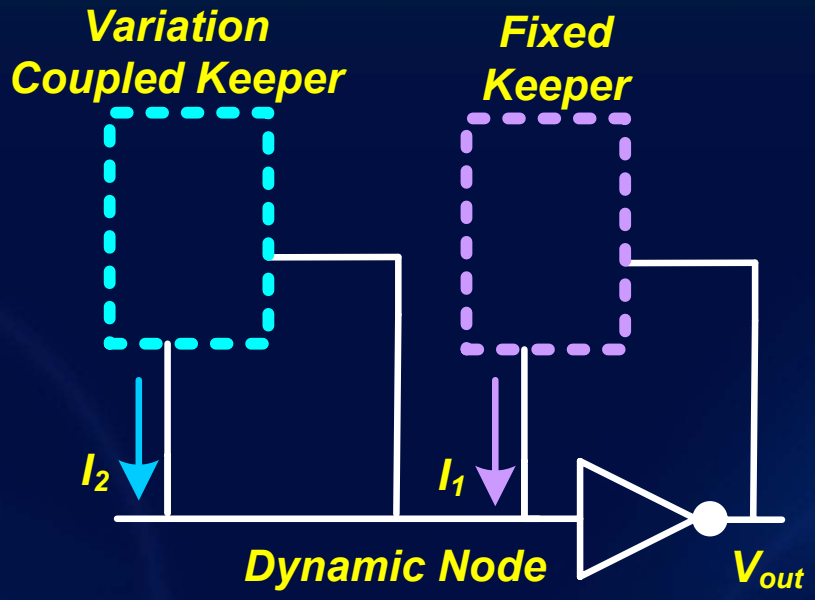
(a) Traditional keeper's behavior

(b) Proposed keeper's behavior

- **To maintain the minimum required current level over entire variation range, traditional PMOS keeper must be resized.**
- **At lower threshold voltage, top line (S_4) supplies enough current; however, at higher threshold voltage huge amount of excess current is injected to node.**

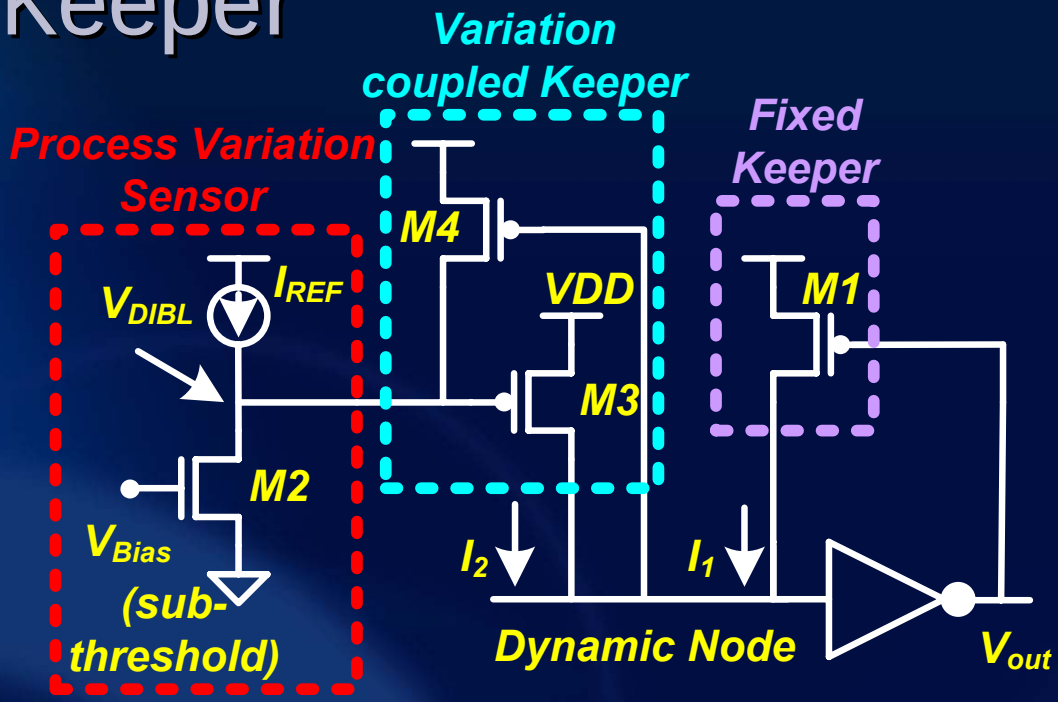
Proposed Keeper





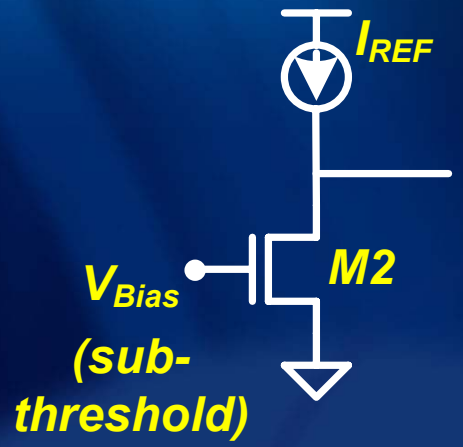
- New keeper is composed of two circuits.
- First one is a small fixed-size PMOS keeper.
- Second one is a variation-coupled keeper.
- Total current shows much better behavior compared to traditional PMOS keepers.

Proposed Keeper



- Beside two keepers, there is a process variation sensor.
- On lower V_{th} side, variation sensor provides higher V_{DIBL} voltage and hence, M_3 supplies less current. On higher V_{th} side vice versa.
- M4 is used to turn off M3 keeper when dynamic node needs to be pulled down.

Proposed Keeper



Process Variation Sensor (Kuroda et al. ISSCC 1996)

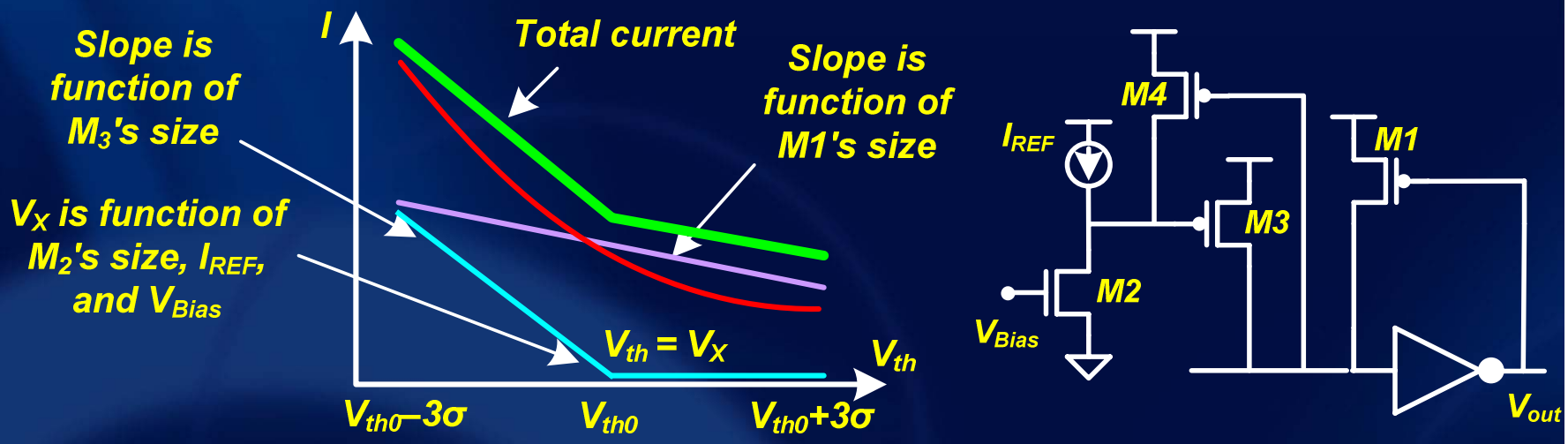
(a) $I_{REF} = \mu_n C_{ox} \frac{W}{L} V_T^{\,2} e^{\frac{V_{Bias} - (V_{th} - \eta V_{DIBL})}{nV_T}}$

(b) I_{REF} **and** V_{Bias} **are function of** nV_T**.**

(c) $V_{th} - \eta V_{DIBL} = cons.$

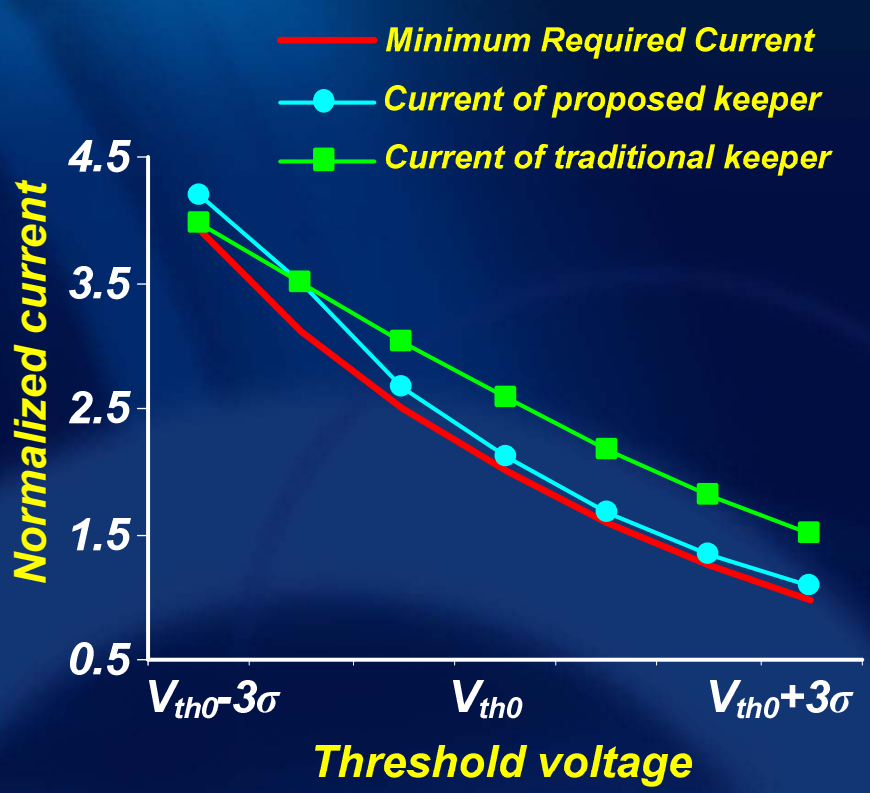
- I_{REF} and V_{Bias} are designed to be independent of V_{th} and it's variations.
- M_2 is biased to operate in sub-threshold region.
- Small variation in V_{th} of M_2 causes η time wider fluctuation on V_{DIBL}. (η is DIBL constant).

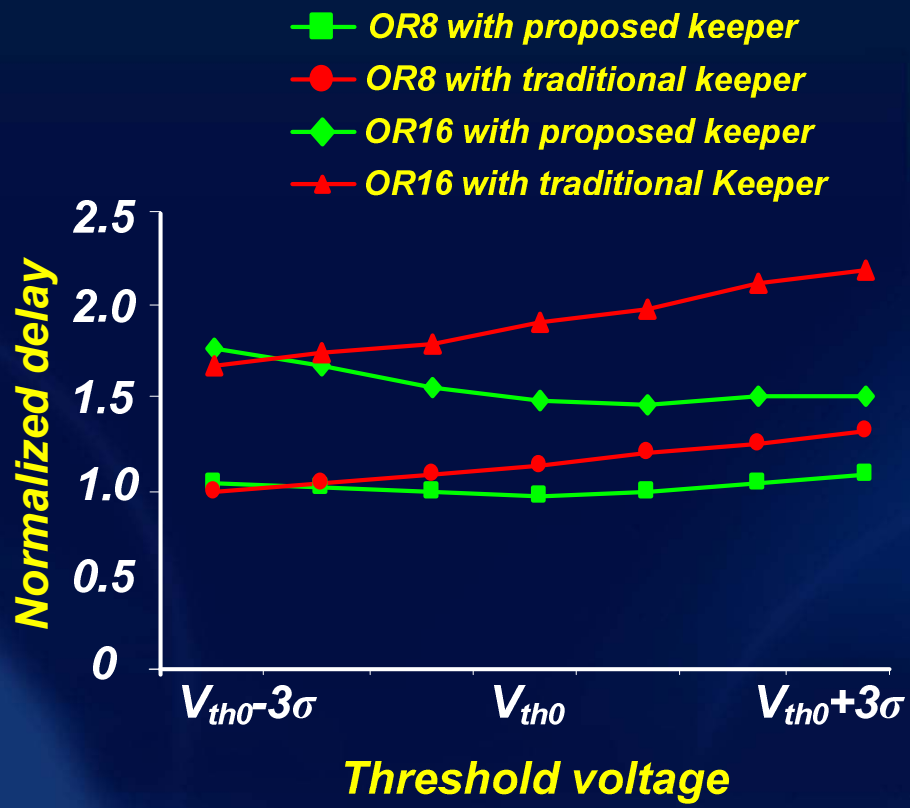
Proposed Keeper



- Through analytical equations, circuit parameter affecting keeper current curves have been studied.
- It is shown that each circuit parameter affects a separate part of curves which gives more flexibility in adjusting current curves to get best possible results.

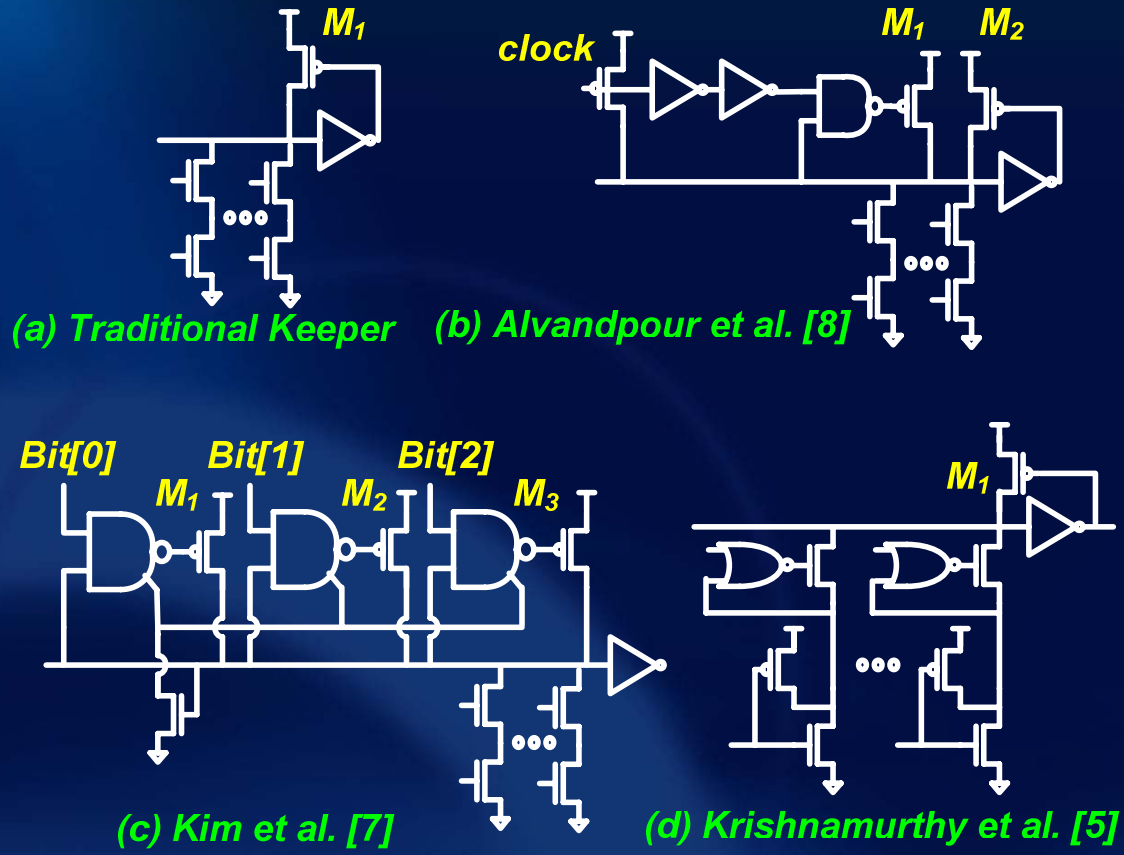
Simulation Results





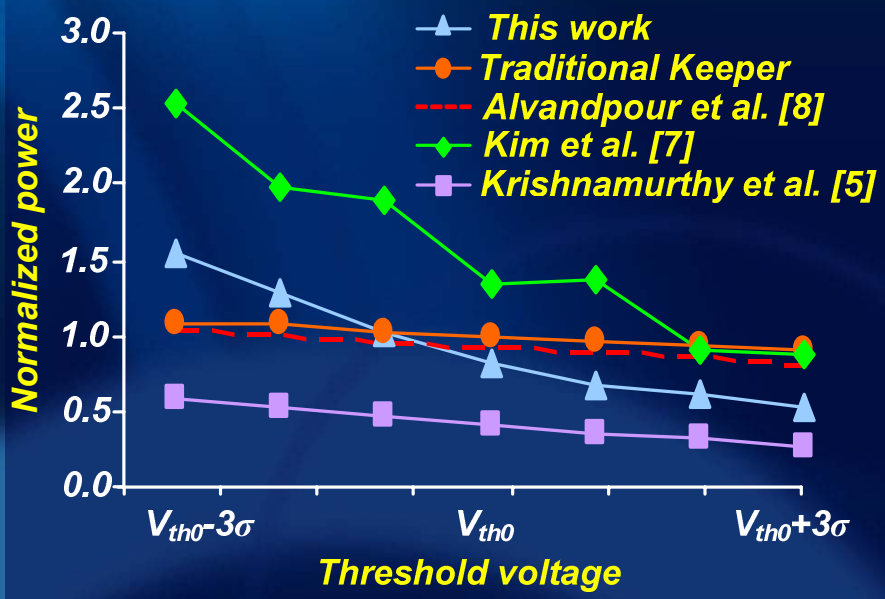
- Normalized current supplied by traditional and proposed keeper vs minimum required current. (left)
- Normalized delay of 8- and 16-input OR gates with traditional and proposed keeper. (right)

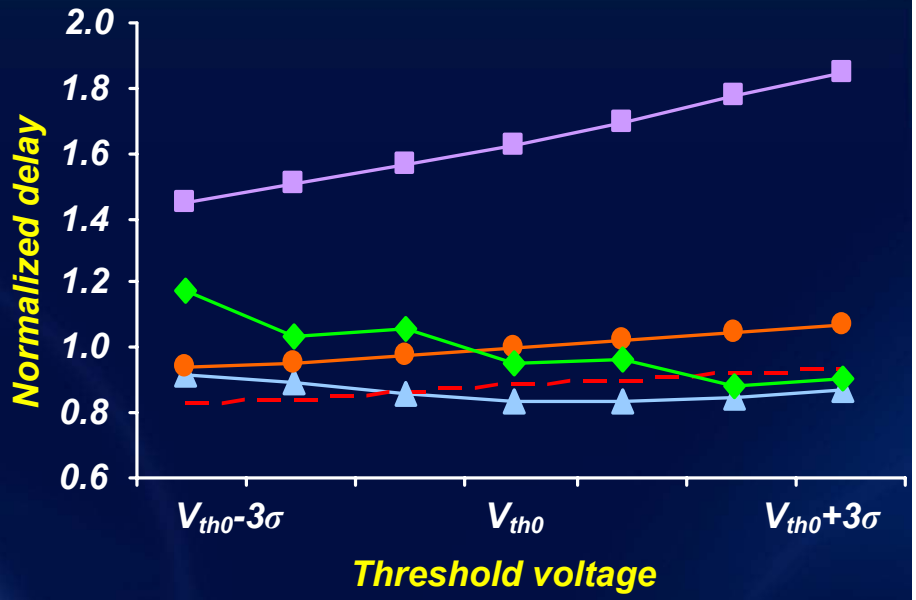
Simulation Results



- **Proposed keeper has been compared to previous work.**
- **Mean delay value, power consumption and standard deviation of delay are used as metrics.**

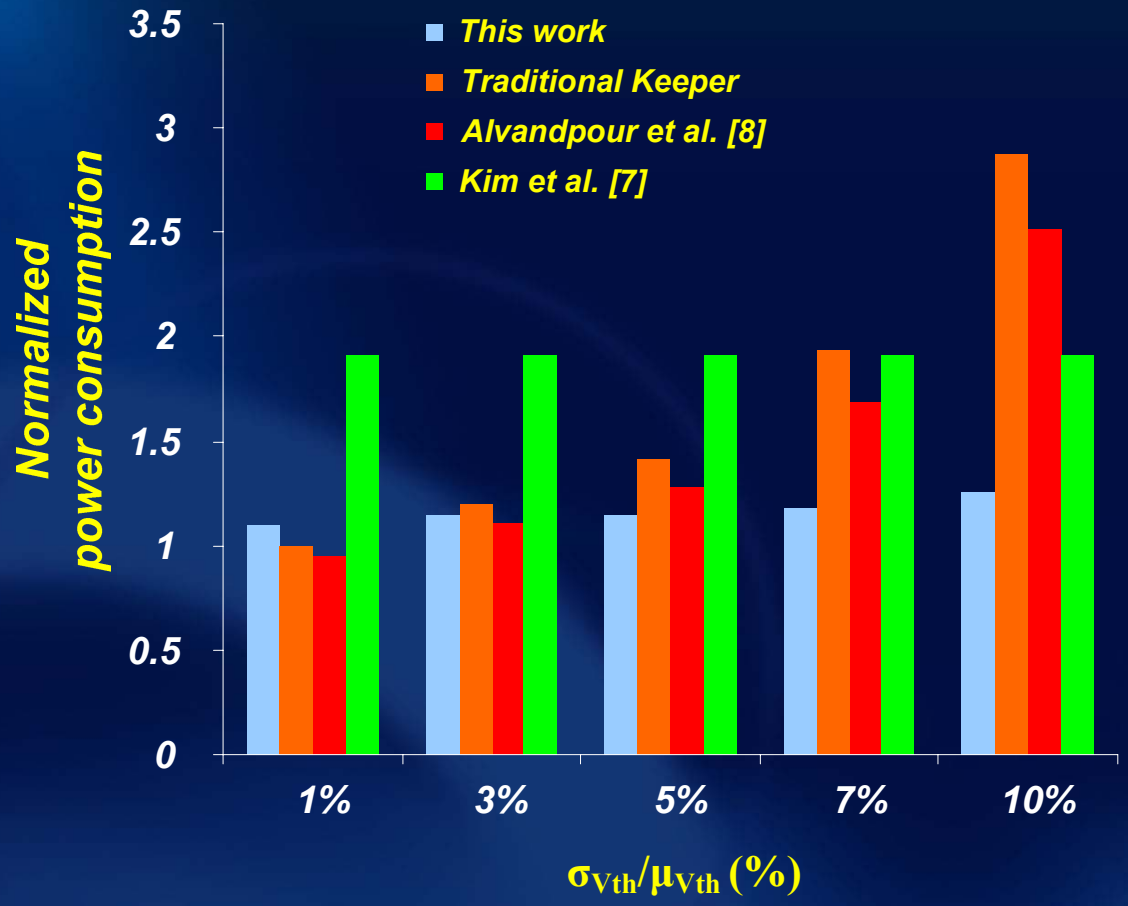
Simulation Results





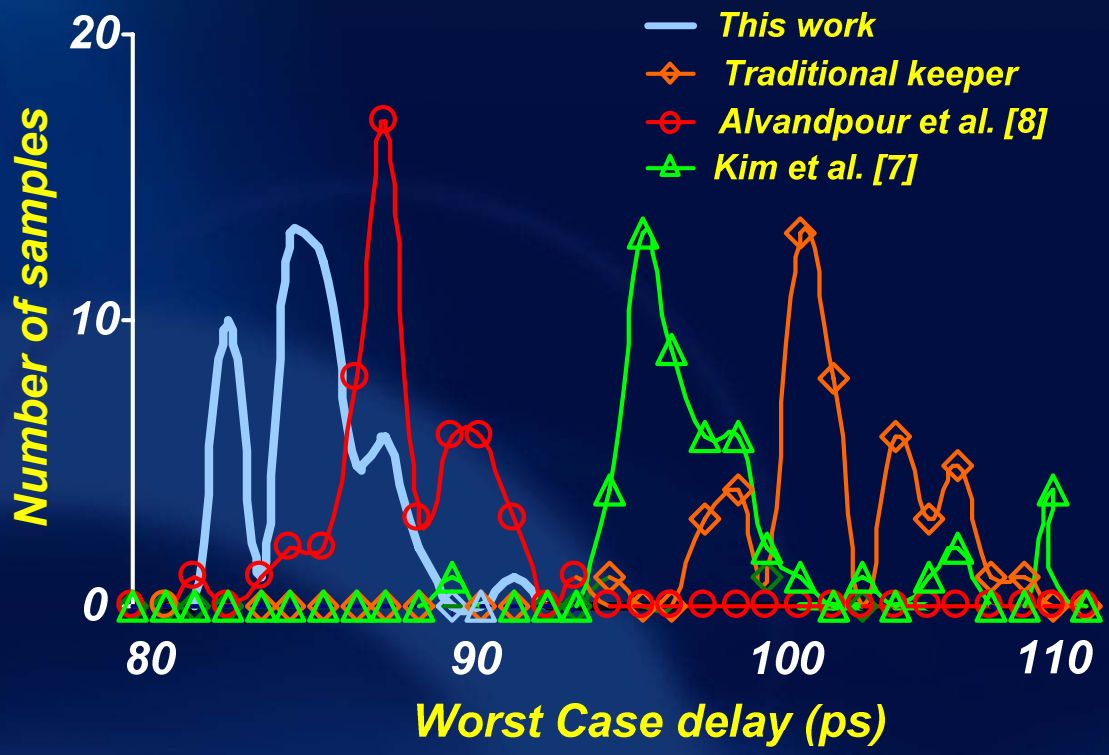
- **Comparison between normalized mean delay (left) and power consumption (right) of OR gates realized by different keepers.**
- **Proposed keeper shows low delay and power consumption.**

Simulation Results



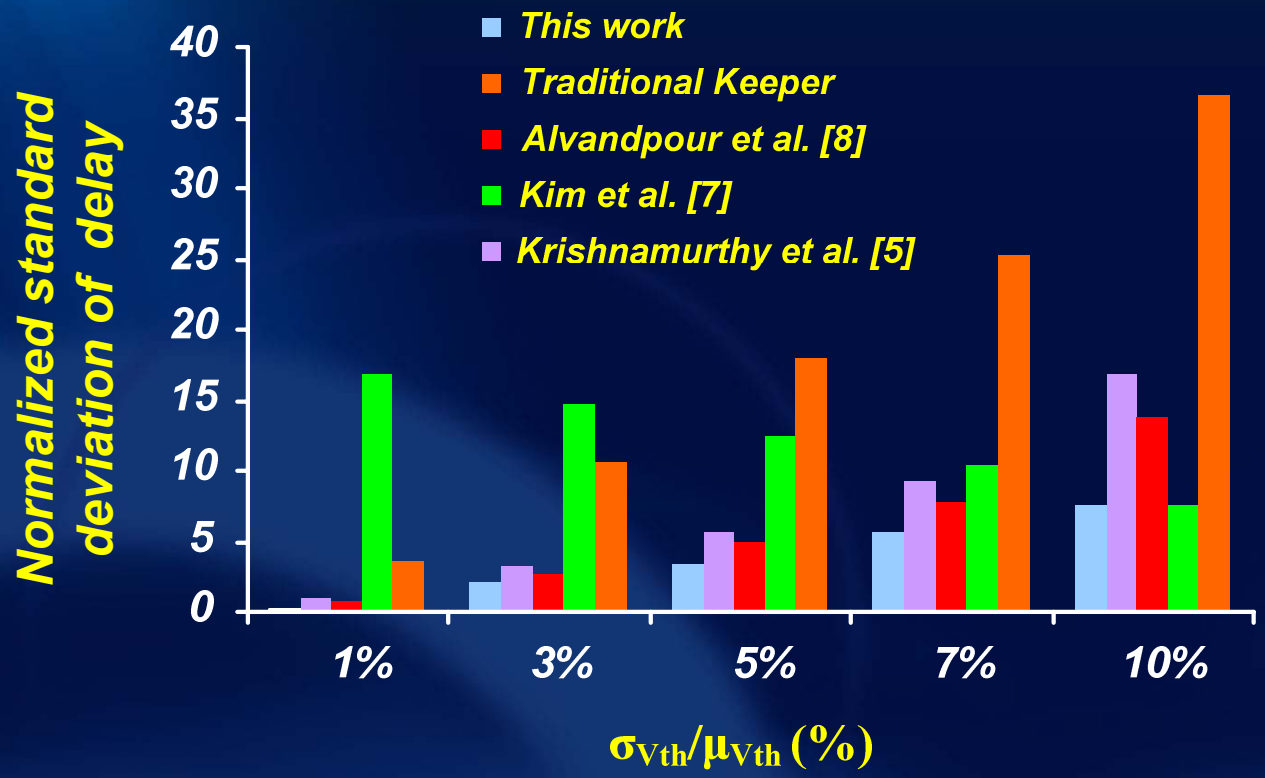
- **Normalized power consumption for different keepers at different levels of process variation (σ_{Vth}/μ_{Vth}).**

Simulation Results



- Delay distribution of dynamic OR gates with different keeper circuits obtained for 100 samples.
- Distribution corresponded to proposed keeper shows lower mean and narrower spread.

Simulation Results



- Normalized STD of delay for different keepers at different levels of process variation (σ_{Vth}/μ_{Vth}).
- Proposed keeper shows superior behavior in terms of robustness to increasing level of variation.

Conclusions

- **A novel approach for designing low-power variation-aware keeper circuits of wide fan-in dynamic gates has been presented.**
- **HSPICE simulation results show that the proposed architecture offers smallest delay deviation for entire *Vth* range compared to all existing works in the literature.**
- **The proposed keeper architecture could be very effective in increasing the robustness of dynamic gates to process variation.**