

ECE 225

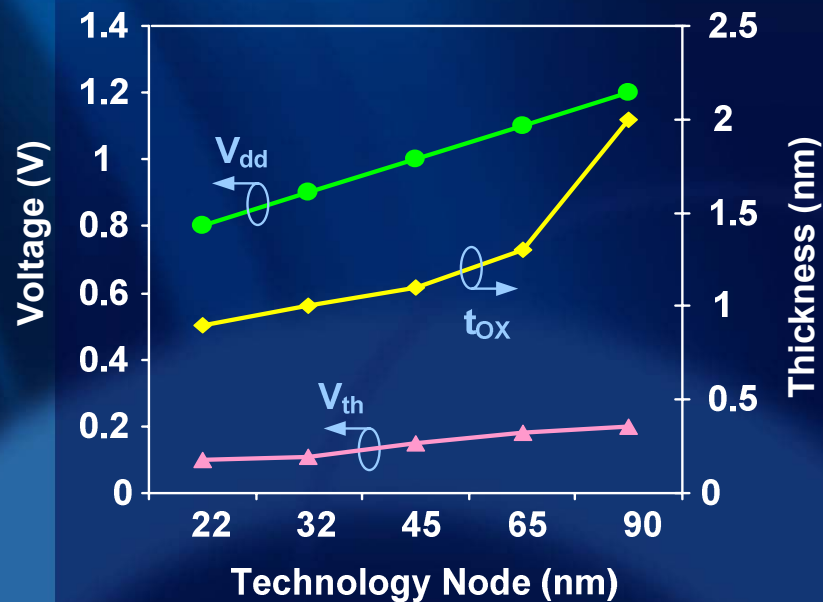
High Speed Integrated Circuit Design

Lecture 15

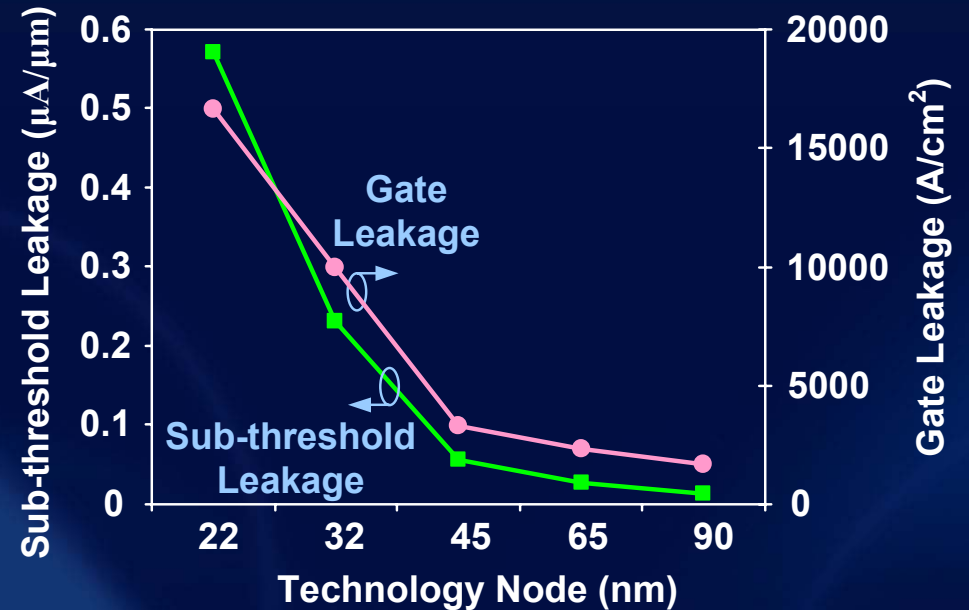
***Ultra Low-Power Design: Hybrid NEMS-CMOS
Circuits for sub kT/q Operation***

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CMOS Scaling Trends



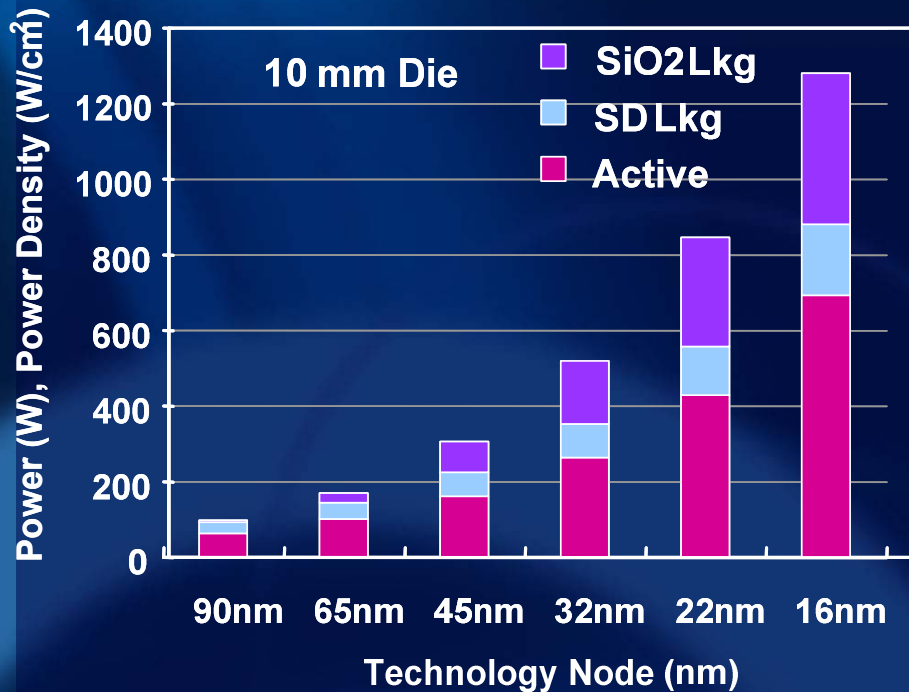
Source: ITRS 2005



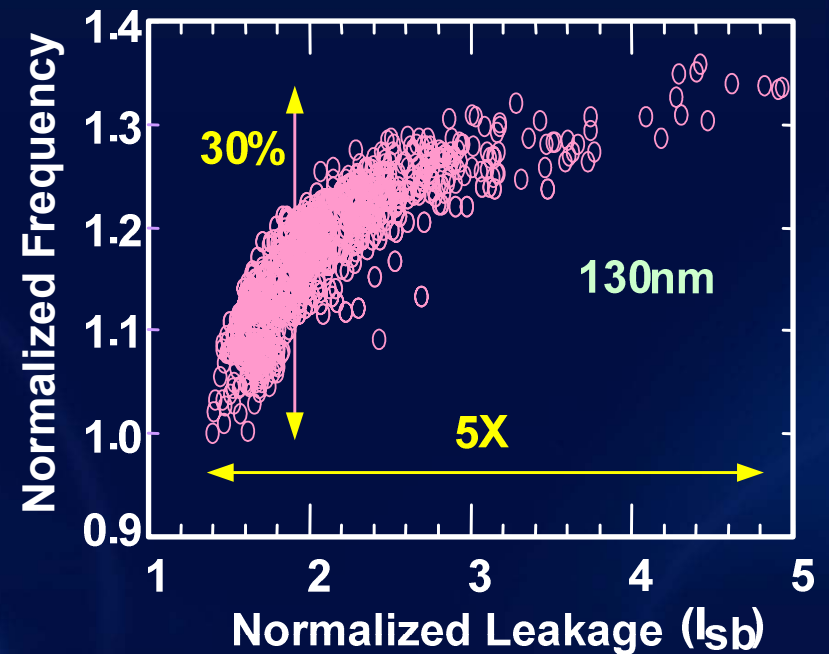
Source: ITRS 2005

- Subthreshold and gate leakage increase dramatically with scaling device parameters.

Leakage, Not Good !



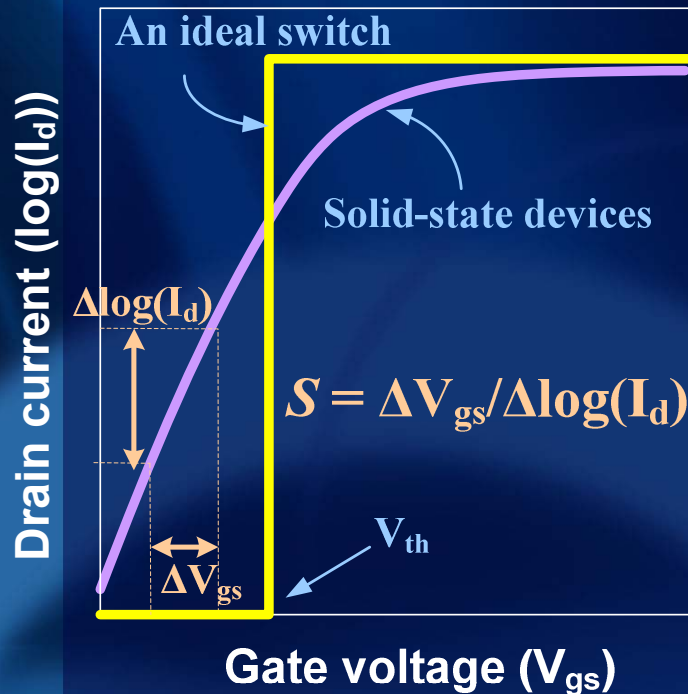
Source: Intel Corp.



Source: Intel Corp.

- Leakage will account for nearly 50% of total power consumption in 16 nm technology node
- More than 5X leakage variation in 130 nm technology node

Theoretical Limit for Sub-threshold Swing of CMOS Devices



Analytical equation for sub-threshold swing (S) of CMOS devices

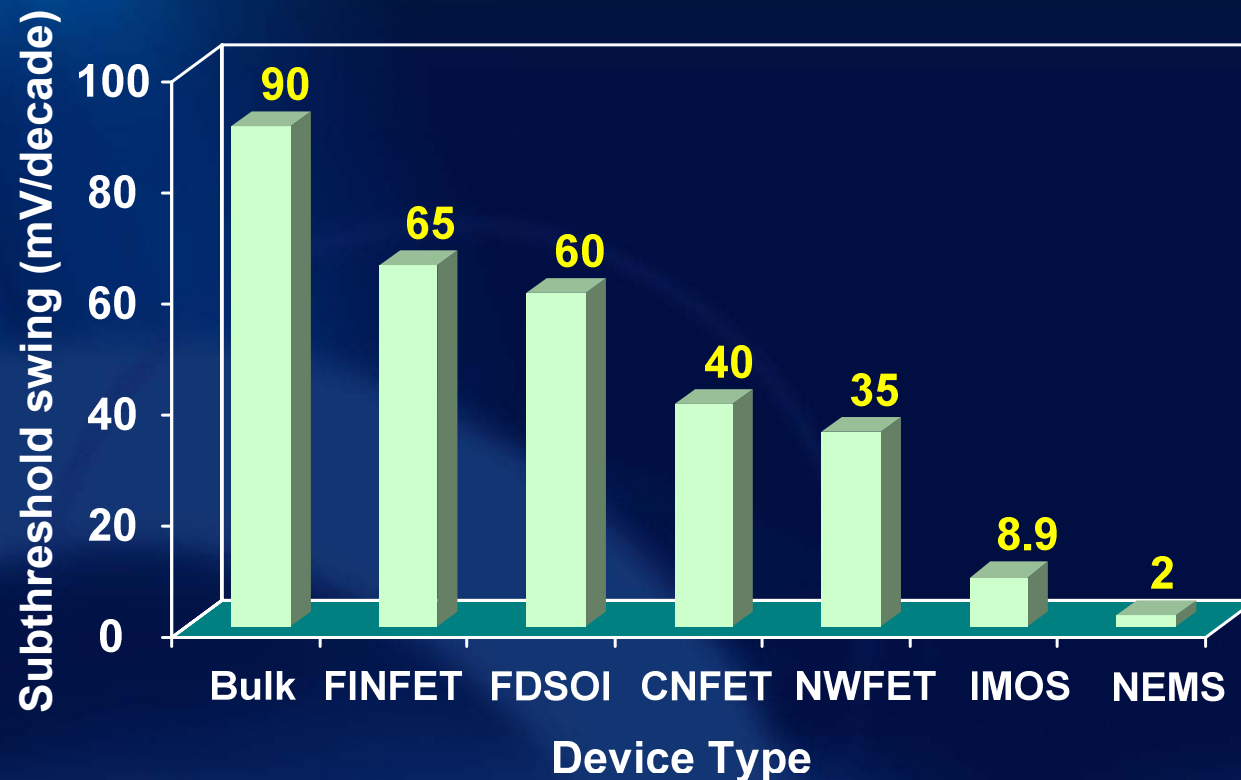
$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} (m-1) \left(\frac{kT}{q} \right)^2 e^{q(V_g - V_t) / mkT} (1 - e^{-qV_{ds} / kT})$$

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g} \right)^{-1} = 2.3 \frac{mkT}{q} = 2.3 \frac{kT}{q} \left(1 + \frac{C_{dm}}{C_{ox}} \right)$$

If $C_{dm} \approx 0$, then $S_{Min} = 2.3 \times 26 \approx 60 \text{ mV/decade}$

- Theoretical limit for sub-threshold swing of all CMOS devices is proven to be **60 mV/decade**

Low Sub-threshold Swing Transistors

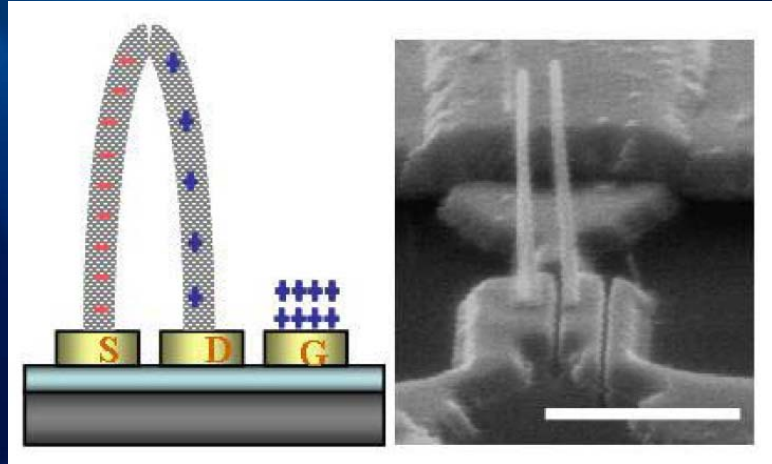


- Minimum measured subthreshold swing value for different MOS devices reported in the literature (references cited in the paper)

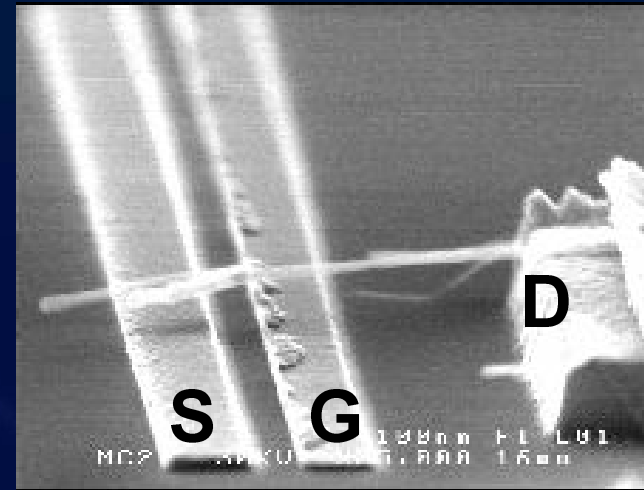
Outline

- **Nano-Electro-Mechanical Switches (NEMS)**
- **Fabrication Feasibility of Hybrid NEMS-CMOS Circuits**
- **Application of Hybrid NEMS-CMOS technology in design of:**
 - **SRAM cells**
 - **Dynamic OR gates**
 - **Sleep transistors**
- **Conclusions**

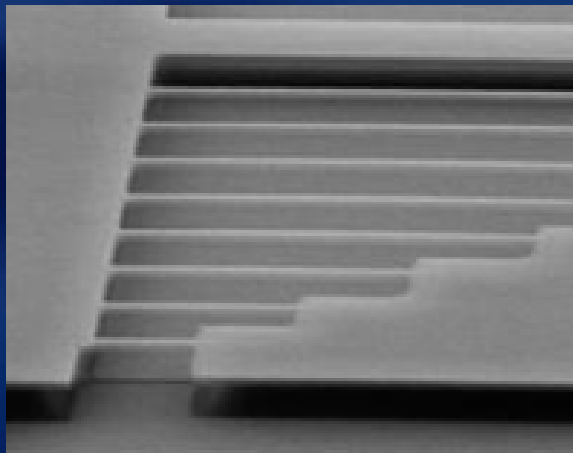
Nano-Electro Mechanical Systems (NEMS)



NEMS-based DRAM
Jang, et al. *IEDM 2005*



CNT-based relay
Lee, et al. *Appl. Phys. 2003*

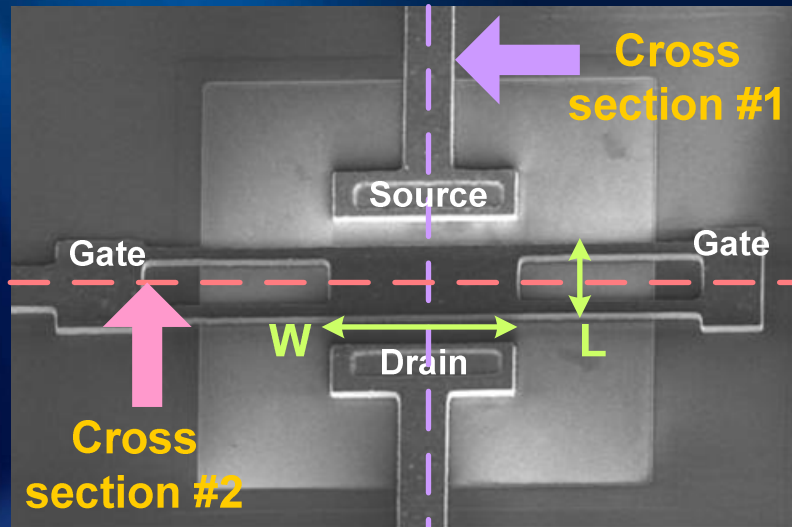


NEMS resonators
Carr, et al. *Appl. Phys. 1999*

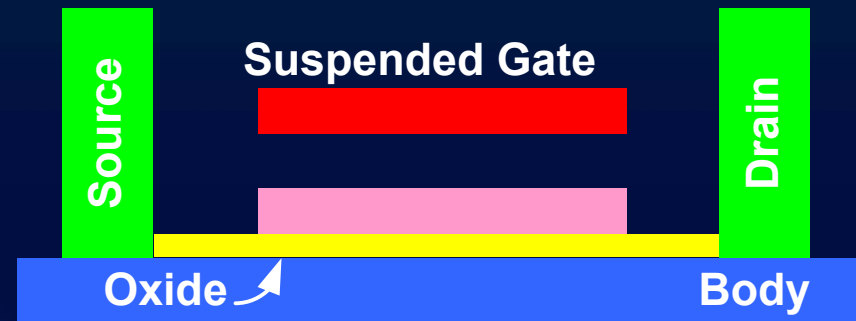
- NEMS can operate in **GHz** range due to very small mass
- NEMS resonators of $l = 2\mu m$ can have Resonance frequency of **400 MHz**

$$f_0 = \frac{(4.730)^2}{2\pi} \frac{1}{l^2} \sqrt{\frac{EI}{\rho A}}$$

Suspended Gate MOSFET (SG-MOSFET)



Proposed by Ionescu, et al. *ISQED 2002*
& Fabricated in Abele, et al. *IEDM 2005*



Cross section #1

- Gate when the device is ON
- Gate when the device is OFF



Cross section #2

- Gate when the device is ON
- Gate when the device is OFF

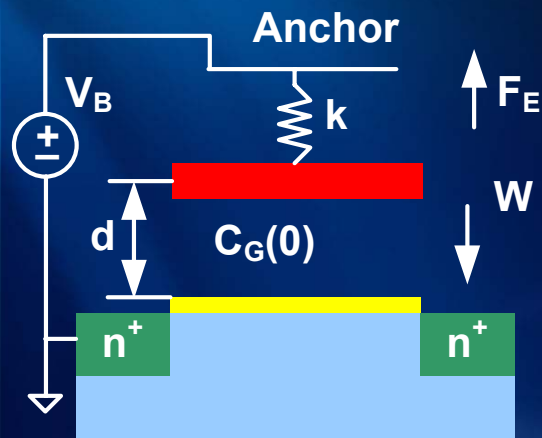
Advantages

- Very low gate leakage
- Very low subthreshold leakage
- Possible Integration in CMOS process

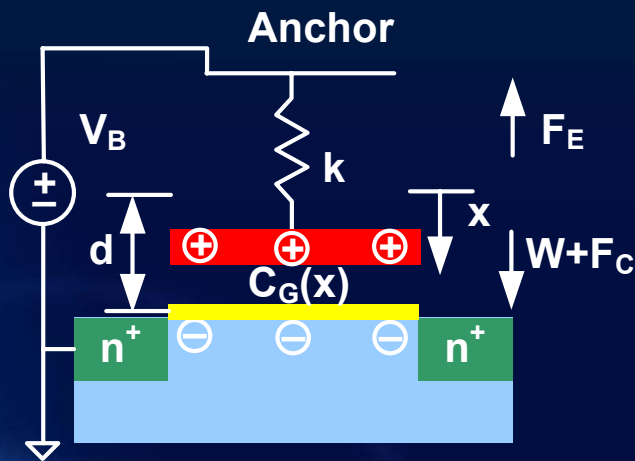
Disadvantage

- Low ON current compared to CMOS devices

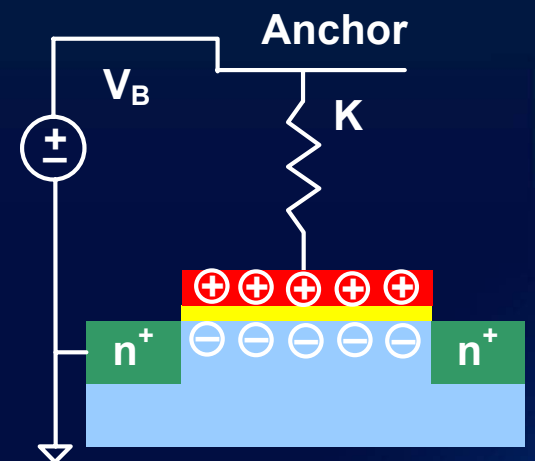
Abrupt Switching of SG-MOSFET



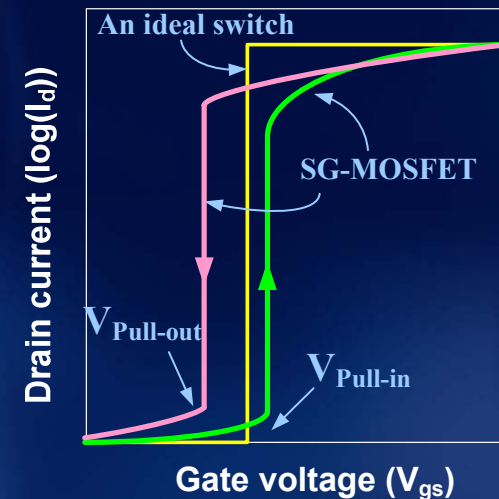
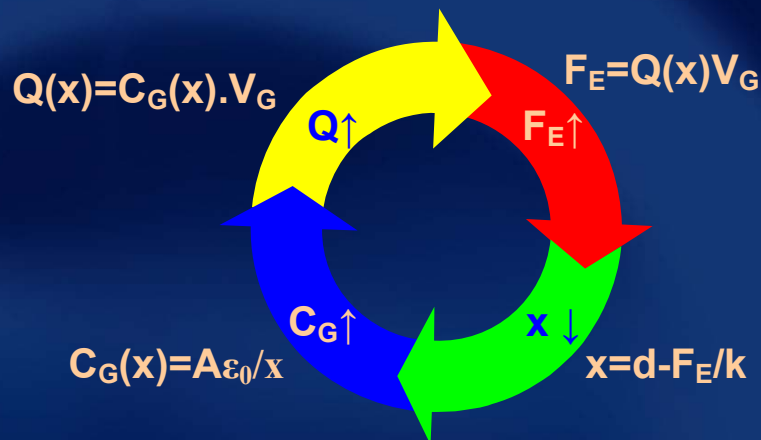
(a) $V_B = 0$ (OFF state)



(b) $0 < V_B < V_{\text{Pull-in}}$ (OFF state)



(c) $V_B > V_{\text{Pull-in}}$ (ON state)



- Operation of SG-MOSFET under three different bias conditions.

Idea: Hybrid NEMS-CMOS

CMOS ?

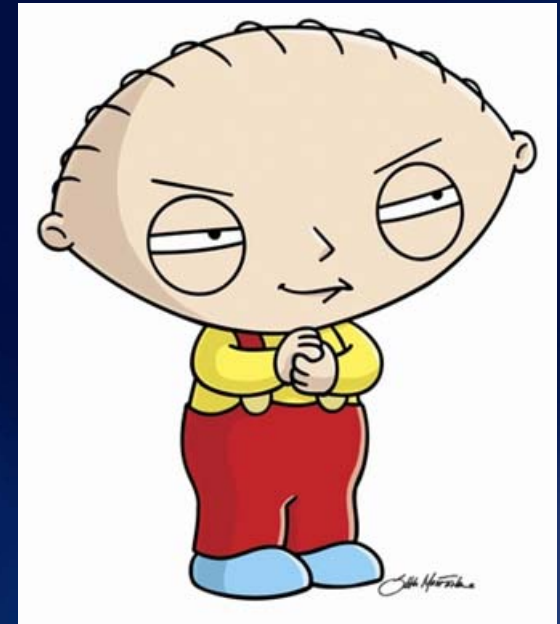
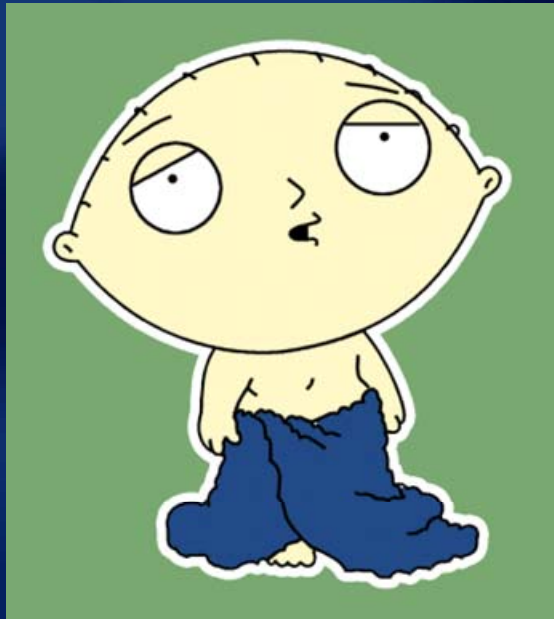
Very high OFF current
High ON current

NEMS ?

Very low OFF current
Low ON current

Hybrid NEMS-CMOS

Very low OFF current
High ON current



SG-MOSFET Modeling

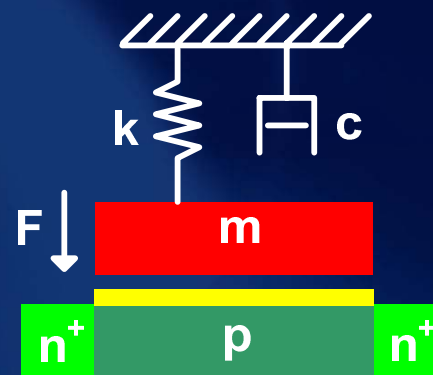
Electrical	Mechanical
$V = I.R$	$f = v.c$
$V = C \int I.dt$	$f = K^{-1} \int v.dt$
$V = L \frac{dI}{dt}$	$f = m \frac{dv}{dt}$

Analogous equations

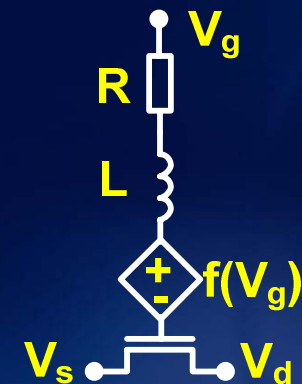
Electrical	Mechanical
Voltage, V	Force, f
Current, I	Velocity, v
Resistance, R	Damping, c
Capacitance, C	Stiffness ⁻¹ , K^{-1}
Inductance, L	Mass, m

Analogous parameters

- Interaction between mechanical and electrical entities complicates modeling of SG-MOSFET
- However, a simplified equivalent HSPICE model is proposed by



SG-MOSFET structure



Equivalent electrical model

Ionescu, et al. *ISQED 2002*

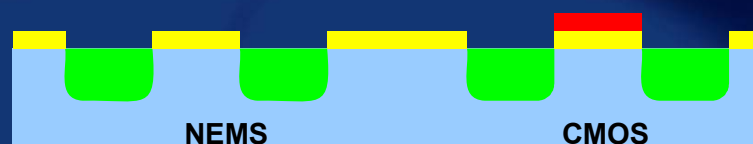
Fabrication Feasibility of SG-MOSFET



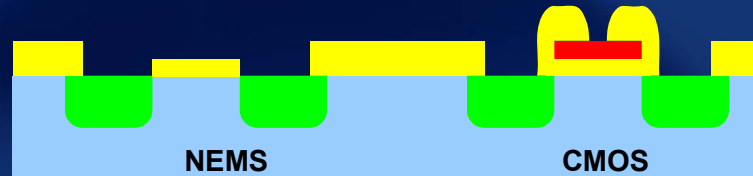
(a) Formation of poly gate for CMOS



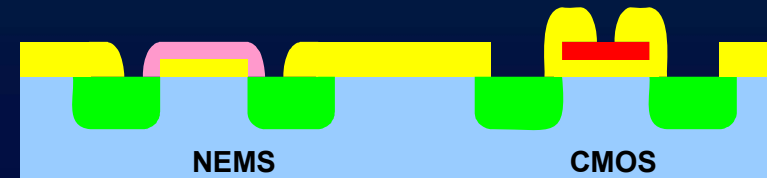
(b) Definition of active area for CMOS



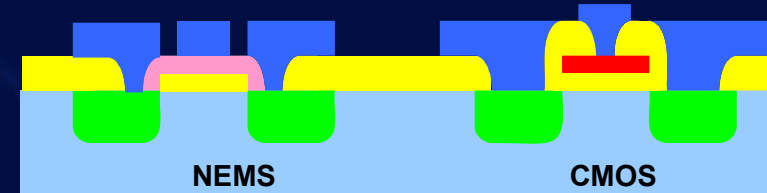
(c) Definition of active area for NEMS



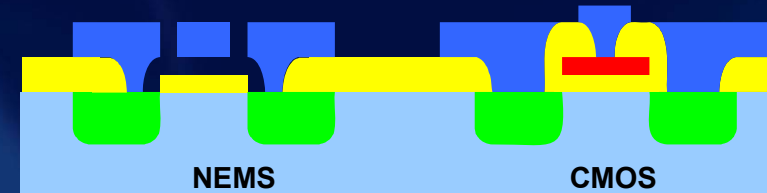
(d) Growth of thick oxide layer



(e) Sacrificial layer deposition



(f) AlSi metalization and dry etching

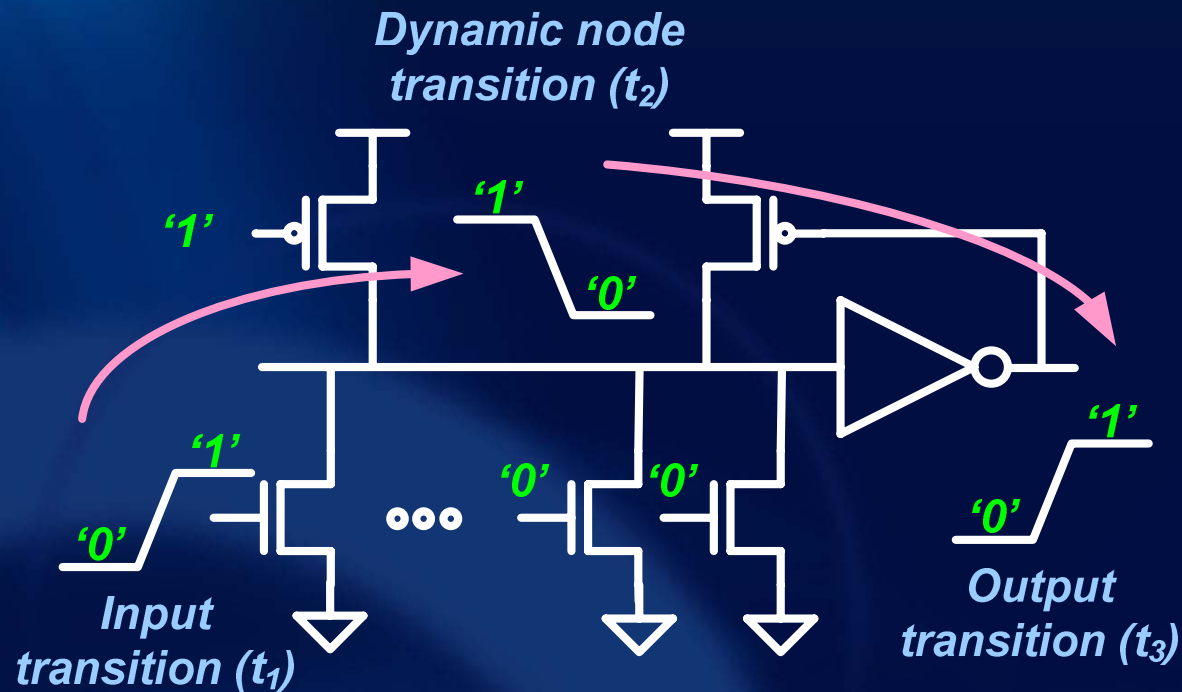


(g) Release of metal gate

■ ALSi 1% ■ Poly ■ Oxide
■ Source/Drain ■ Polymide

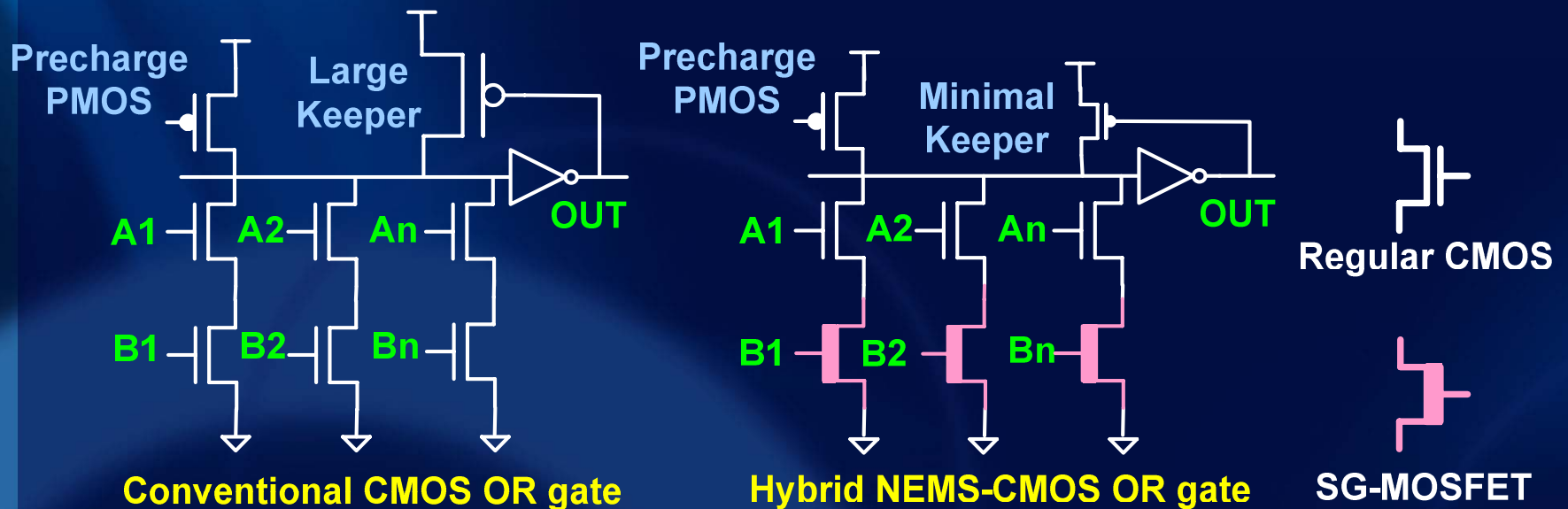
- Simplified proposed fabrication model for hybrid NEMS-CMOS technology (Based on Abele, et al. *IEDM 2005*)

Issues with CMOS Dynamic OR Gates



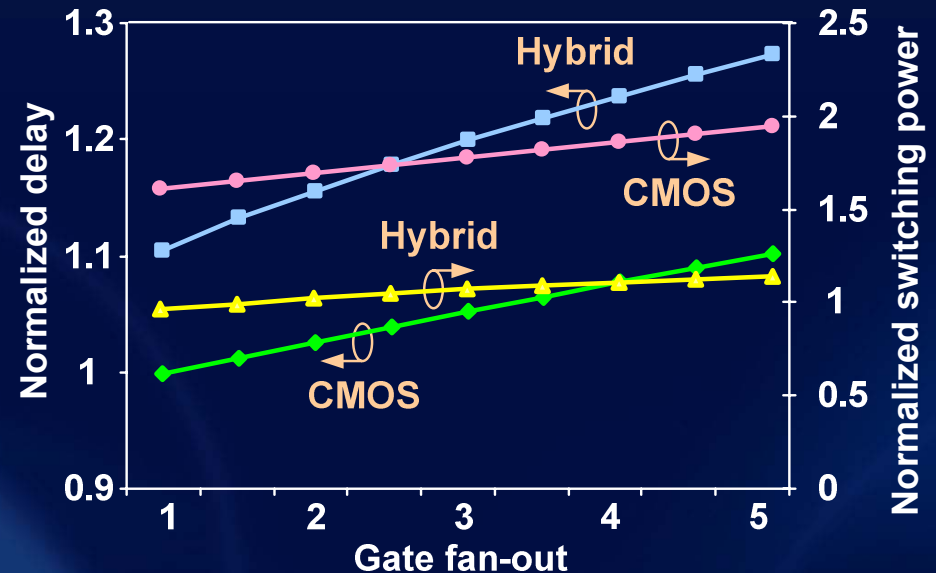
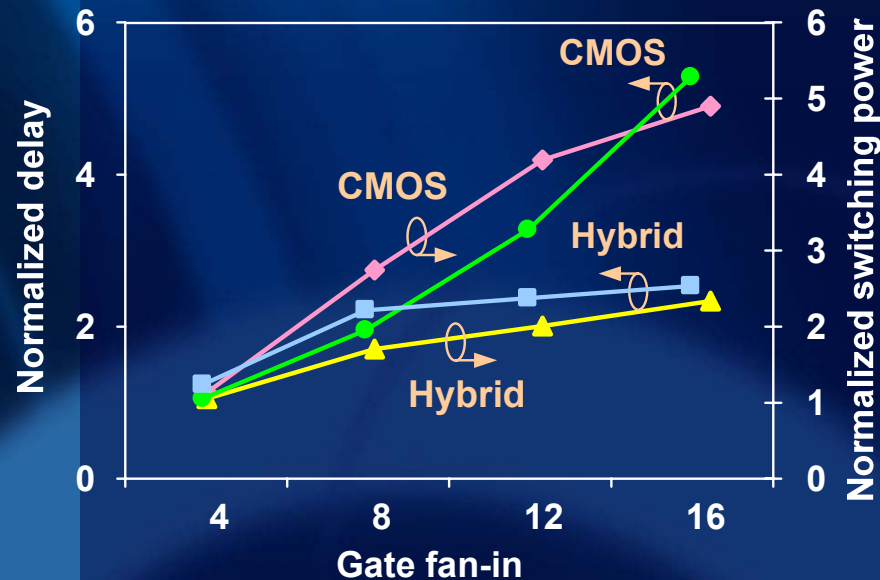
- High leakage current reduces reliability of dynamic gates
- Reliability can be improved by using larger keepers; however, this will increase delay and power consumption

Hybrid NEMS-CMOS Dynamic OR Gates



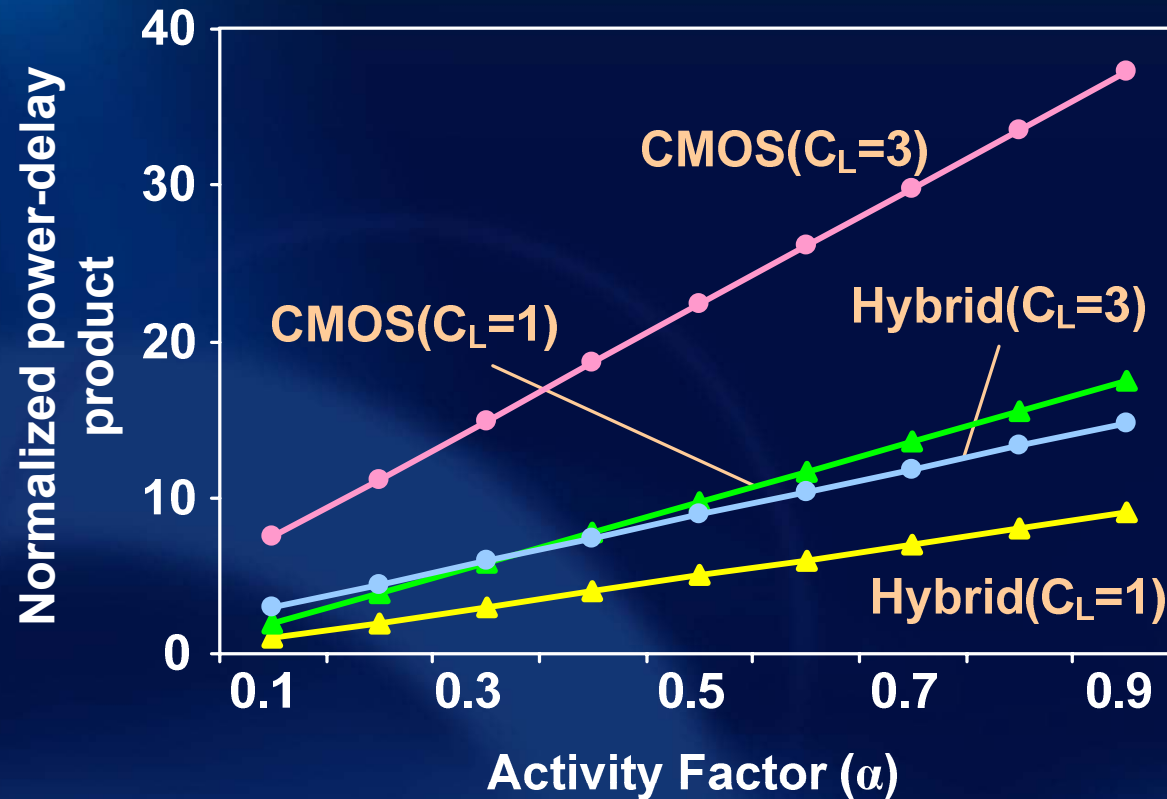
- **SG-MOSFET devices reduce leakage and hence, allows us to use minimal-size keeper in the hybrid architecture**

Dynamic OR Gates Simulation Results



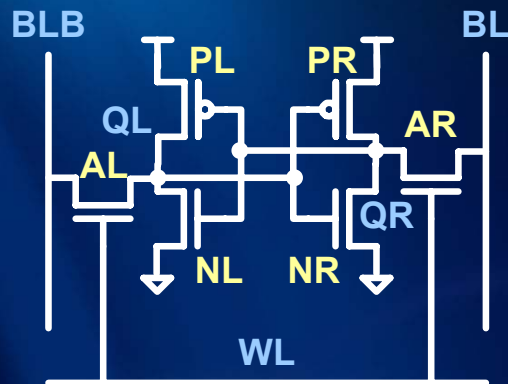
- Dynamic OR gates can achieve 60-80% lower switching power
- For high fan-in values, the hybrid gate outperforms the CMOS gate in terms of both delay and power consumption

Dynamic OR Gates Simulation Results

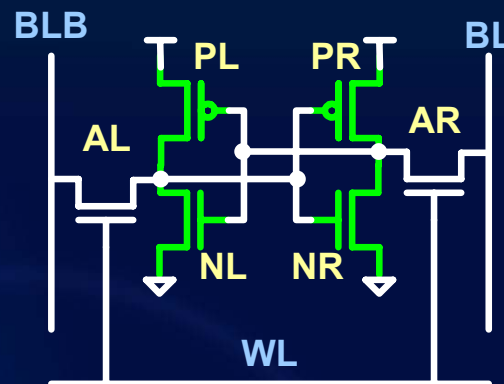


- The hybrid gates have lower power-delay product over entire range of activity factor.

Different Low-leakage SRAM Cell Designs

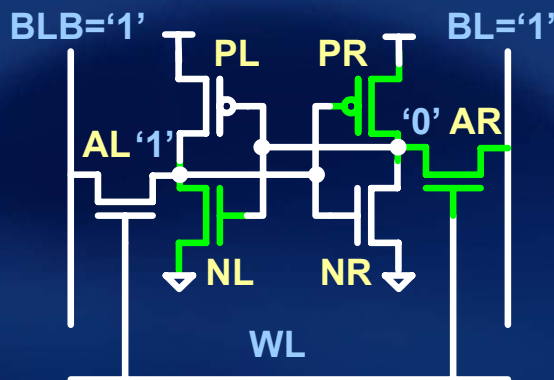


Conventional CMOS Cell



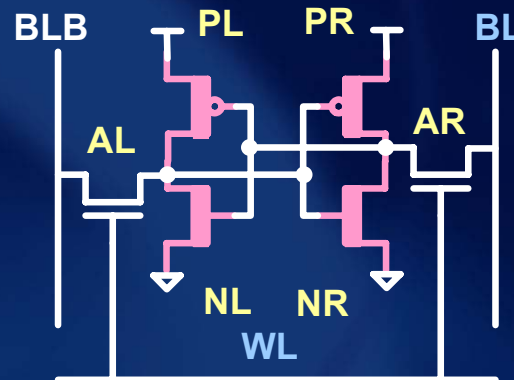
Dual V_t Cell

Hamzaoglu, et al. *ISLPED2000*



Asymmetric Cell

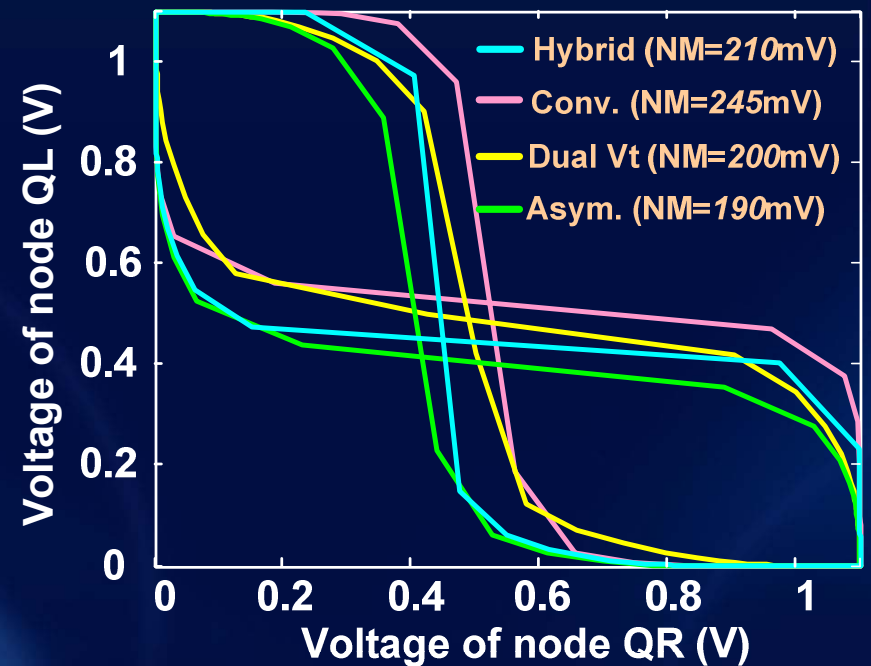
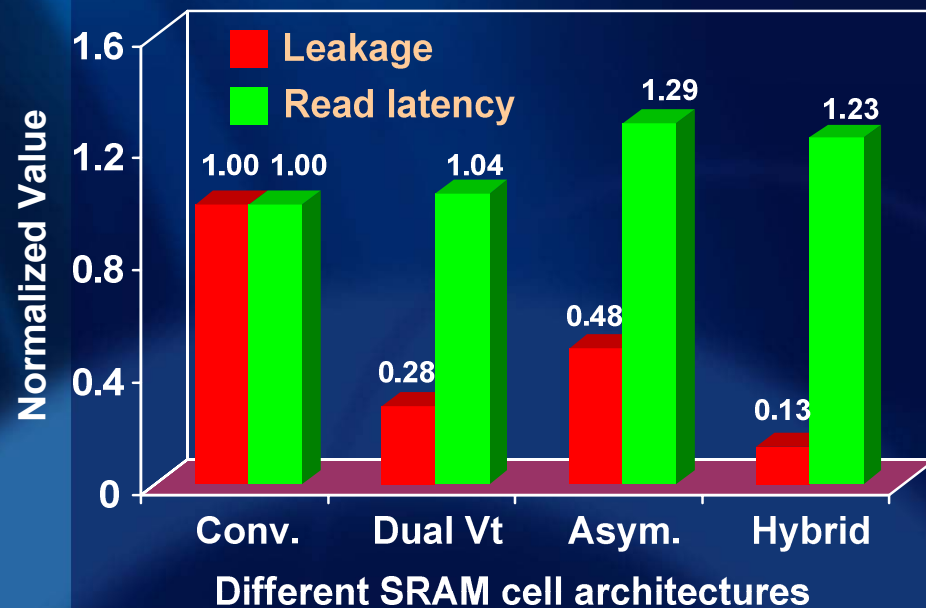
Azizi, et al. *DAC 2006*



Hybrid NEMS-CMOS Cell

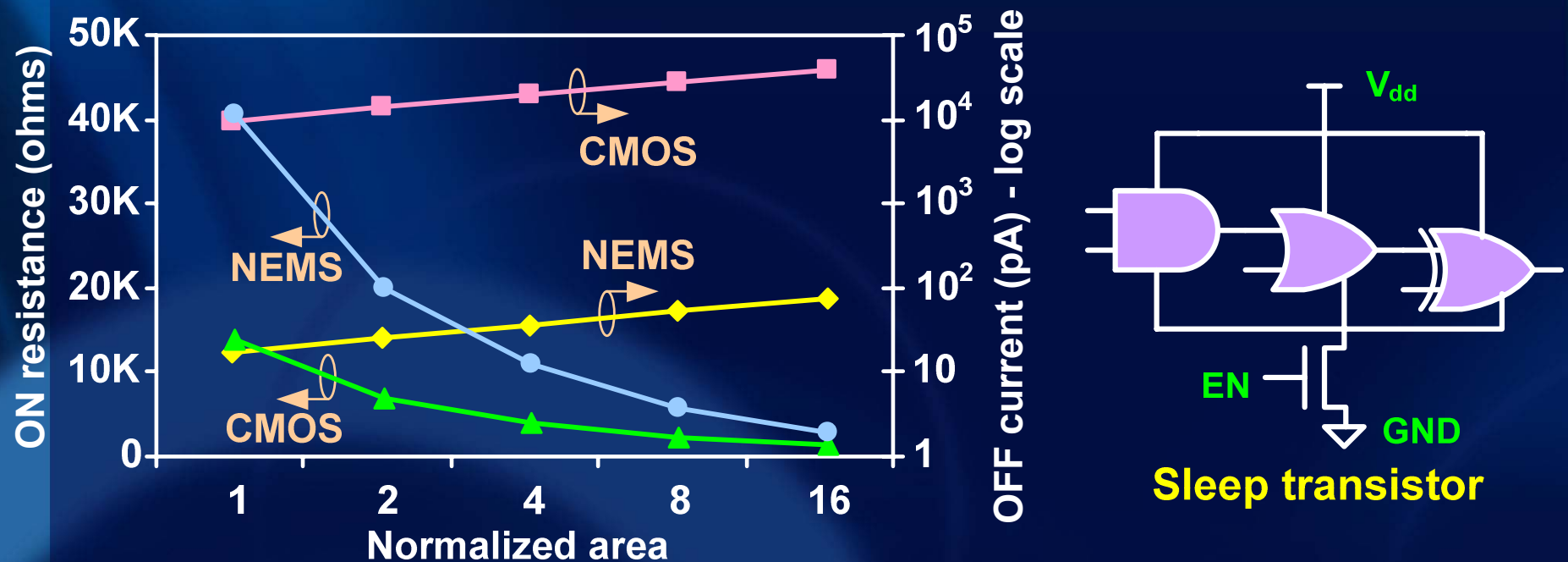


SRAM Cell Simulation Results



- Hybrid SRAM cell has nearly **8X lower** leakage
- Hybrid cell offers higher noise margin than Asym. And Dual- V_t architectures

Sleep Transistor Simulation Results



- For the same area, NEMS sleep transistors offer **three orders of magnitude lower OFF current**
- NEMS sleep transistors have slightly higher ON resistance

Conclusions

Contributions of this paper, we:

1. Proposed the idea of hybrid NEMS-CMOS technology
2. Showed that Hybrid NEMS-CMOS:
 - *Dynamic OR gates can achieve 60-80% lower switching power and for high fan-in values, the hybrid gate outperforms the CMOS gate in terms of both delay and power consumption*
 - *SRAM cell can have nearly 8X lower standby leakage power*
 - *Sleep transistors offer up to three orders of magnitude lower OFF current*