# *ECE 225*
# *High Speed Digital IC Design*
# *Lecture 6*

## Interconnect Technology and Scaling Issues-III (Inductive Effects, Voltage Drop, and Parameter Variations)

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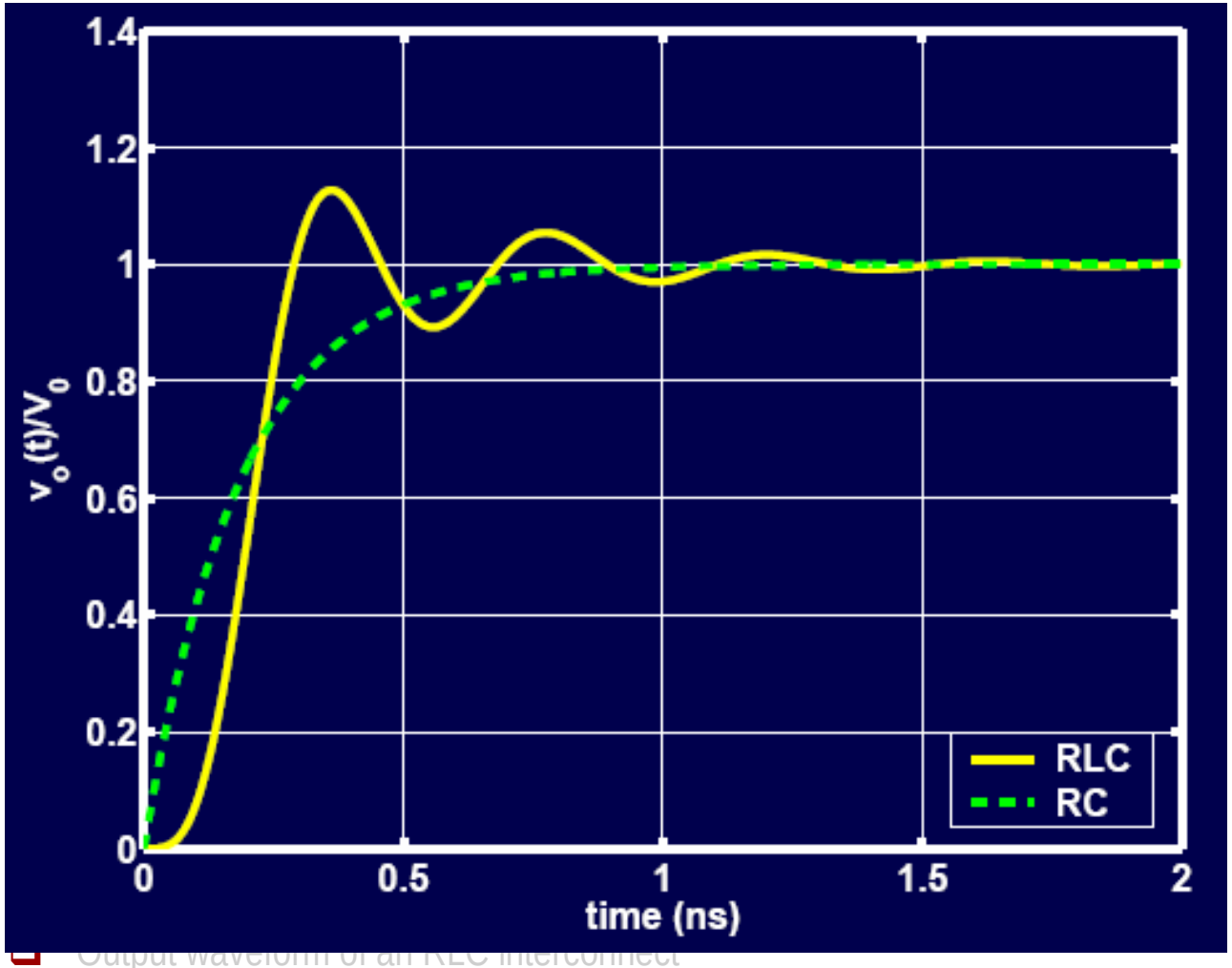
# On-Chip Inductance Effects

**K. Banerjee and A. Mehrotra, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 21, No. 8, pp. 904-915, August 2002.**

# On-Chip Inductance Effects

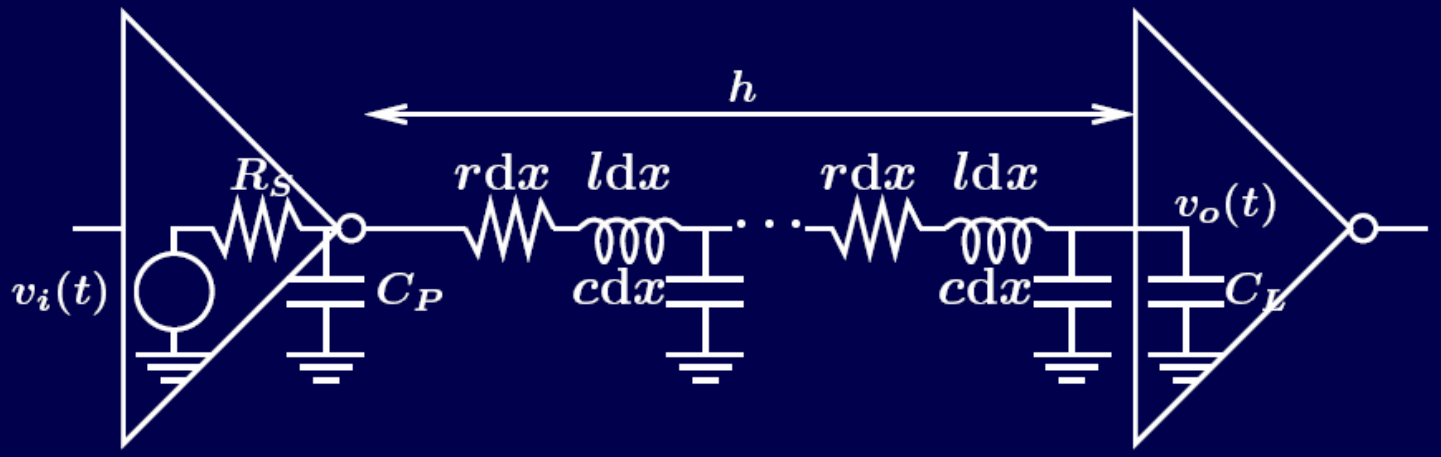
- Increasing clock speeds and decreasing rise times cause inductive effects
- Low resistance wires more susceptible to inductive effects
  - Global wires that are usually wide
  - introduction of Cu: lower resistivity
- Line inductance depends on current return path
  - strongly dependent on circuit topology
  - difficult to extract accurately
  - large variations

# Step Response of an RLC Line




Output waveform of an RLC interconnect

# Time-Domain Response of RLC Segment




$$H(s) = \frac{1}{[1+sR_S(C_P+C_L)]\cosh(\theta)+\left[\frac{R_S}{Z_0}+sC_LZ_0+s^2R_SC_PC_LZ_0\right]\sinh(\theta)}$$

$$\approx \frac{1}{1+sb_1+s^2b_2+s^3b_3+s^4b_4}$$

$$Z_0 = \sqrt{\frac{r+sl}{sc}} \qquad \theta = \sqrt{(r+sl)sch}$$

# Critical Inductance

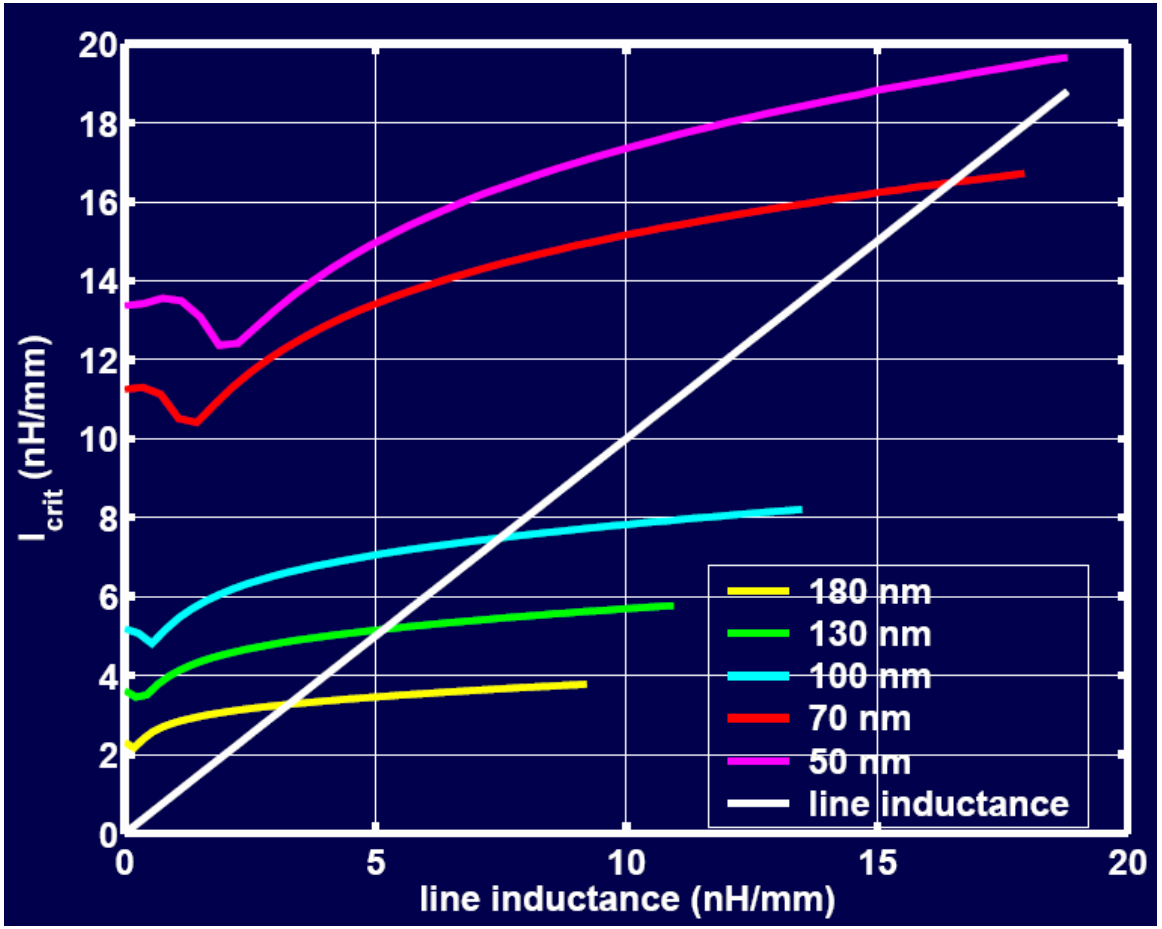
- Second order Padé expansion of $H(s)$

$$H(s) \approx \frac{1}{1 + b_1 s + b_2 s^2}$$

- System overdamped, critically damped or underdamped when $b_1^2 - 4b_2$ is $>, =, < 0$.
- At optimum buffer size and interconnect length, find $l_{crit}$ for which the system is critically damped.
- For $l$ $<, =, >$ $l_{crit}$, the system is overdamped, critically damped or underdamped

# Impact of Scaling: Case 1

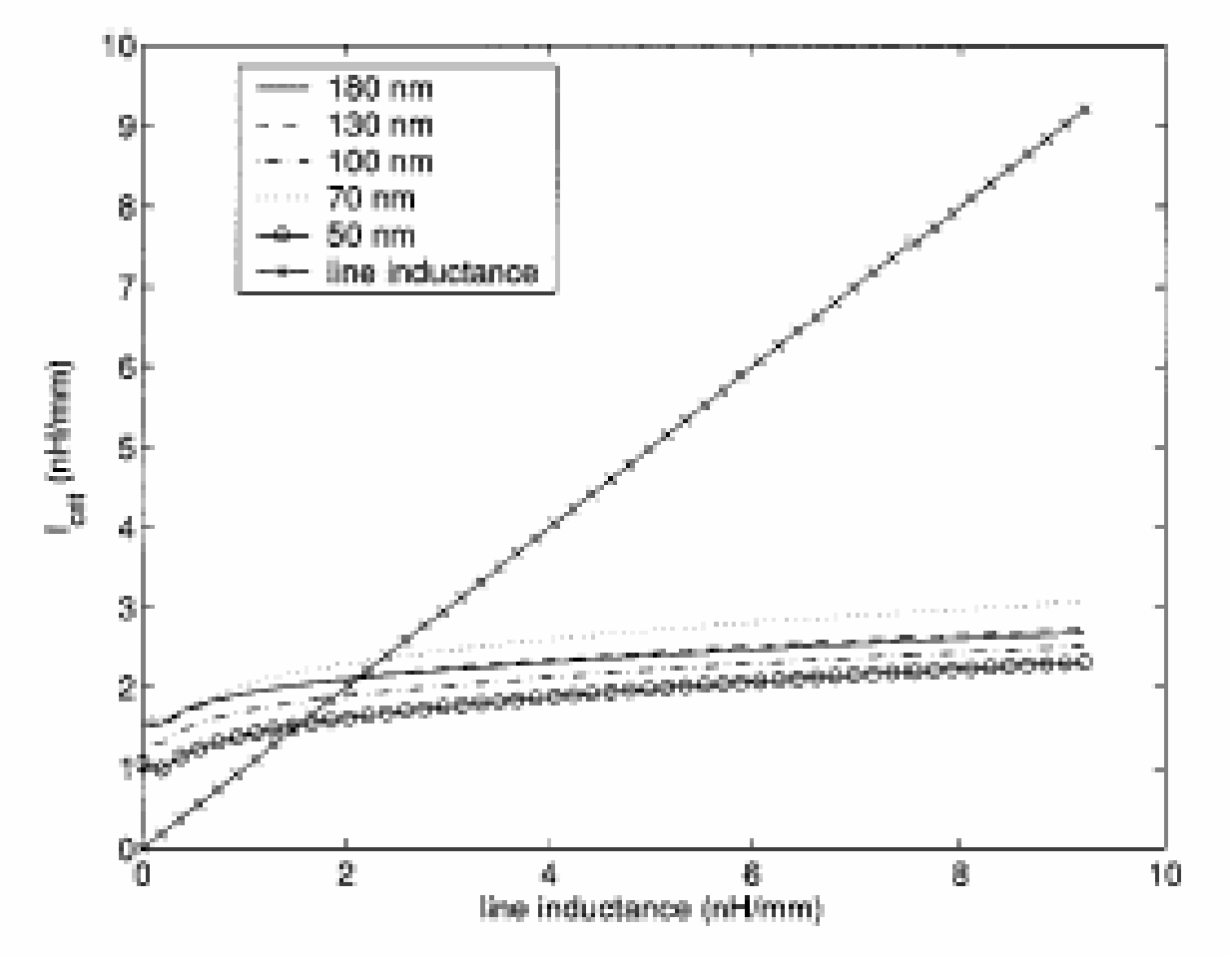
## Minimum Width Global Wires




- As technology scales, $l < l_{crit}$ over larger range of line inductance
- Hence, impact of inductance reduces with scaling

# Impact of scaling: Case 2

## Unscaled Global Wires




- As technology scales, $l > l_{crit}$ over larger range of line inductance
- Hence, impact of inductance increases with scaling

# Voltage Drop Effects in Power Distribution Networks

**A. H. Ajami, K. Banerjee and M. Pedram, International Journal of Analog Integrated Circuits and Signal Processing, Vol. 42, No. 3, pp. 277-290, Springer, 2005.**

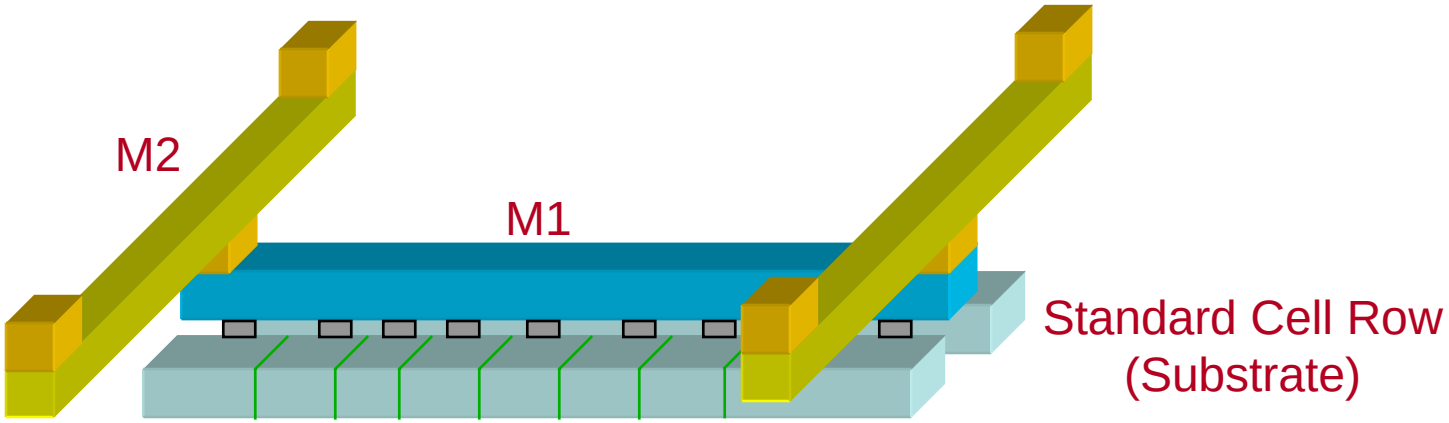
# Voltage Drop Effects

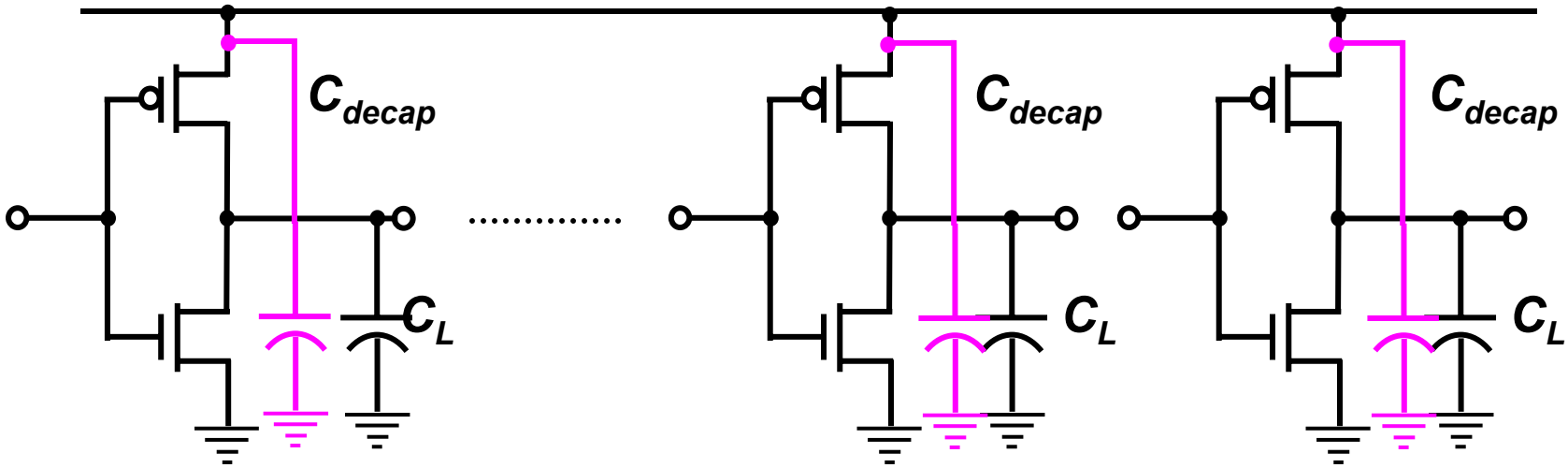
- Voltage-drop is an inseparable aspect of DSM power distribution network (PDN)
  - resistive voltage drop $\Delta V$ (on-chip resistance)
  - switching noise, $L di/dt$ (off-chip inductance)
- Degrades device switching speed and *DC* noise margins
- Can cause functional failure in dynamic logic and timing violation in static logic
- 10% voltage-drop → 8% increase in device propagation delay (0.18μm tech.)

# Challenges in P/G Network Design

- Satisfying the electromigration (EM) rules for each power routing segment
- Minimizing the area consumed by PDN
- Limiting the worst-case voltage-drop (~10% of *Vdd* for current technology)
  - Power network wire-sizing (↑ routing area)
  - Decoupling-cap insertion (↑ substrate area)

# Local Power Distribution



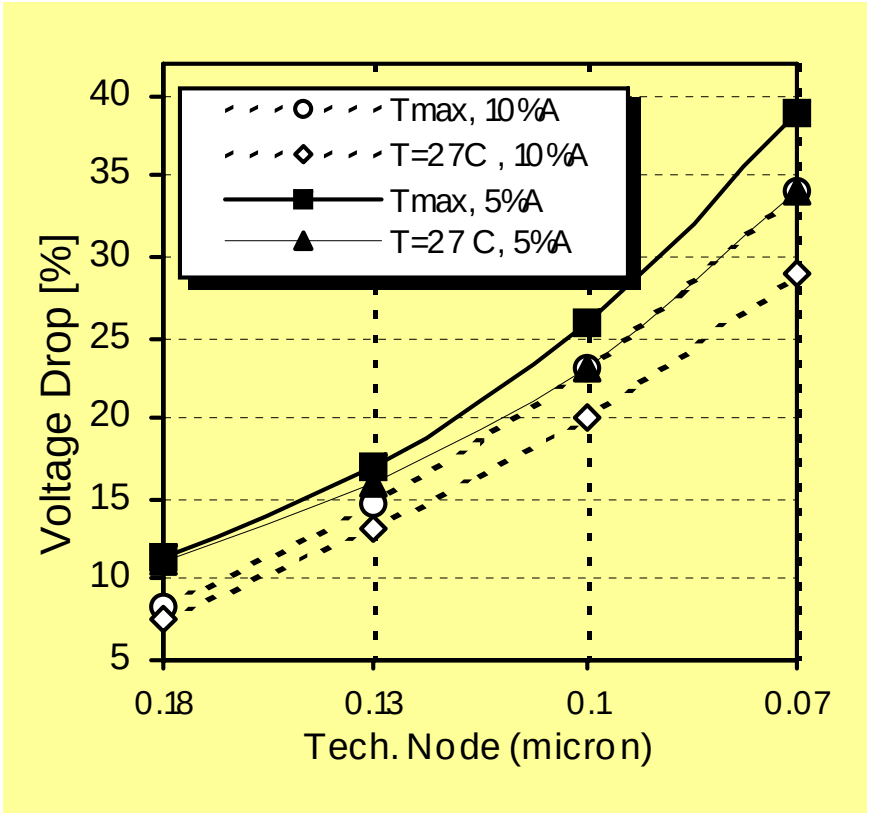



# Technology Scaling Impacts

- Scaling of line dimension (*R*, *L*, *C*)
- Scaling of chip frequency, power, and # of power pads
- Interconnect thermal effects
  - Electromigration rules
  - R
- Thin-film scattering and barrier thickness effects in DSM interconnects
  - R

# Global/Semi-global PDN IR-Drop

Allocation of 5% and 10% of the routing area for wire sizing to minimize the voltage-drop:

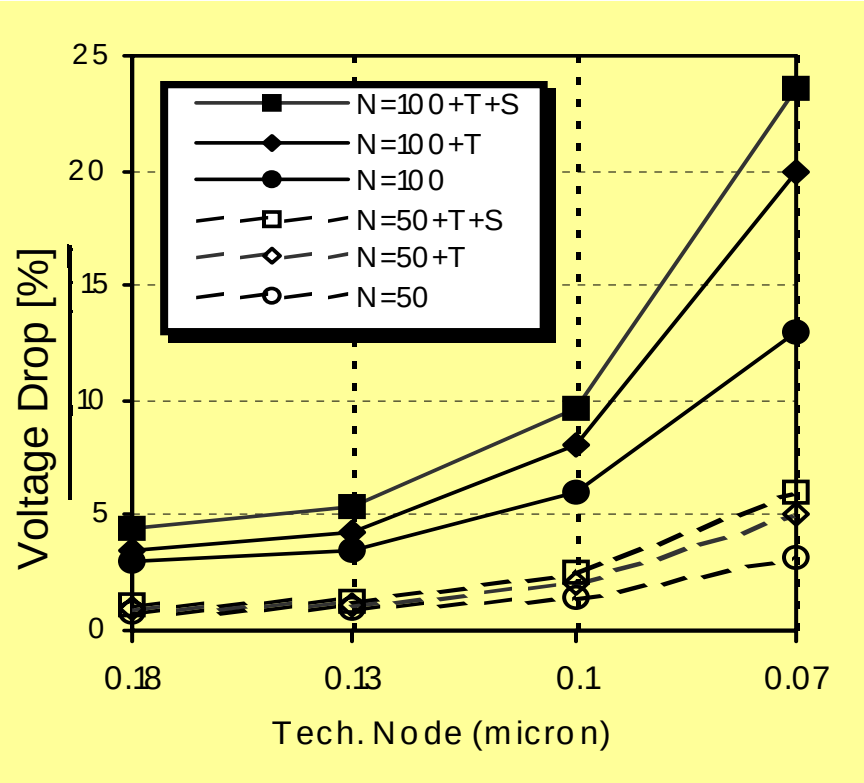



**Voltage-drop increases rapidly with technology scaling….**

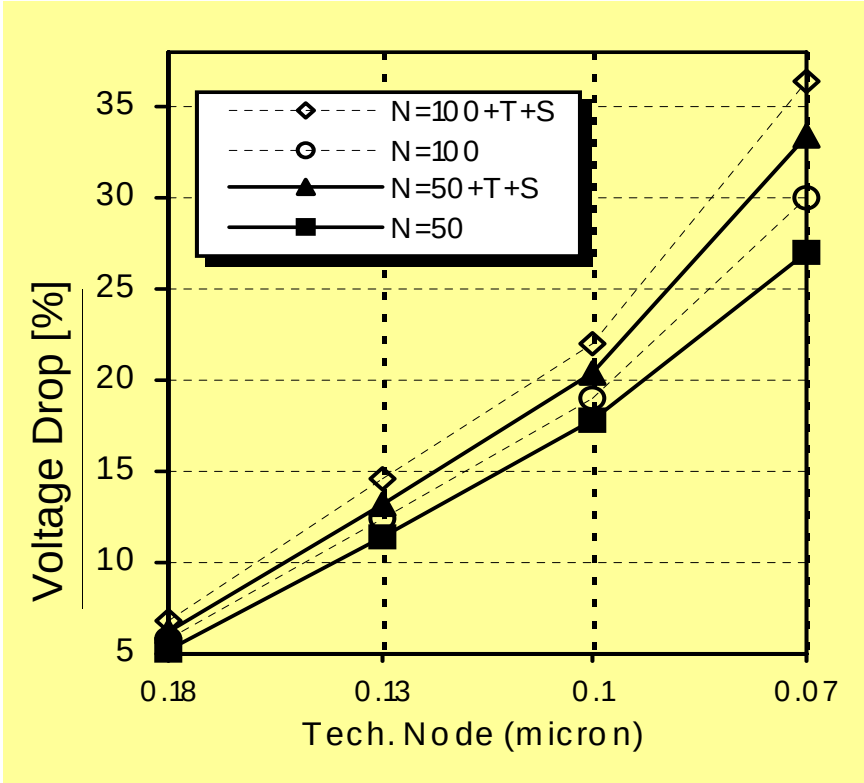
**Interconnect temperature has a major impact on the voltage-drop of global segments…..**

# Full Chip IR-Drop

Local worst-case IR-Drop
for 50 and 100 switching cells




Total chip worst-case IR-Drop
10% routing, 5% chip area



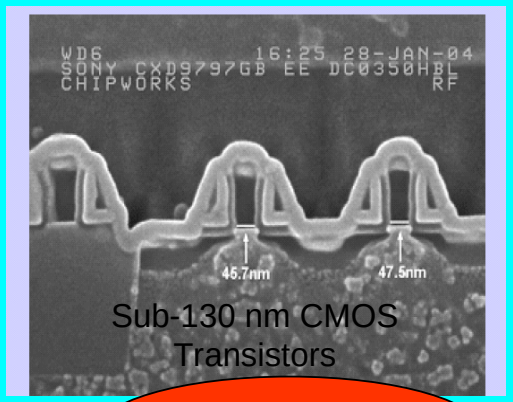

**T– considering temperature effect** **S—considering thin-film effects**

# Implications of Parameter Variations

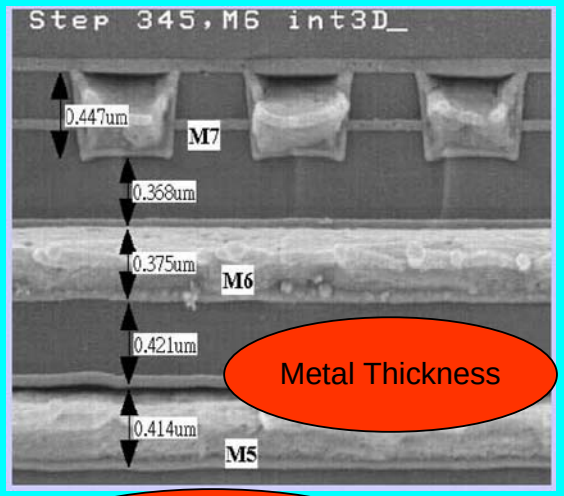
**V. Wason and K. Banerjee, IEEE International Symposium on Low Power Electronic Design (ISLPED), 2005, pp. 131-136.**

**A. H. Ajami, K. Banerjee and M. Pedram, IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol. 24, No. 6, pp. 849-861, 2005.**

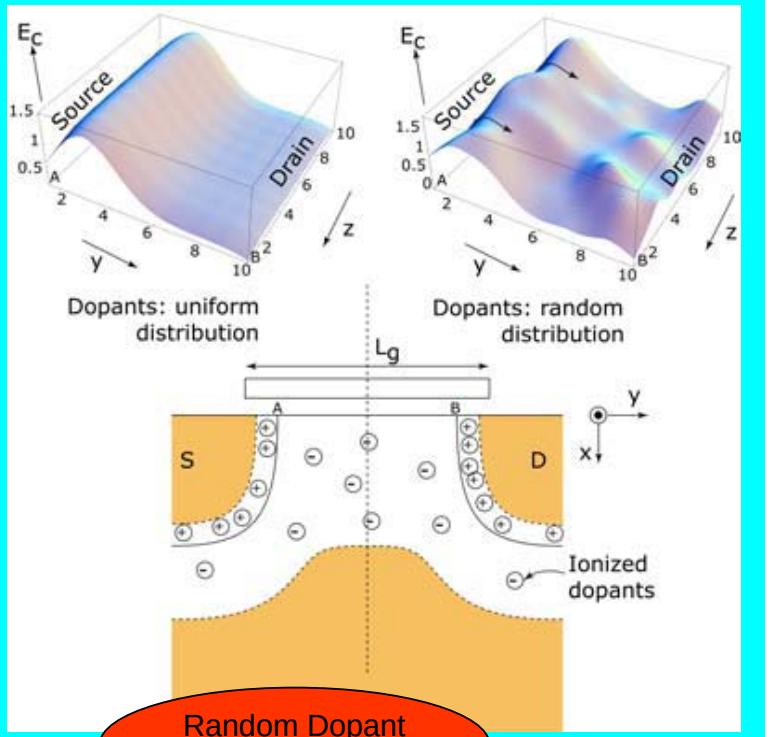
# Parameter (P-V-T) Variations




Transistor channel length

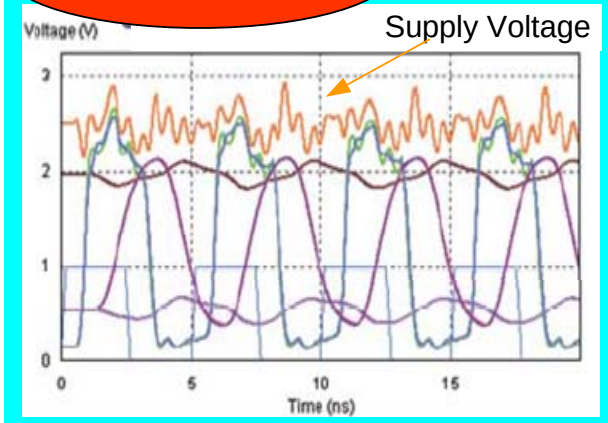



Metal Thickness

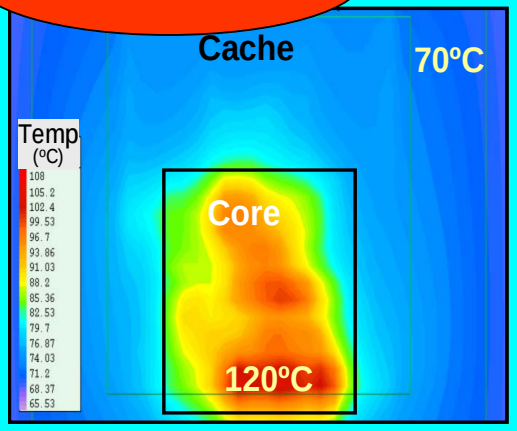



Random Dopant Fluctuations

Power Supply Voltage

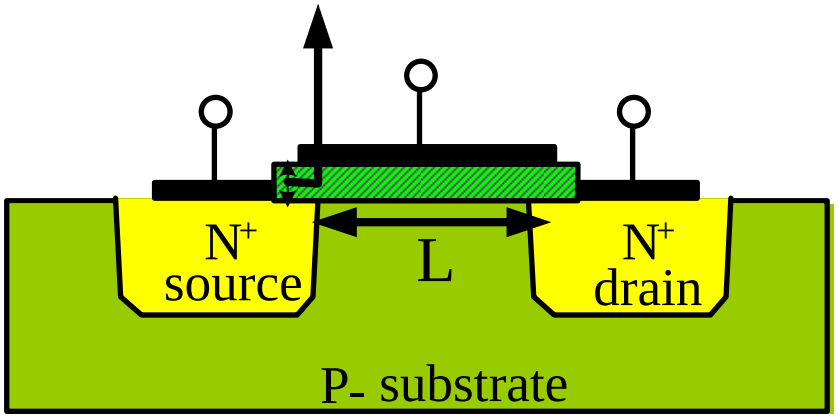


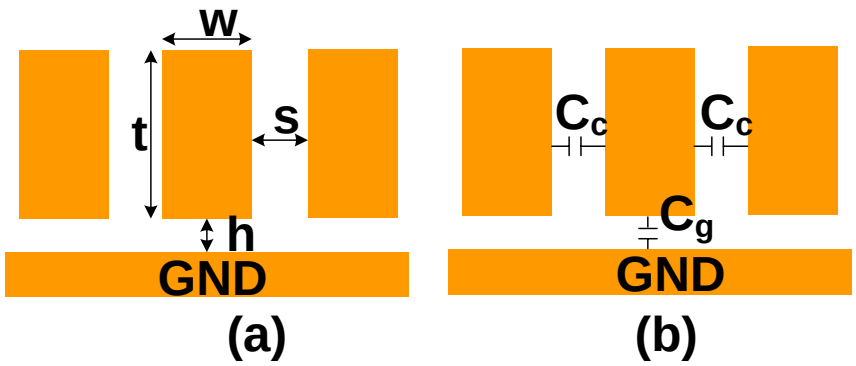

Chip Temperature



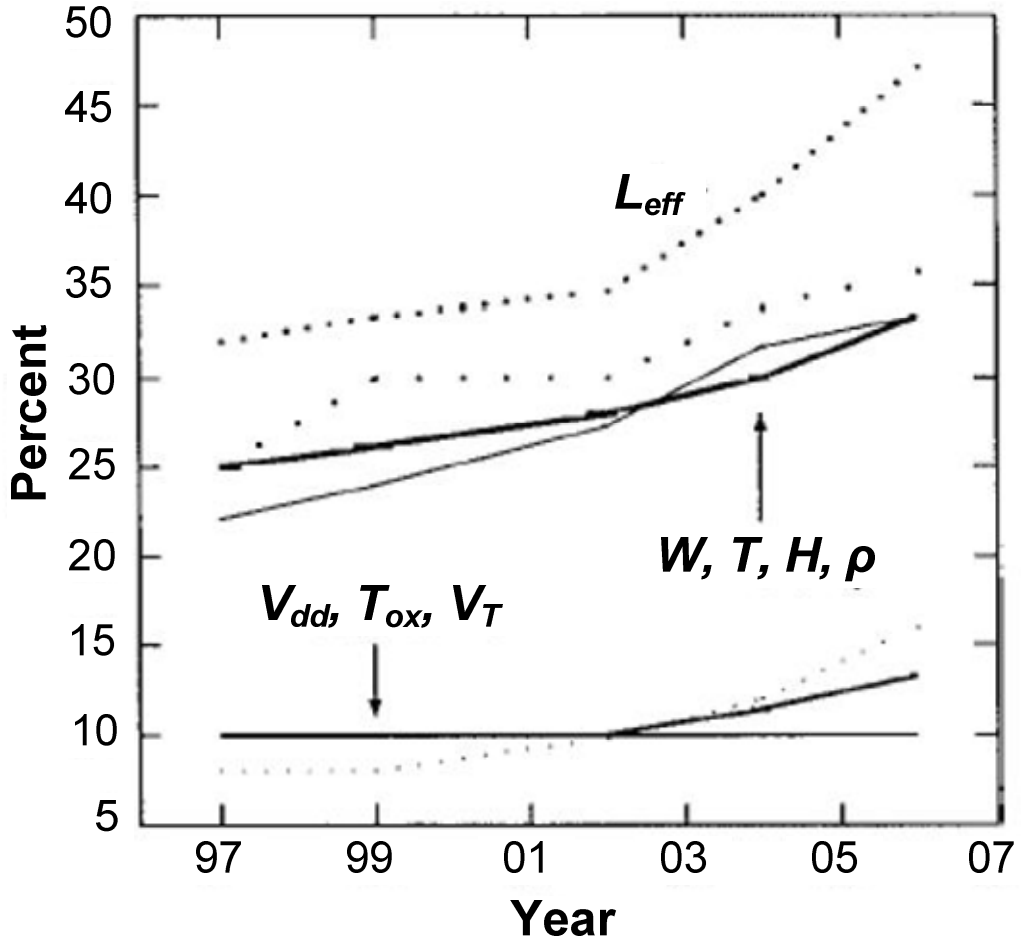
# Process Variations

- Device Variations
  - Channel Length (L)
  - Oxide Thickness ($t_{ox}$)
  - Dopant Density ($N_a$)
- Interconnect Variations
  - Line Width (w)
  - Spacing (s)
  - Metal Thickness (t)
  - Dielectric Thickness (h)



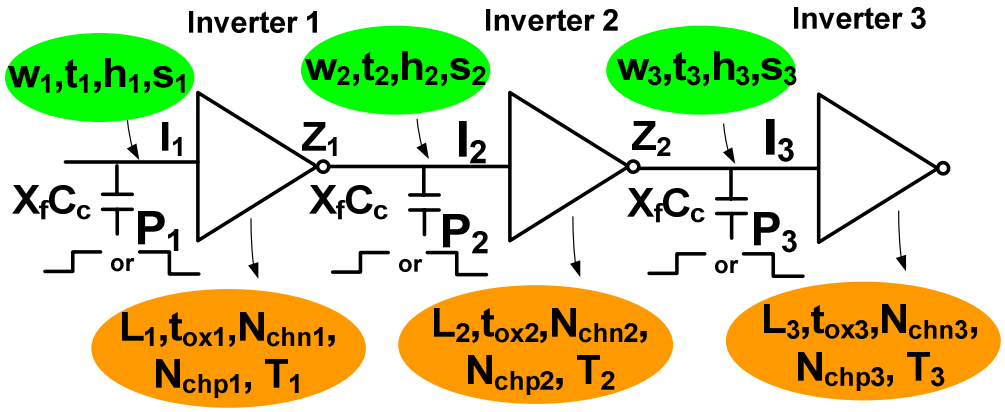



# Device vs. Interconnect Variations



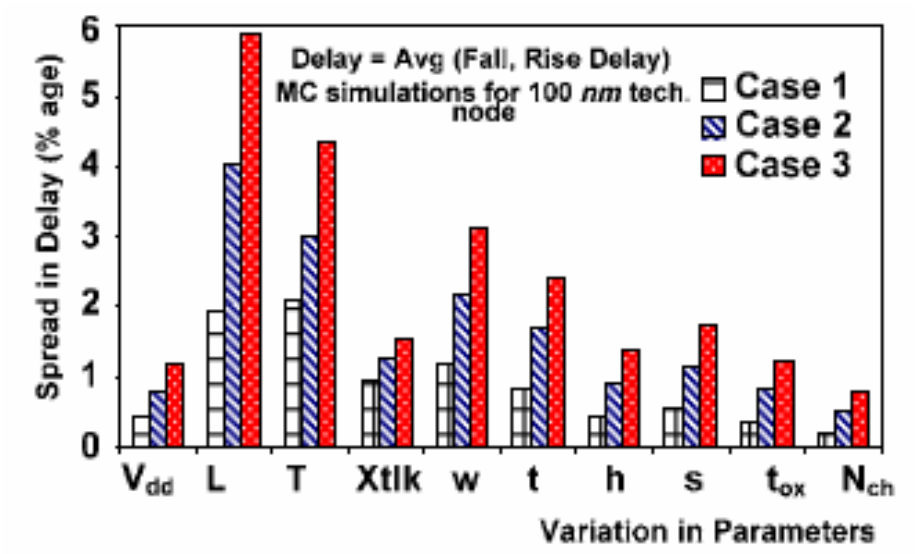

S. Nassif (IBM)

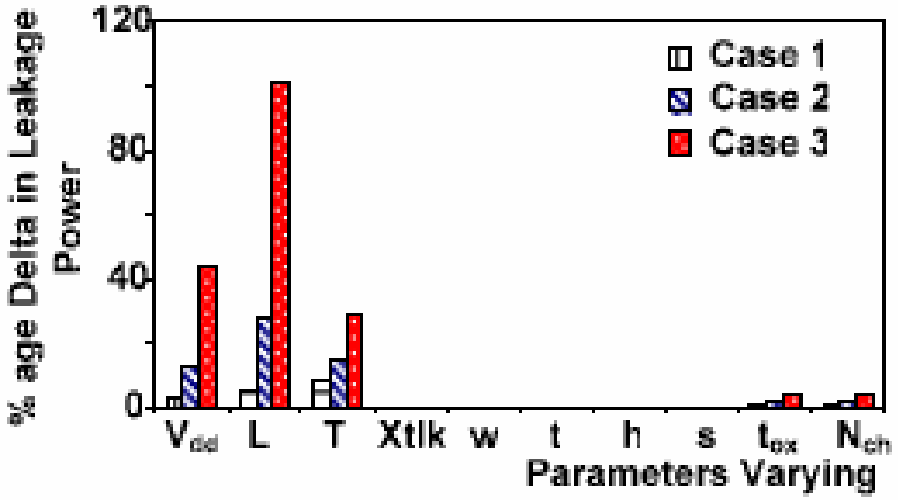
# Sensitivity Analysis of Delay and Power




3 cases considered;
% variations increase from case 1 to case 3

**Wason and Banerjee, ISLPED 2005**

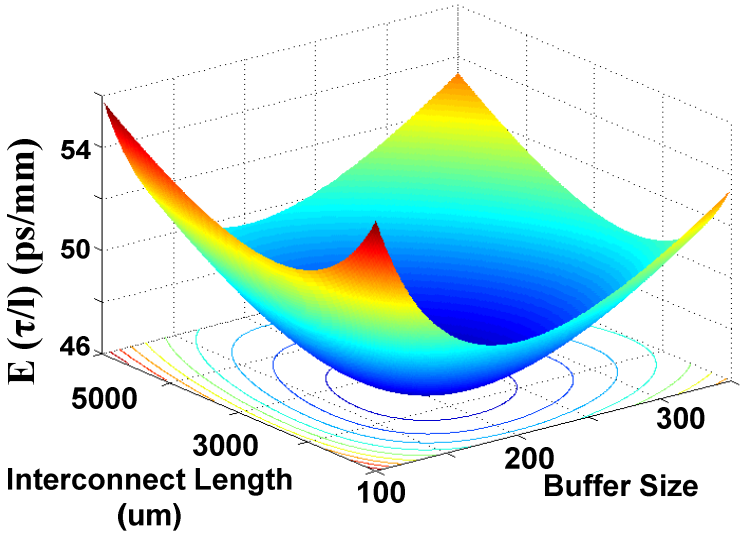


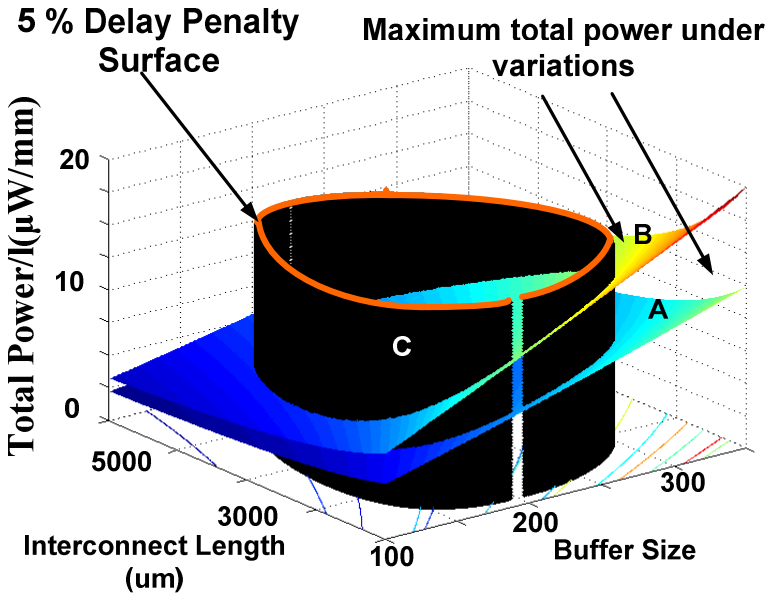




- Variations have significant impact on leakage power and delay

# Interconnect Design Considering Variations

- Significant Implications for Interconnect Design
- Power-Optimal Repeater Insertion- tradeoff delay with power

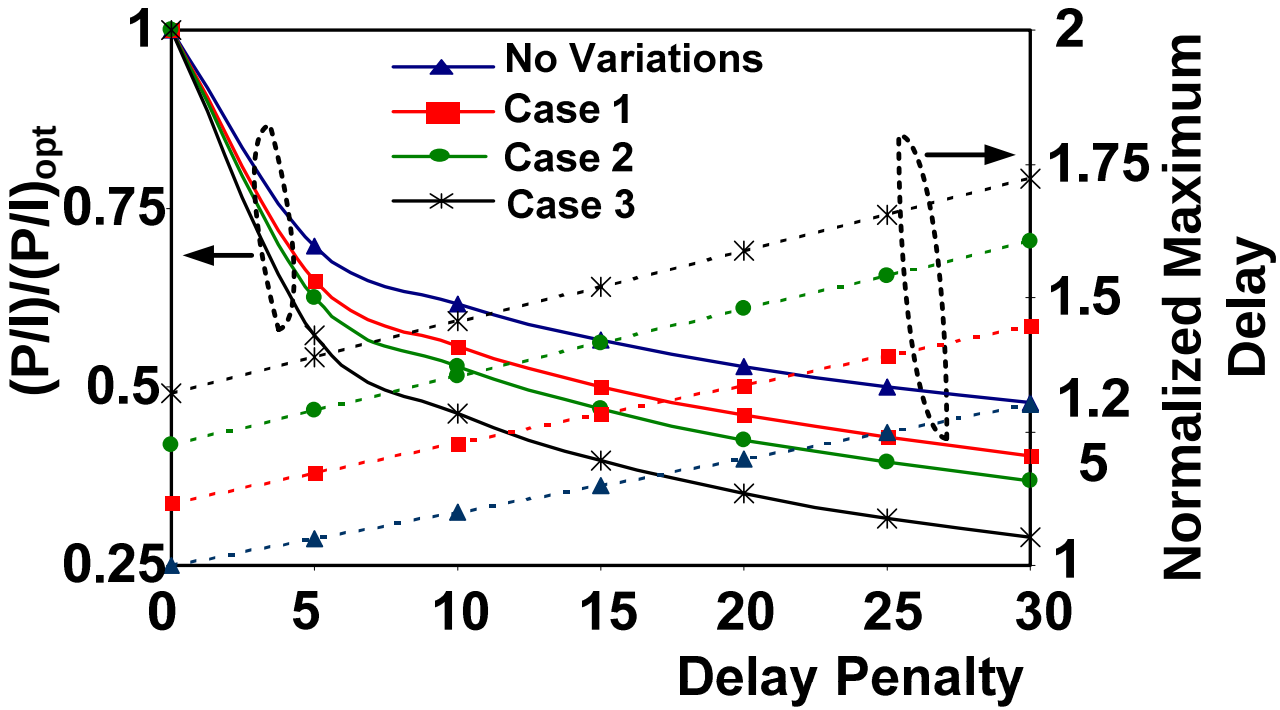



**Wason and Banerjee, ISLPED 2005**

Variations can significantly impact power-optimal repeater insertion

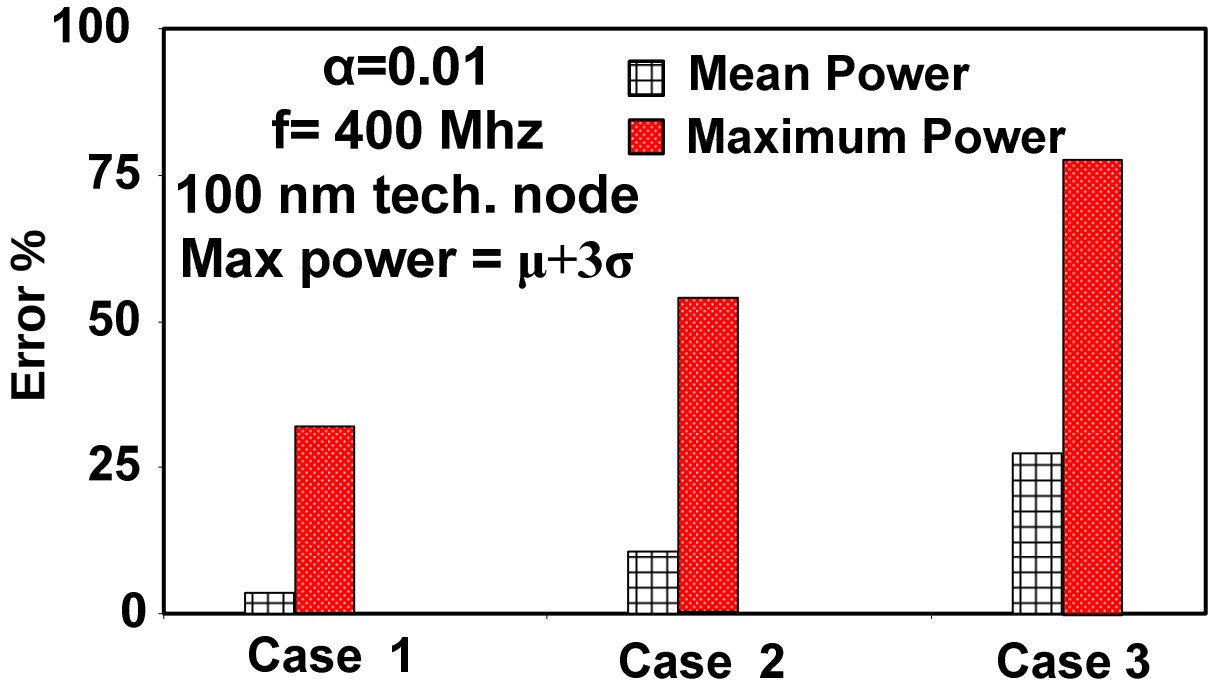
# Optimization under Parameter Variations




Wason and Banerjee, ISLPED 2005

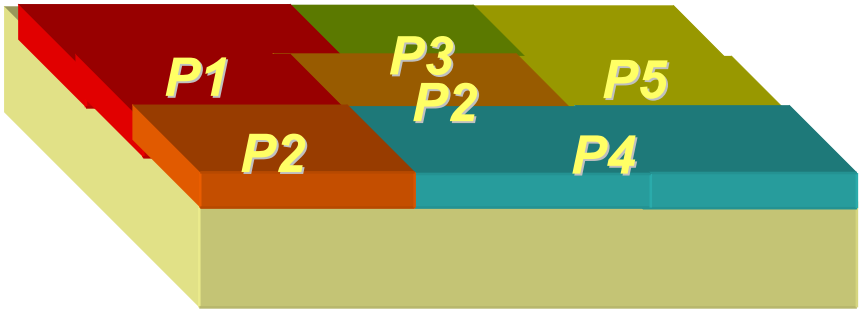
- The normalized delay increases under variations
- Power savings are higher for the same penalty in delay, as variations increase
- Importance of power-optimal repeater insertion increases

# Implications for Power Estimations




- Error in power estimation can be significant if variations are neglected

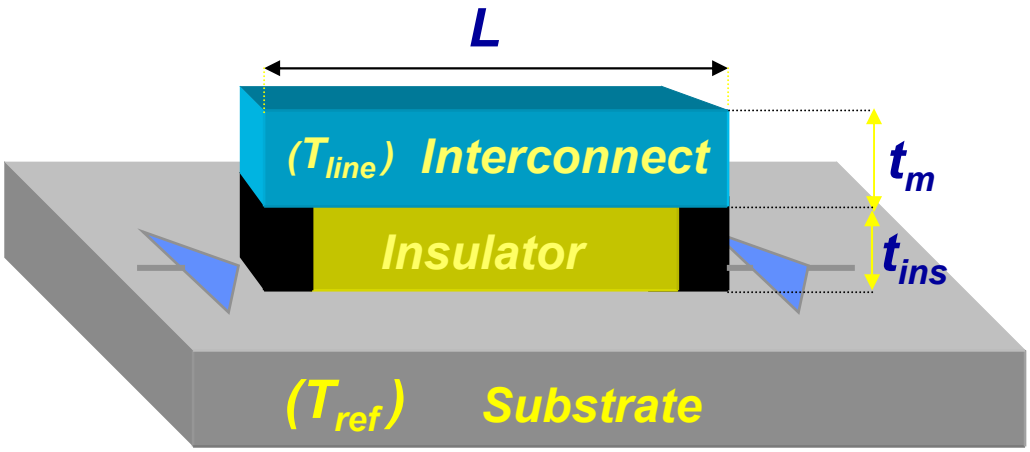
# Within-Die Temperature Variations

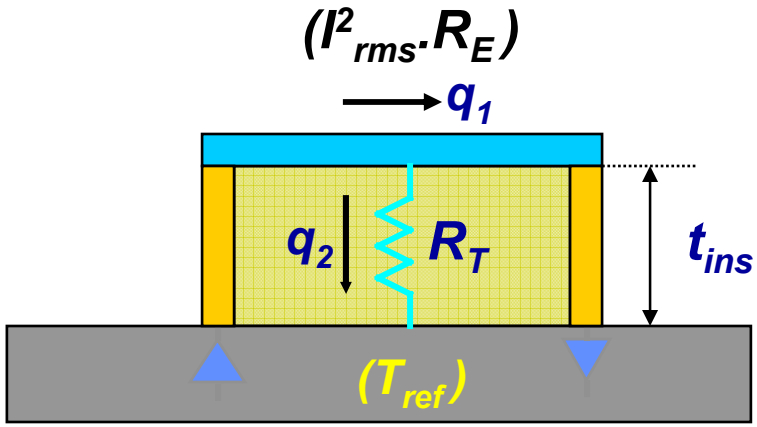



- Substrate power generation distribution is generally non-uniform
  - Functional block clock gating
  - System-level power management
  - Non-uniform distribution of gate sizing and switching activities in different blocks
- Substrate thermal profile is non-uniform
  - Thermal time constant is of the order of *ms*
  - Switching activities at the block level are more important
  - Introduces non-uniformity in the global interconnect thermal profile

# Interconnect Thermal Profile

A. Ajami et al., DAC 2001




$$\frac{d^2T_{line}}{dx^2} = -\frac{Q}{k_m}$$

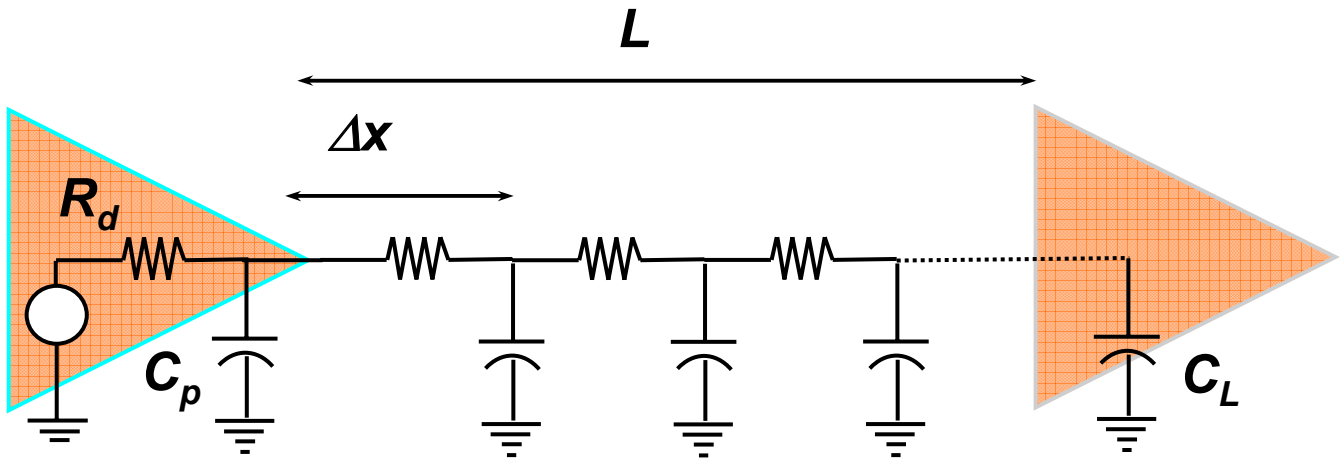
$$Q = q_1 - q_2$$

$$\frac{d^2T_{line}(x)}{dx^2} = \lambda^2 T_{line}(x) - \lambda^2 T_{ref}(x) - \theta$$

$\lambda$ and $\theta$ are constants

$f(L, t_m, k_m, t_{ins}, k_{ins}, I_{rms}, R_E)$

# Non-Uniform Temperature-Dependent Delay




$$D = R_d(C_P + C_L + \int_0^L c_0(x)dx) + \int_0^L r_0(x)(\int_x^L c_0(\eta)d\eta + C_L)dx$$

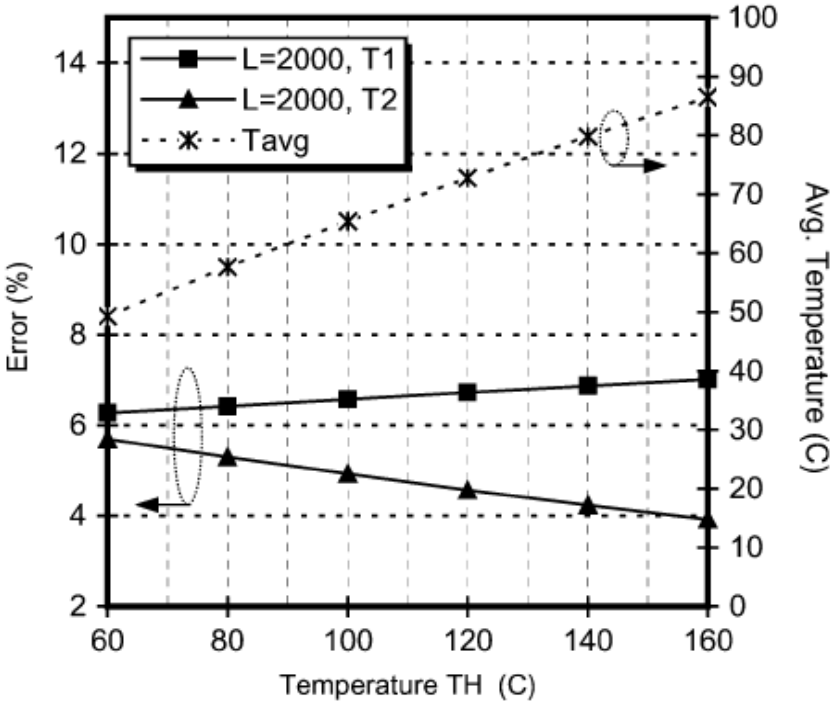
$$D = D_0 + (c_0 L + C_L)\rho_0\beta\int_0^L T(x)dx - c_0\rho_0\beta\int_0^L xT(x)dx$$

**$D_0$ is the Elmore delay model at reference temp.**

# Implications for Delay and IR-Drop

## Impact on delay estimation…..

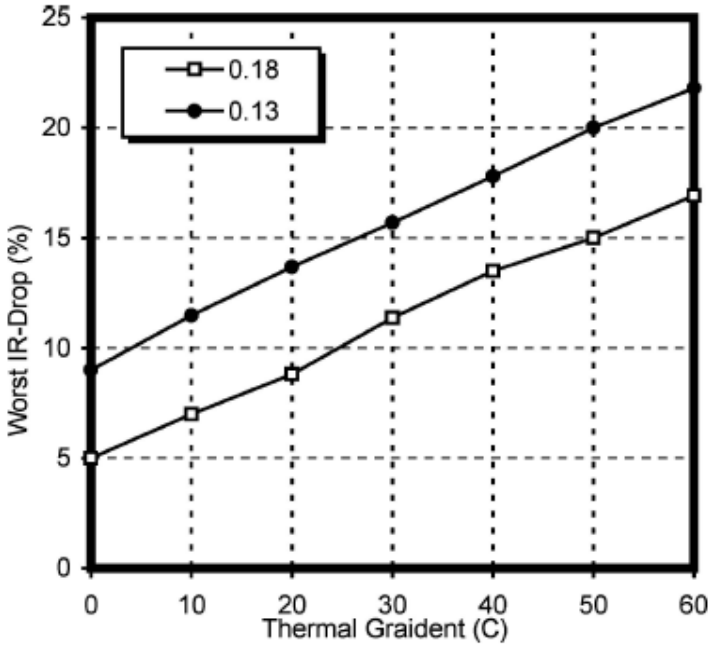
**T1: positive exponential gradient**
**T2: negative exponential gradient**
**For a fixed T_Low**




**Ajami et al., TCAD 2005**

## Impact on IR-drop analysis…..

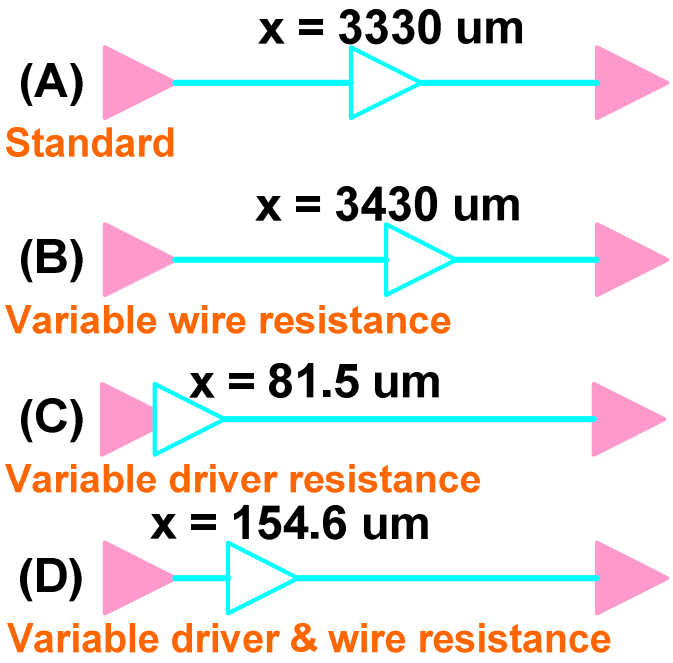
**Worst-case voltage-drop ($V_{IR}/V_{dd}$) increases in the presence of thermal gradients**



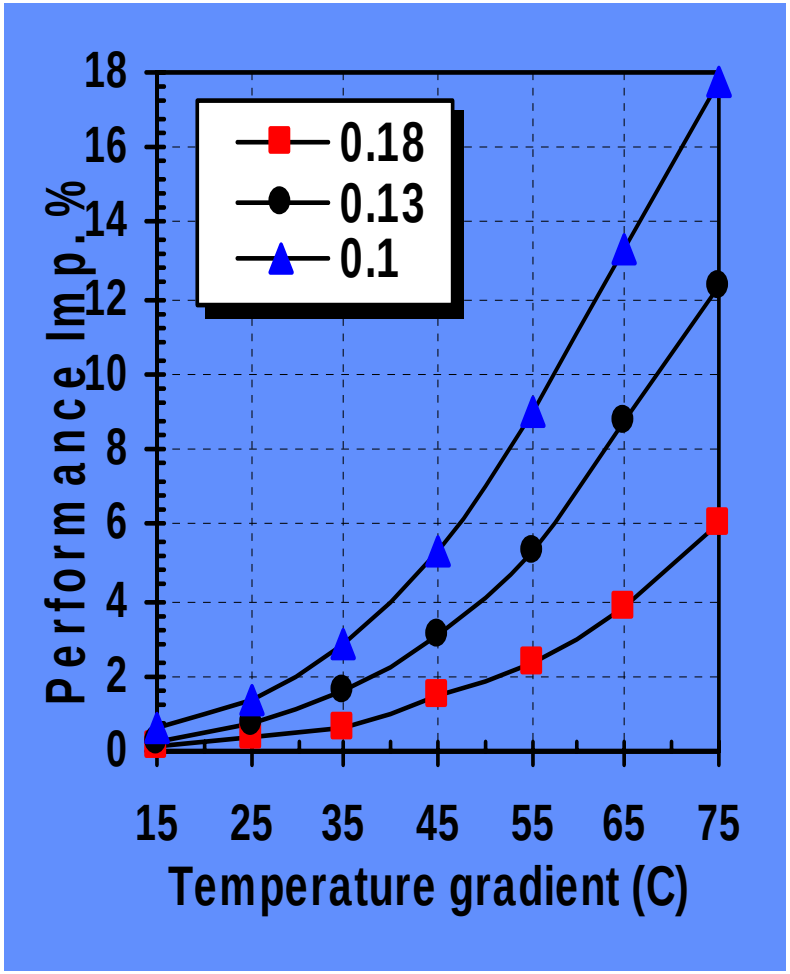

**Ajami et al., JAICSP, 2005**

# Impact on Buffer Insertion

**Buffer movement in a 6660 um line (180 nm node)**




**Delay improvement after thermally-aware buffer insertion**




Ajami et al., ICCAD 2001