ECE 225
High Speed Digital IC Design
Lecture 7

Interconnect Technology and Scaling Issues-IV
(High-Frequency Effects, Emerging Technologies)

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High-Frequency Issues

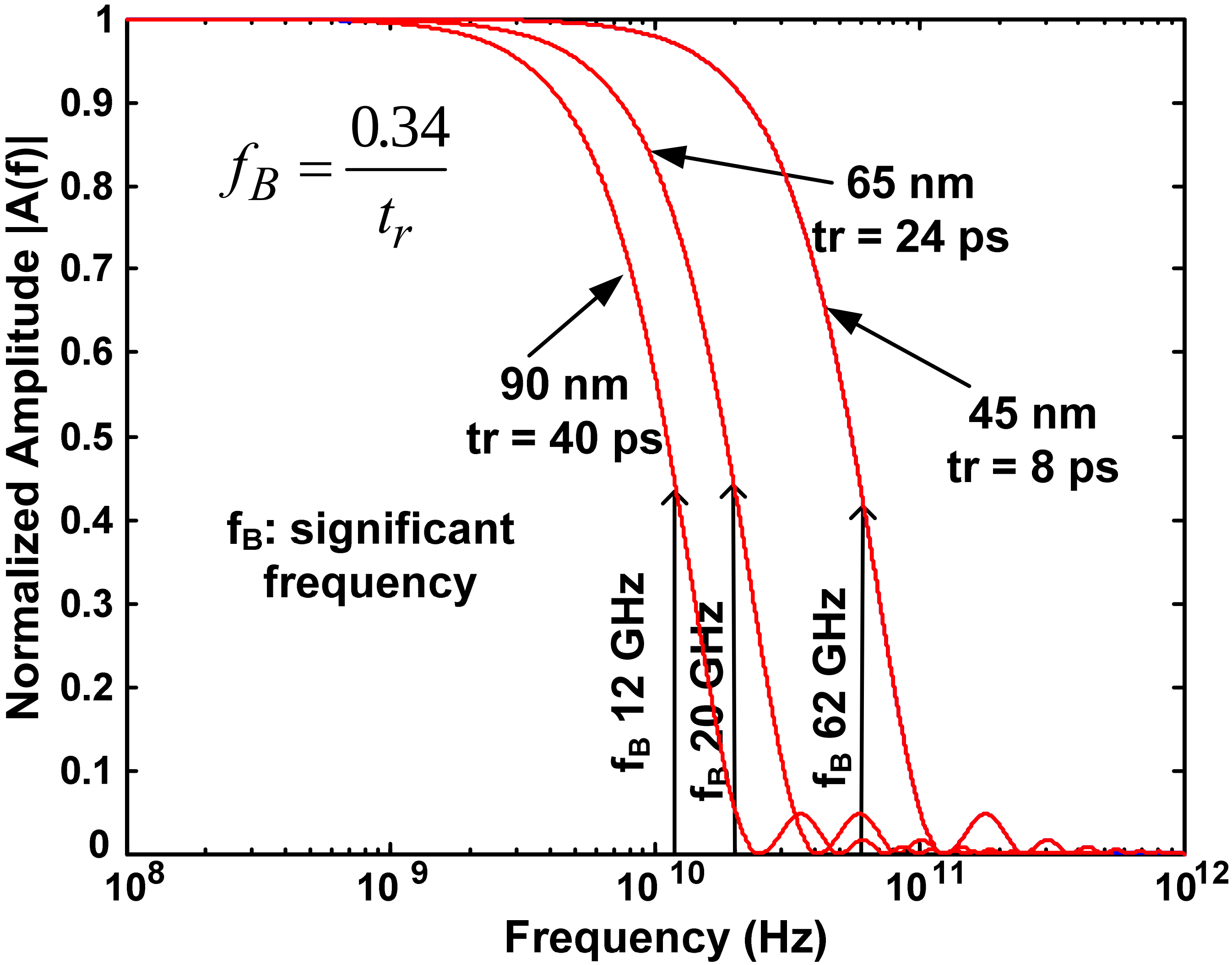
K. Banerjee, S. Im and N. Srivastava, Proc. Advanced Metallization Conf., 2005.

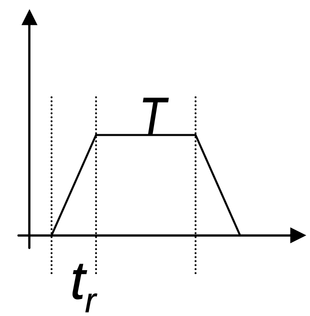
S. Suaya, R. Escovar, S. Ortiz, K. Banerjee and N. Srivastava, Proc. Advanced Metallization Conf., 2006.

High-Frequency Effects

- Frequency of signals on interconnects is rising rapidly
- Frequency dependent impedance extraction is a major hurdle
  - Field solvers are unable to handle the complexity of VLSI interconnects
- Need to develop models for interconnect geometry dependent calculation of high frequency impedance

Signal Frequency on Interconnects





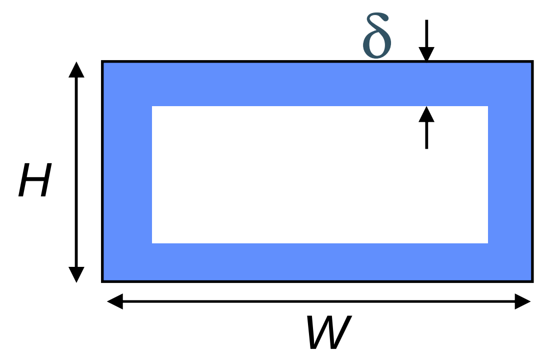
Digital signal composed of various frequency components.

Significant Frequency:

Frequency used for interconnect analysis

Frequency Dependence of R

- **At high enough frequencies, R can increase due to** *skin effect*
- **Current flow constrained in a thin layer along the surface of the conductor:** R increases
- **The current falls off exponentially with depth into the interconnect**
- Skin depth**,** δ **is defined as the depth at which current falls of to a value of 1/e of its nominal value**



$$\delta = \sqrt{\frac{\rho}{\pi f \mu}}$$

μ is the permeability of the surrounding dielectric

Resistance per unit length:

$$r(f) = \frac{\sqrt{\pi f \mu \rho}}{2(H+W)}, \quad for\ \ W, H >> \delta$$

Skin Effect

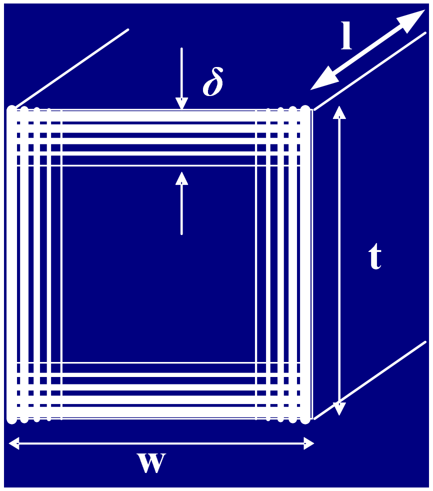
- Onset of skin effect: at $f=f_s$, δ =1/2 x smallest dimension

$$f_s = \frac{4\rho}{\pi\mu(\min(W,H))^2}$$

- For Cu wires:

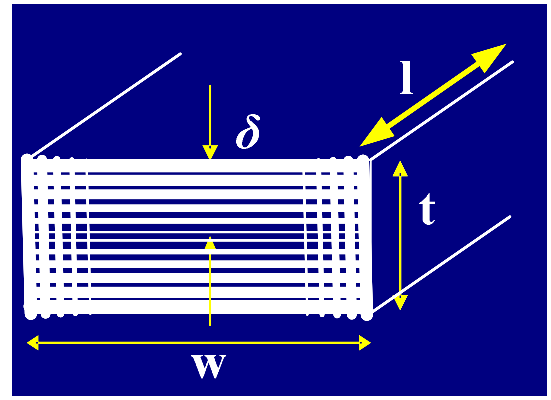
Freq	1 GHZ	5 GHZ	10 GHZ	15 GHZ	20 GHZ
Skin depth (μm)	2.08	0.93	0.66	0.53	0.46

Skin and Proximity Effects



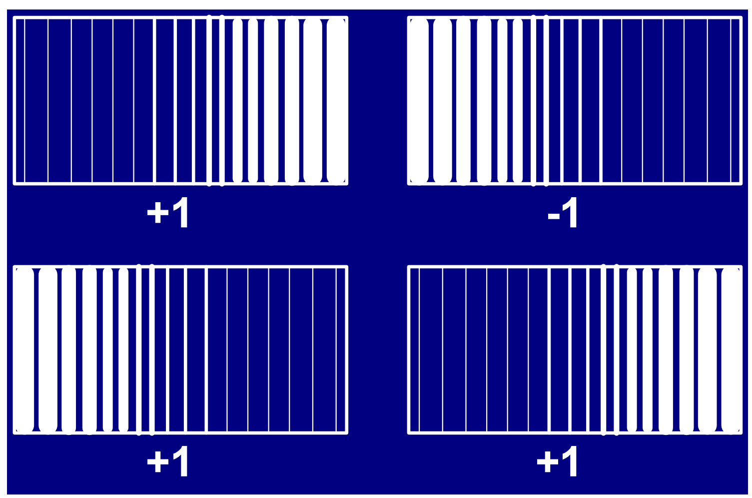
Isolated Wire 5um x 5um

Skin Effect in Isolated Conductors

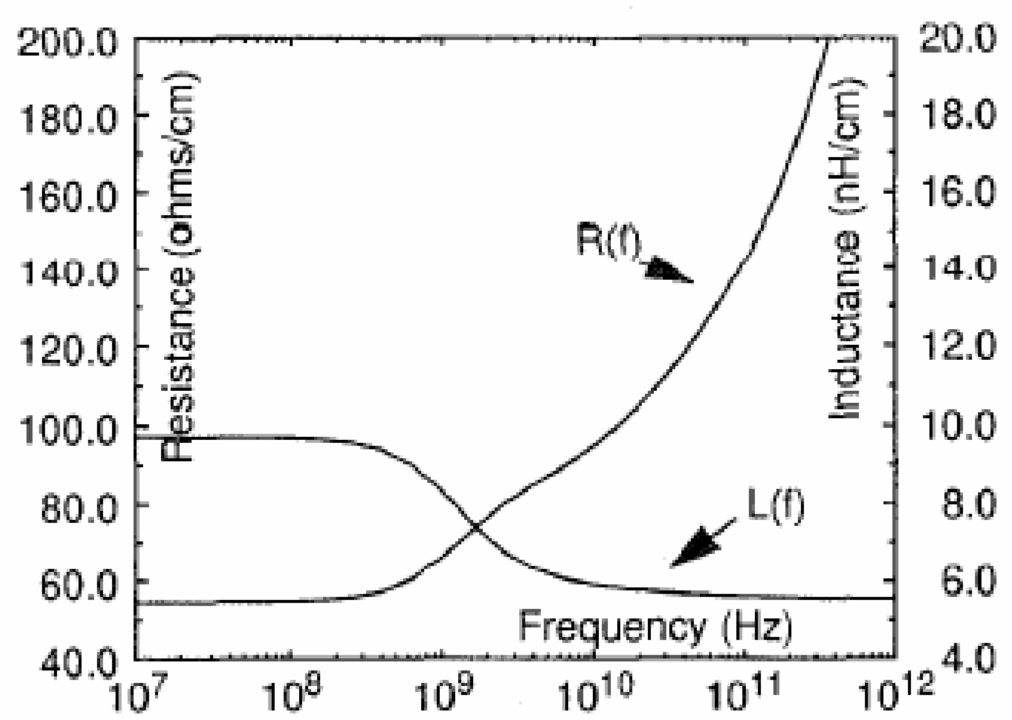


Isolated Wire 5um x 1um

Proximity Effect in Coupled Conductors



Frequency Dependence of R and L

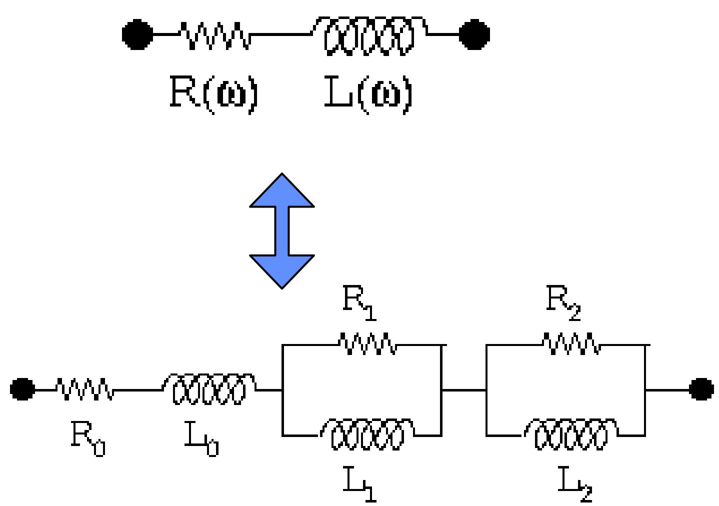


B. Krauter and S. Mehrotra, DAC, 1998.

- **Resistance increases due to skin effect**
- **For lower frequencies, current return path is distributed between all ground lines---thus loop inductance is higher and return path resistance is smaller…..**
- **For higher frequencies, current returns through closest ground paths---thus loop area is smaller, hence loop inductance reduces and return path resistance increases**

Modeling Frequency Dependent Behavior

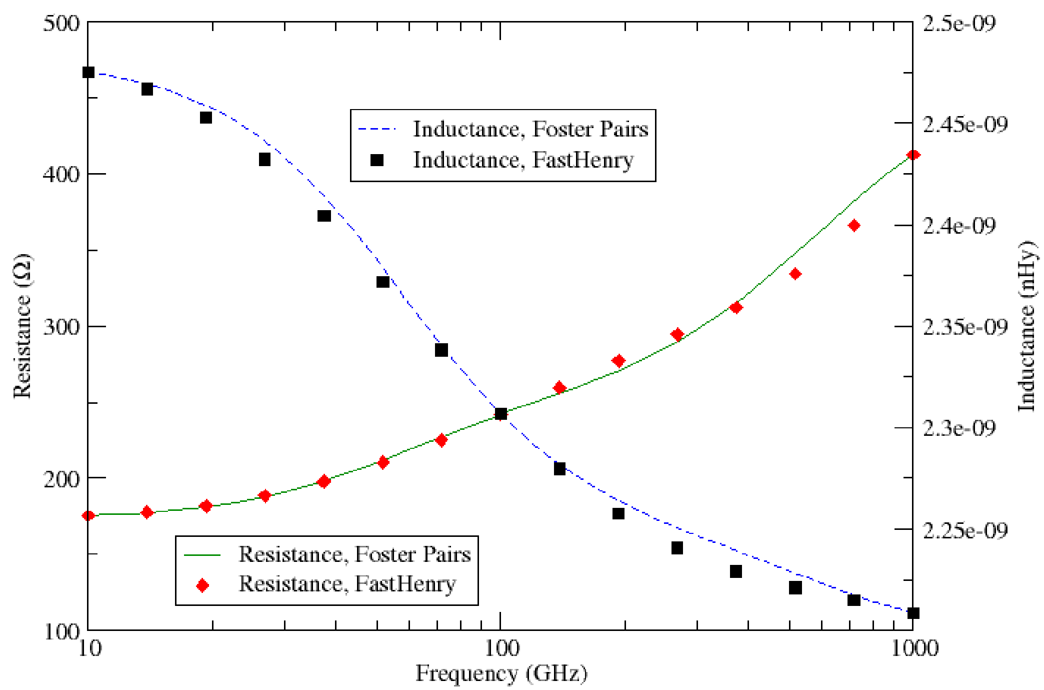
Replacing $R(\omega), L(\omega)$ with Foster Pairs



Note that at smaller frequencies L_1 ($Z=j\omega L$) will short R_1

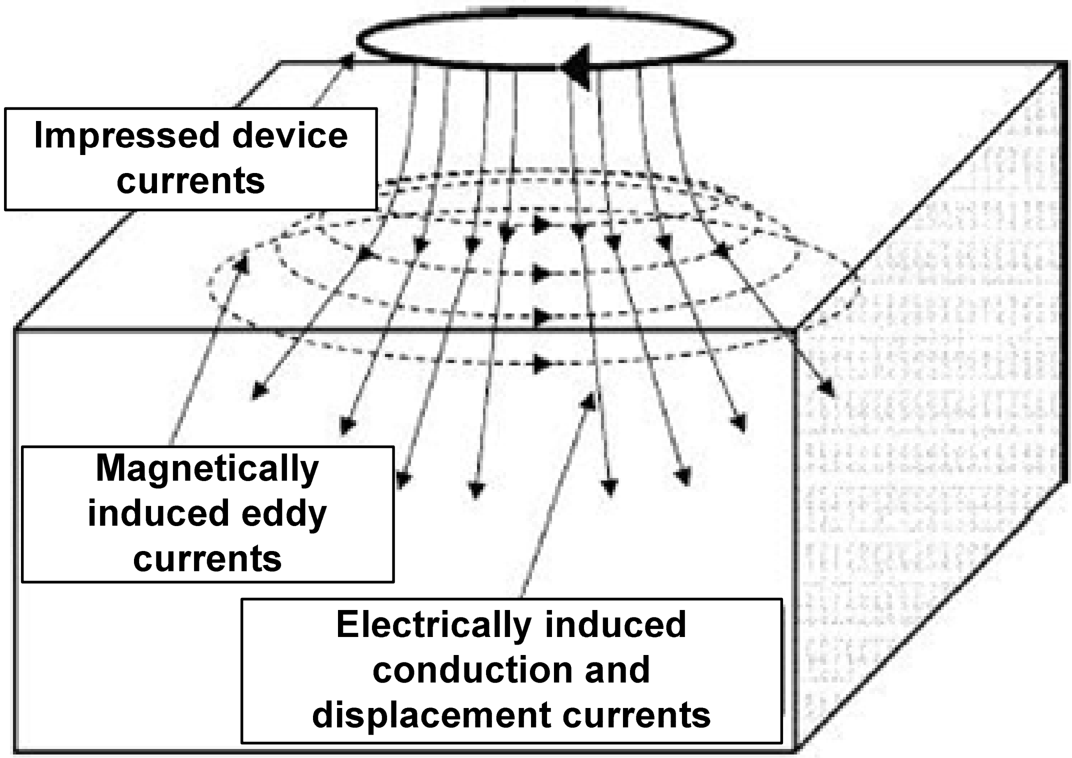
R_0 and $L_0+L_1+L_2$ are low-frequency values of R and L

At higher frequencies some current flows through R_1 and R_2, hence R increases with frequency and effective inductance decreases



Suaya et al., Advanced Metallization Conf. 2006

Substrate Effects



Impacts interconnect impedance extraction

A. M. Niknejad and R. G. Meyer, IEEE Trans. on Microwave Theory and Techniques, 2001

Carbon Nanotube Interconnects

- Limitations of Copper Interconnects
- Carbon Nanotubes: Basics
- CNT Interconnect Analysis: Performance, Power and Thermal/Reliability
- CNT Interconnect Fabrication and Integration Challenges
- Summary

What is wrong with Cu?

Future Interconnect Requirements: 2005 ITRS

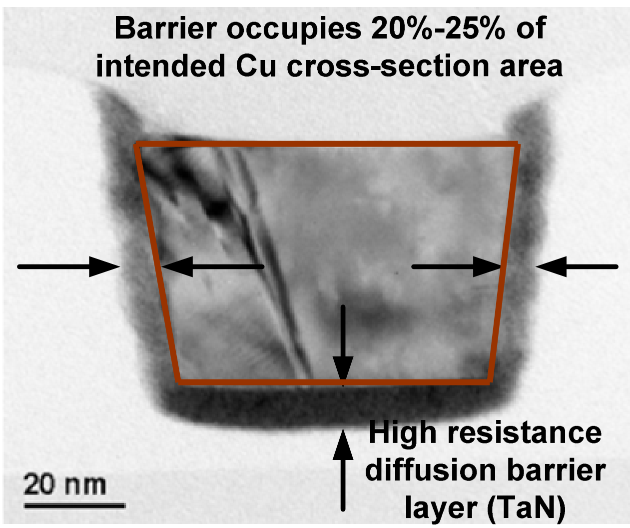
Year of Production	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*
DRAM ½ Pitch (nm) (contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU/ASIC Metal 1 ½ Pitch (nm)(contacted)	*28*	*25*	*22*	*20*	*18*	*16*	*14*
MPU Physical Gate Length (nm)	*11*	*10*	*9*	*8*	*7*	*6*	*6*
Number of metal levels	13	13	13	14	14	14	14
Number of optional levels – ground planes/capacitors	4	4	4	4	4	4	4
Total interconnect length (m/cm^2) – Metal 1 and five intermediate levels, active wiring only [1]	3571	4000	4545	5000	5555	6250	7143
FITs/m length/cm^2 × 10^{-3} excluding global levels [2]	1.4	1.3	1.1	1	0.9	0.8	0.7
J_{max} (A/cm^2) – intermediate wire (at 105°C)	1.06E+07	1.14E+07	1.47E+07	1.54E+07	1.80E+07	2.23E+07	2.74E+07
Metal 1 wiring pitch (nm)	56	50	44	40	36	32	28
Conductor effective resistivity (μΩ-cm) Cu intermediate wiring including effect of width-dependent scattering and a conformal barrier of thickness specified below	5.2	5.58	6.01	6.33	6.7	7.34	8.19

Red Areas: no known solutions! **from 2014 onwards: J_{max} > 1.06 x 10^7 A/cm2**

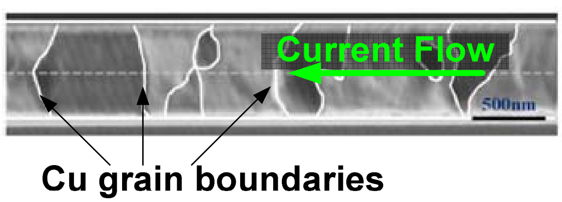
What is wrong with Cu?

- Size effect on Cu resistivity

MFP of Cu ~ 40 nm at room temperature

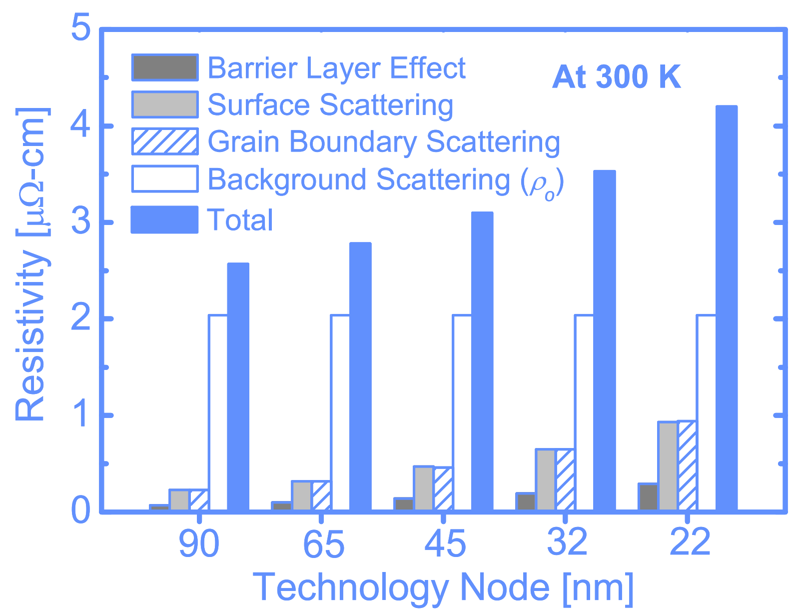


TEM cross-section of narrow Cu interconnect



Top-view TEM of Cu interconnect

Intermediate Tier Wires



Im et al., *IEEE TED*, Dec. 2005

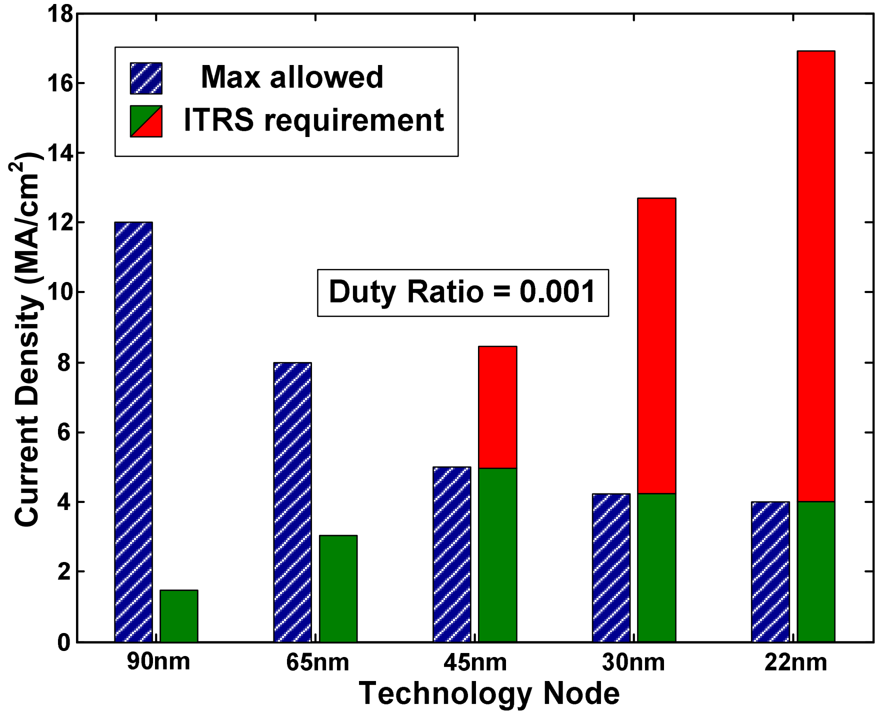
Based on analytical models in Steinhogl et al., *J. Appl. Phys.*, 2005.

Impact is worse for local wires and vias

Increases wire delay: even in local wires

Current Carrying Capability

- Electromigration Lifetime: strongly reduces with temperature
- Limits maximum current carrying capacity….



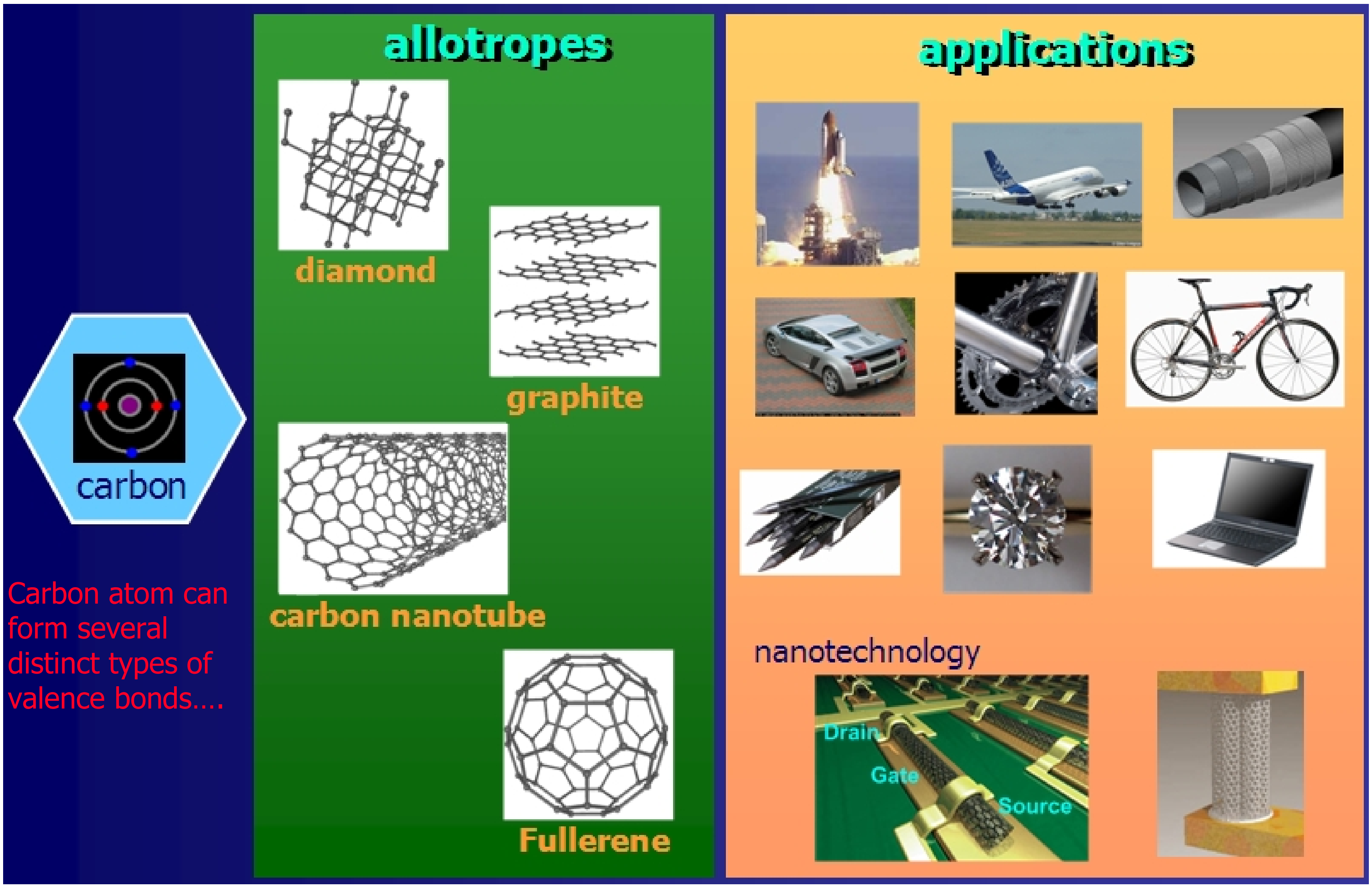
Maximum allowed J based on self-consistent (EM+Self-heating) solutions…

Significant deficit in current carrying capacity for local vias….

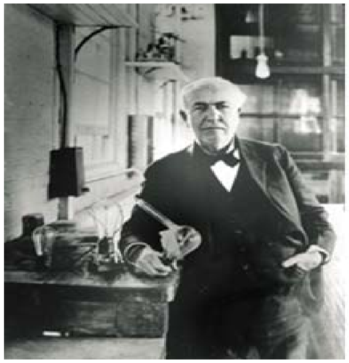
Increasing via size and/or number will be expensive….

Srivastava and Banerjee, *JOM 2004.*

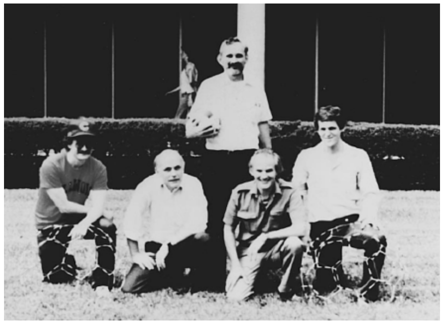
Forms of Carbon…



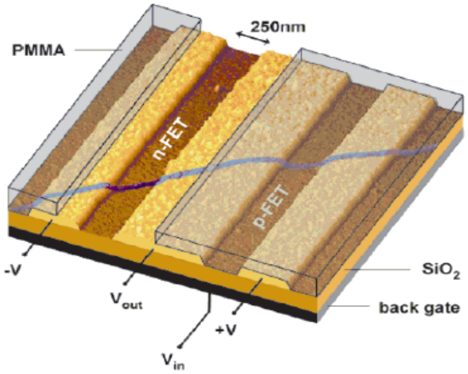
A bit of history....



Edison's original
carbon-filament lamp
US Patent 223898



Discovery of Fullerenes
(Smalley)



Carbon nanotube transistor
based logic-performing ICs (IBM)

1880

1985

2001

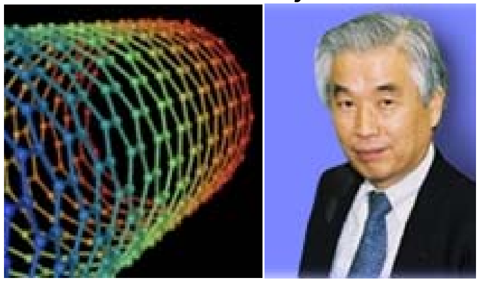
1978

1991

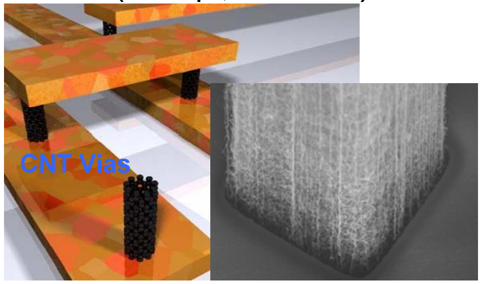
2002

F/A-18 Hornet
The first aircraft with
carbon fiber wings

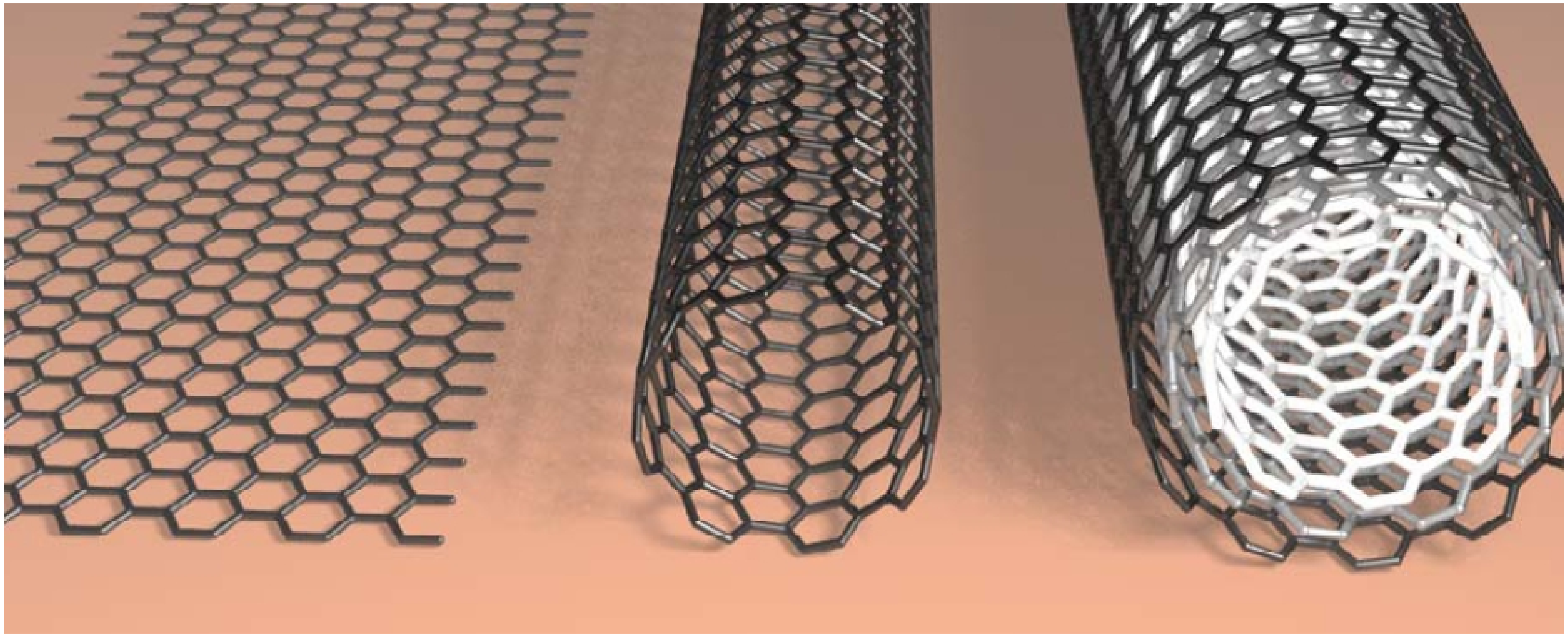
Nanotubes discovered at
NEC, by Japanese researcher
Dr. Sumio Iijima



Carbon nanotubes in
interconnet applications
(Kreupl, Infineon)



What are Carbon Nanotubes?



Graphene

Single-Walled Nanotube (SWCNT)

Multi-Walled Nanotube (MWCNT)

Courtesy: F. Kreupl, Infineon

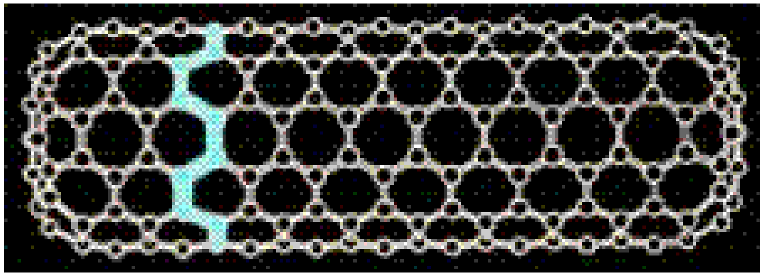
Multi-Walled CNTs….

- Most metal-CNT contact processes result in conduction confined to outermost shell – for interconnects, need to contact max shells.
- E_g ~1/d: Thick (>5nm) MWCNTs have a vanishing band gap at 300K, hence metallic…..
- Although Multi-Walled CNTs (MWCNTs) easier to fabricate in bundles, SWCNT bundles are more desirable for interconnect applications.
  - Higher resistivity than SWCNTs, especially for short (<1um) lengths
- From a reliability perspective, both MWCNT and SWCNT can carry currents in excess of 10^9 A/cm^2.

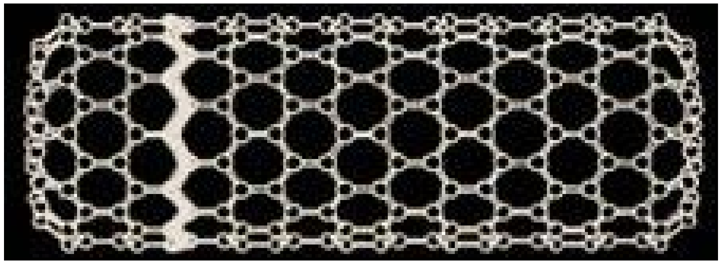
Single-Walled Carbon Nanotubes

SWCNTs

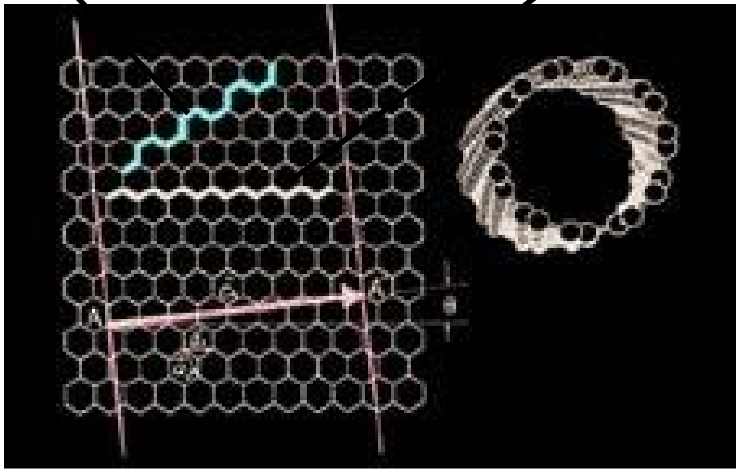
Armchair Nanotube (all metallic)



Zigzag Nanotube (metallic or semi-conducting)



Various roll-ups possible---chirality



About 1/3 of all SWCNTs are metallic and 2/3 are semiconducting

Chiral nanotube (mostly semi-conducting)

Attractive properties of SWCNTs

Length: microns to millimeters

Diameter: 0.4-100 nm

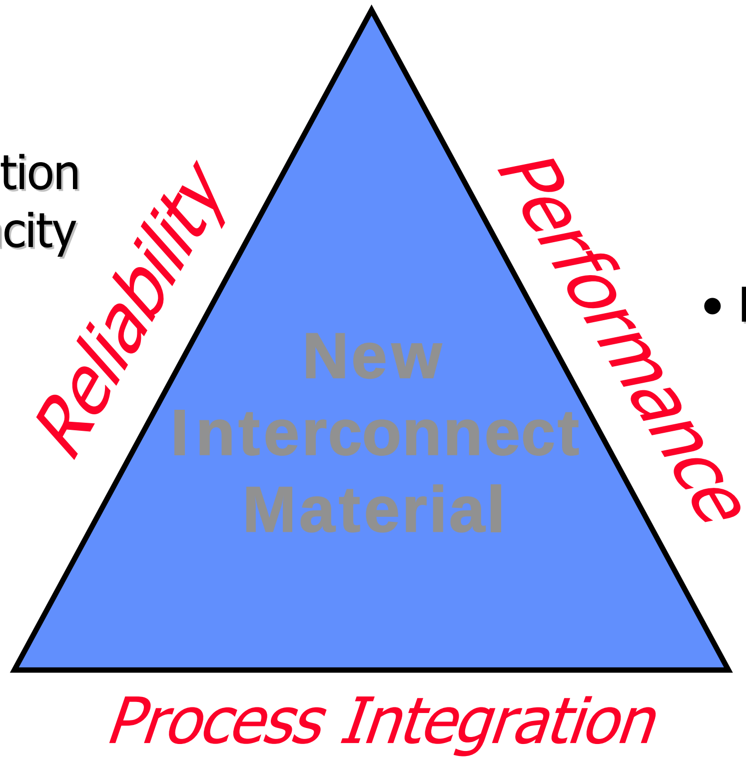
Tensile strength: 45 TPa! (high strength steel ~ 2TPa)

Temperature Stability: up to 2800 ^{0}C in vacuum and up to 700 ^{0}C in air

	CNT	Cu
Max current density (A/cm^2)	>1x10^9 **Radosavljevic, et al.**, *Phys. Rev. B*, **2001**	<1x10^7
Thermal conductivity (W/mK)	5800 **Hone, et al.**, *Phys. Rev. B*, **1999**	385
Mean free path (nm) @ room temp	>1000 **McEuen, et al.**, *Trans. Nano.*, **2002**	40

Requirements for a new interconnect material….

- Resistance to electromigration
- High current carrying capacity
- High mechanical strength



- High conductance (low resistivity)

- CMOS process compatible
- Low thermal budget
- Low diffusivity in dielectrics and Si

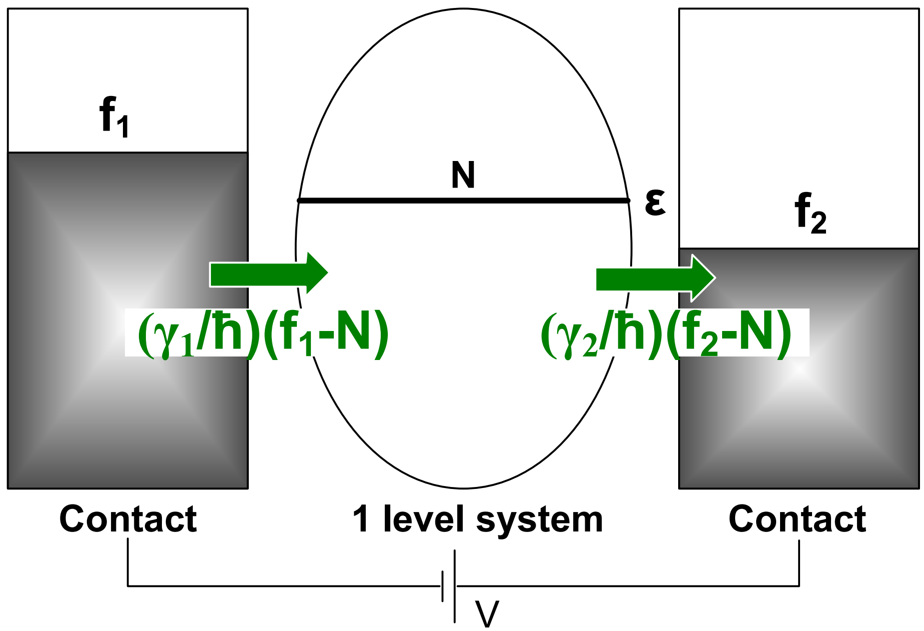
CNT Interconnect performance Modeling

Model R, C and L: Important to understand mesoscopic physics……

Provide early feedback to process designers…..

CNT Quantum Resistance : R_Q

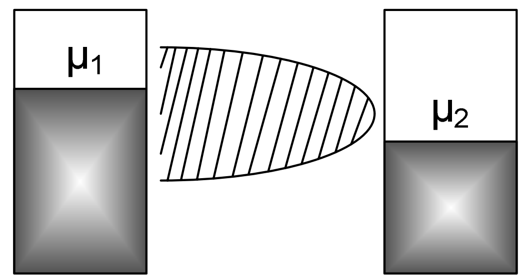
S. Datta, *Nanotechnology*, 2004



f_1, f_2: Fermi functions at left and right contacts

$\gamma_1/\hbar$, $\gamma_2/\hbar$: rate at which electron initially at energy ε will escape into left/right contact resp.

$$I = \frac{e}{\hbar}\frac{\gamma_1\gamma_2}{\gamma_1+\gamma_2}\left[f_1 - f_2\right]$$



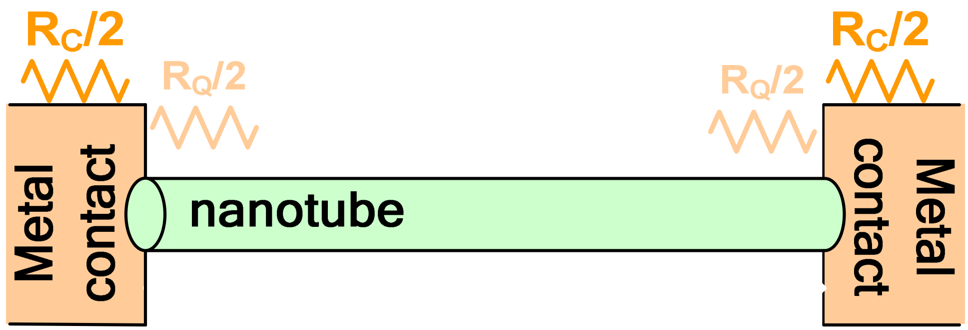
Energy level broadens due to coupling with contacts

$$I = \frac{4e^2}{h}\frac{\gamma_1\gamma_2}{\gamma_1+\gamma_2}\frac{V}{\gamma_1+\gamma_2} \rightarrow \frac{e^2 V}{h}$$

Ideal (max.) conductance: $\gamma_1 = \gamma_2 : G = \frac{I}{V} = \frac{e^2}{h}$

Carbon nanotube has 4 conducting channels: $R_Q = \frac{h}{4e^2}$; For $L > \lambda_{CNT}$: $R_S(p.u.l) = \left(\frac{h}{4e^2}\right)\frac{1}{\lambda_{CNT}}$

CNT Resistances: R_Q, R_C and R_S



- **$R_Q \approx 6.45\ K\Omega$: Intrinsic nanotube quantum contact resistance - even for very short lengths with no scattering and perfect contacts (lowest possible R—hence need bundles!)**

$$= \frac{h}{4e^2}$$

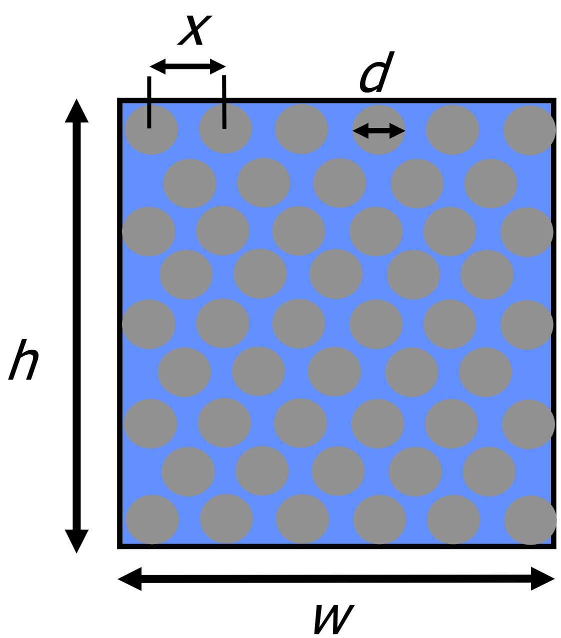
- **R_C : Imperfect metal-nanotube parasitic contact resistance (can be high…up to 100 KΩ)**

S. Datta, *Nanotechnology,* 2004

- **R_S: length dependent scattering resistance (for Length >> CNT mfp =λ)**

$$= \frac{h}{4e^2}\frac{L}{\lambda}$$

CNT Bundle Resistance



- x accounts for density of metallic CNTs
- calculate n_{CNT} in terms of w, h, d and x

Srivastava et al., *IEDM* 2005

Note: higher n_{CNT} ⇒ lower R_{bundle}

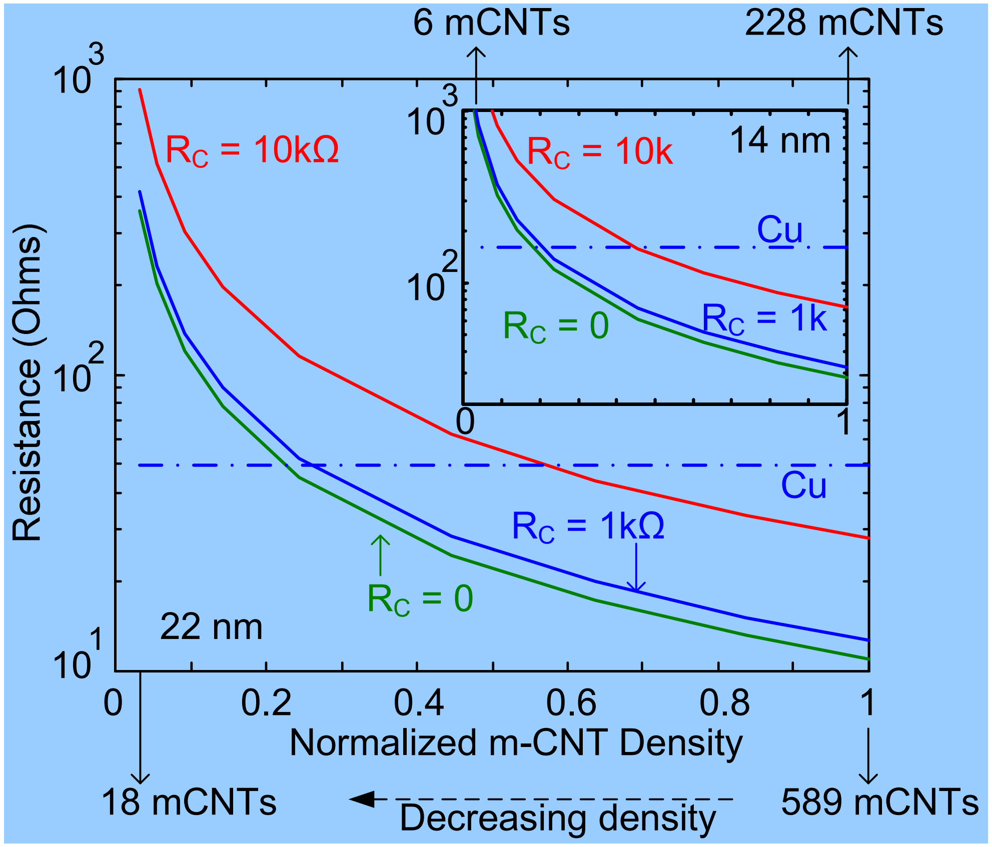
Hence dense bundle is desirable, i.e., smallest possible d and x

Assuming parallel independent currents– since inter-tube resistance is high: ~ 2 MΩ -10 MΩ H. Stahl, et al., *Phys. Rev. Lett.*, 2000

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} = \frac{R_Q + R_C}{n_{CNT}} \quad \text{..............if } L << \lambda_{CNT}$$

$$R_{bundle} = \frac{R_{isolated}}{n_{CNT}} = \frac{R_Q + R_C + R_S}{n_{CNT}} \quad \text{.......if } L > \lambda_{CNT}$$

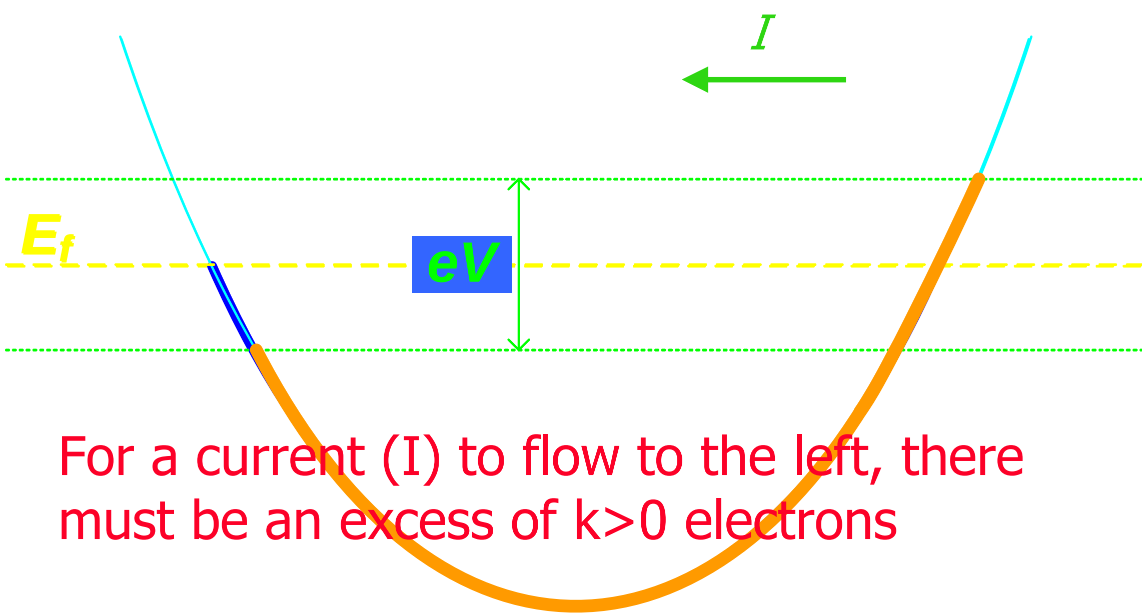
CNT Bundle Resistance (Results)



Local interconnect length 1um

*Impact of metal-nanotube contact resistance R_C on bundle resistance will decrease for long lengths

CNT Inductance: L_K and L_M



For a current (I) to flow to the left, there must be an excess of k>0 electrons

Initially equal number of left-moving (k<0) and right-moving (k>0) electrons

Additional Kinetic energy stored in the system when a current (I) flows:

$$\Delta E = \frac{1}{2} \times \frac{h}{2e^2 v_F} \times I^2$$

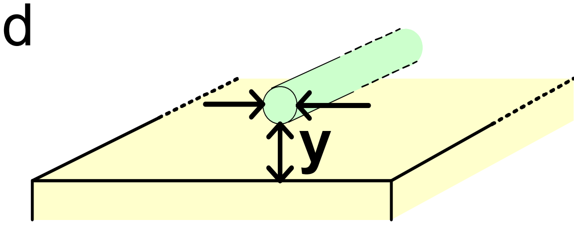
$$L_K \approx 16 nH / \mu m$$

Kinetic inductance: for L << mfp

(Bockrath, PhD Thesis, Berkeley, 1999)

Magnetic inductance

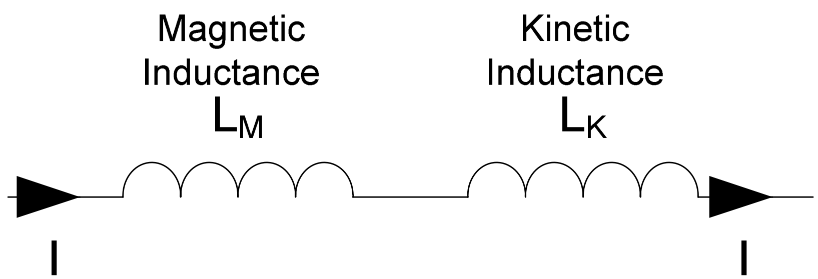
Magnetic energy stored in a current carrying wire over a substrate



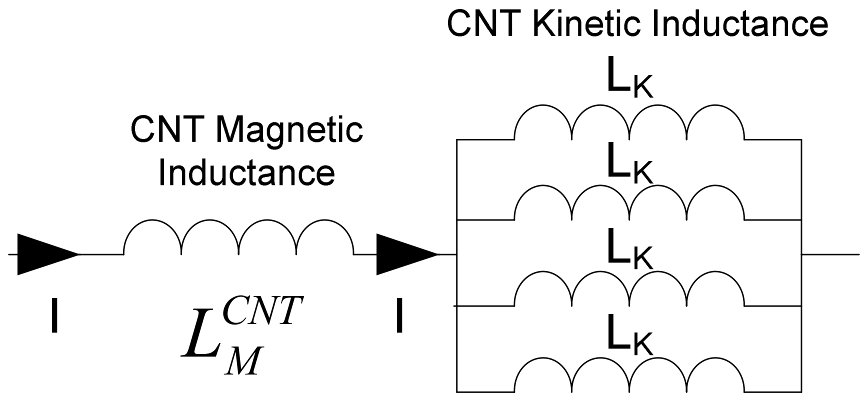
$$L_M^{CNT} = \frac{\mu}{2\pi} \ln\left(\frac{y}{d}\right)$$

CNT Bundle Inductance

1 channel of a CNT

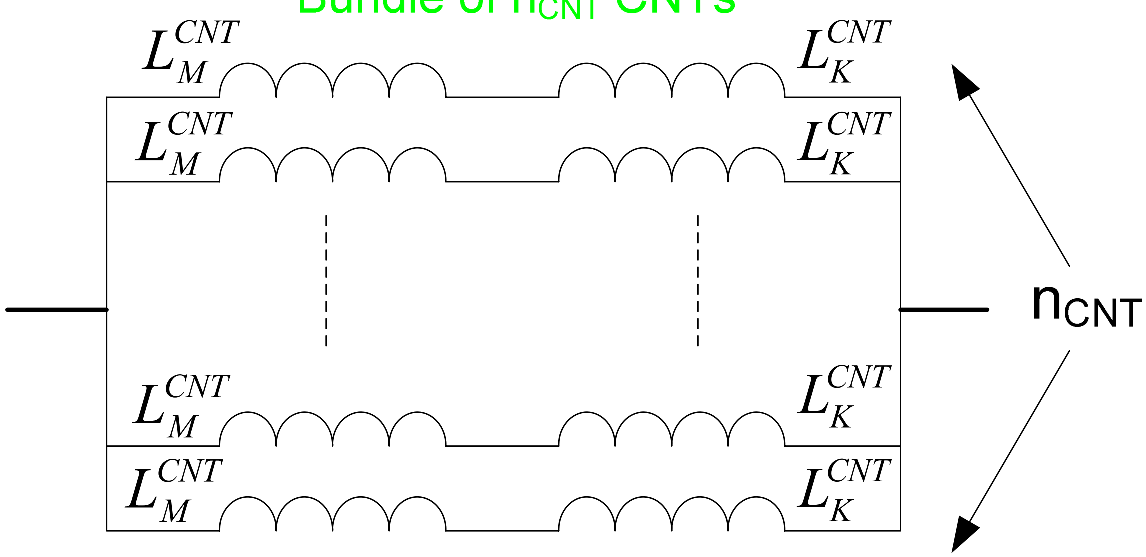


Isolated CNT (4 channels)



$$L_K^{CNT} = L_K / 4$$

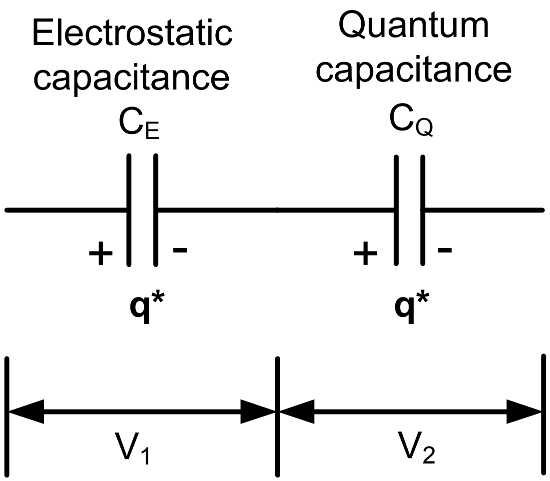
Bundle of n_{CNT} CNTs



$$L_{bundle} = \frac{L_M^{CNT} + L_K^{CNT}}{n_{CNT}}$$

Large n_{CNT} makes L_{bundle} small – delay dominated by RC

CNT Capacitance: C_Q and C_E

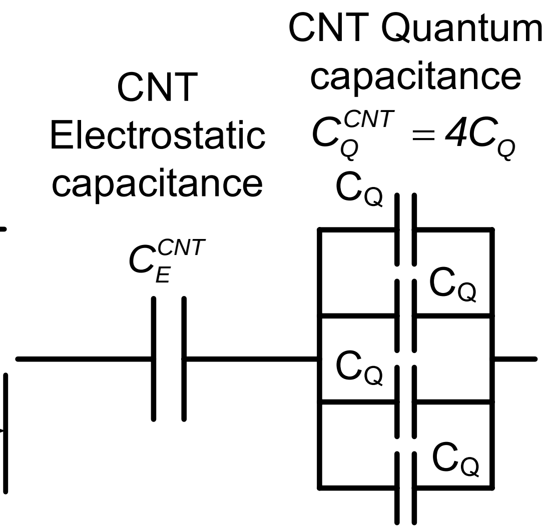


1 channel of a CNT

$$C_Q = \frac{2e^2}{hv_F}$$

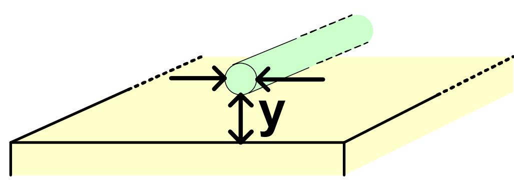
Energy needed to add an electron at an available quantum state above Fermi level (v_F = Fermi velocity)

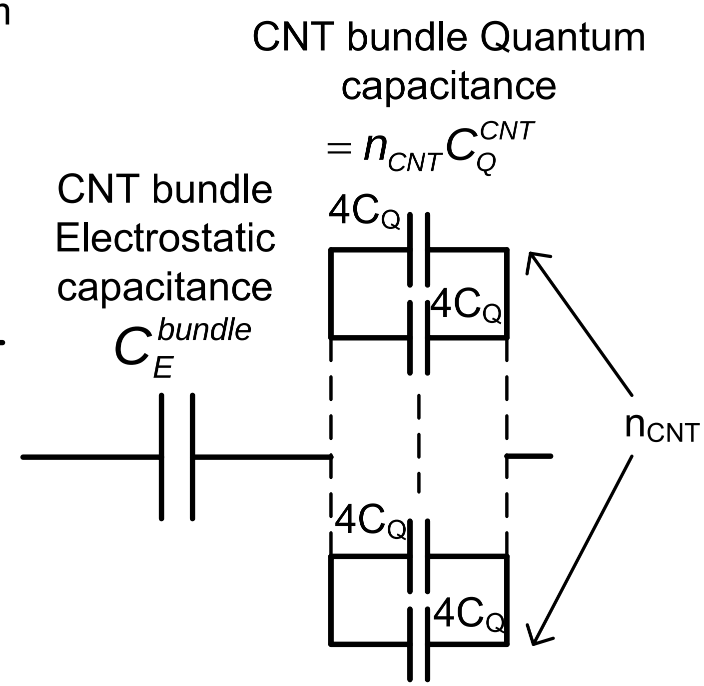
(Datta, Quantum Transport, 2005)



Isolated CNT (4 channels)

$$C_E^{CNT} = \frac{2\pi\varepsilon}{\ln\left(\frac{y}{d}\right)}$$





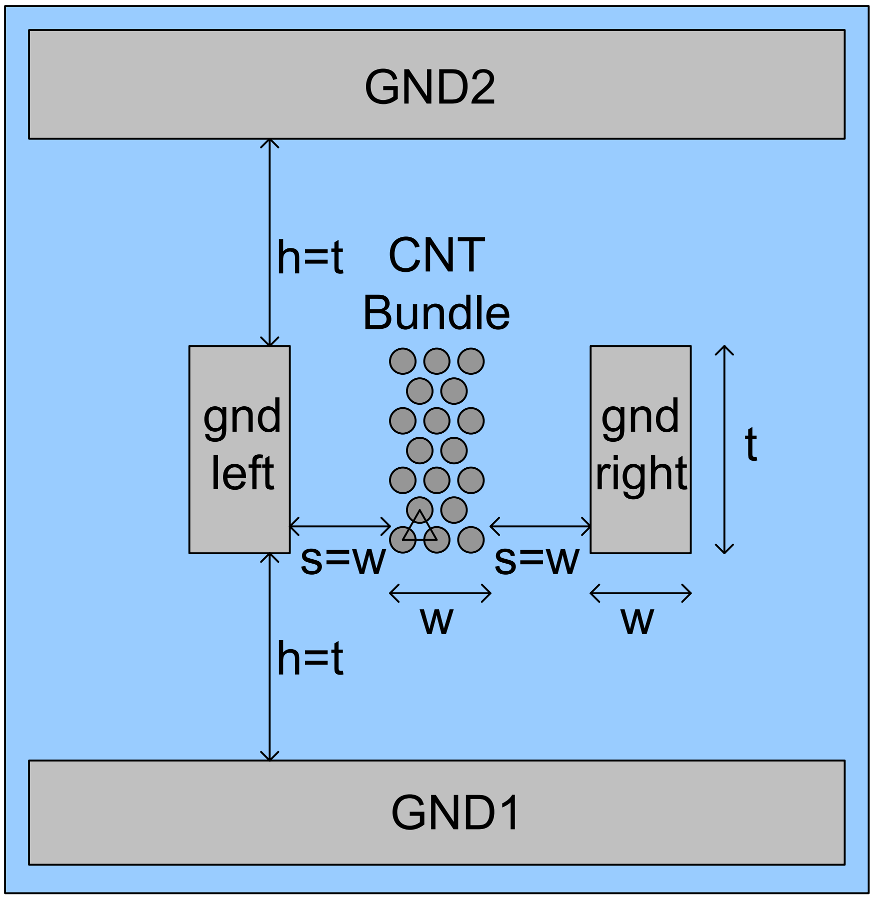
Bundle of n_{CNT} CNTs

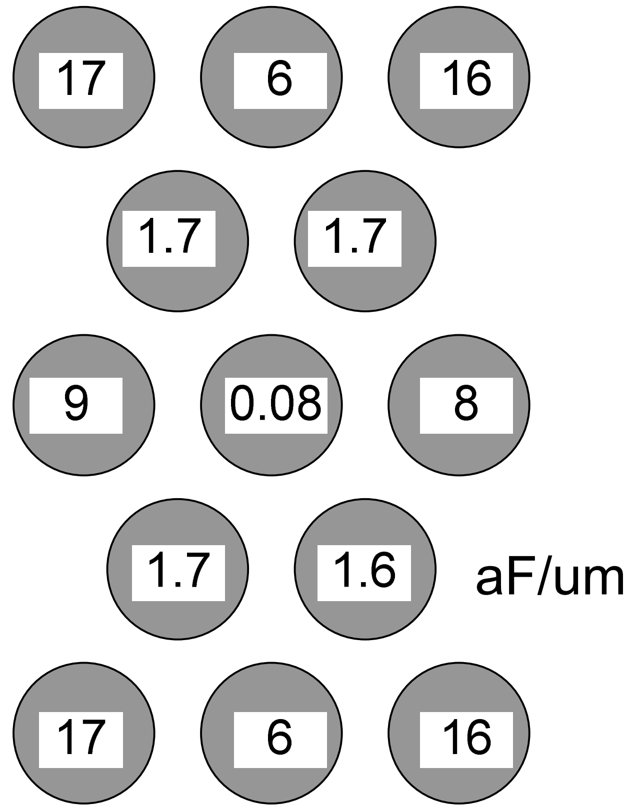
$$C_Q^{bundle} = C_Q^{CNT} \cdot n_{CNT}$$

$$\frac{1}{C^{bundle}} = \frac{1}{C_Q^{bundle}} + \frac{1}{C_E^{bundle}}$$

N. Srivastava et al., *IEDM* 2005

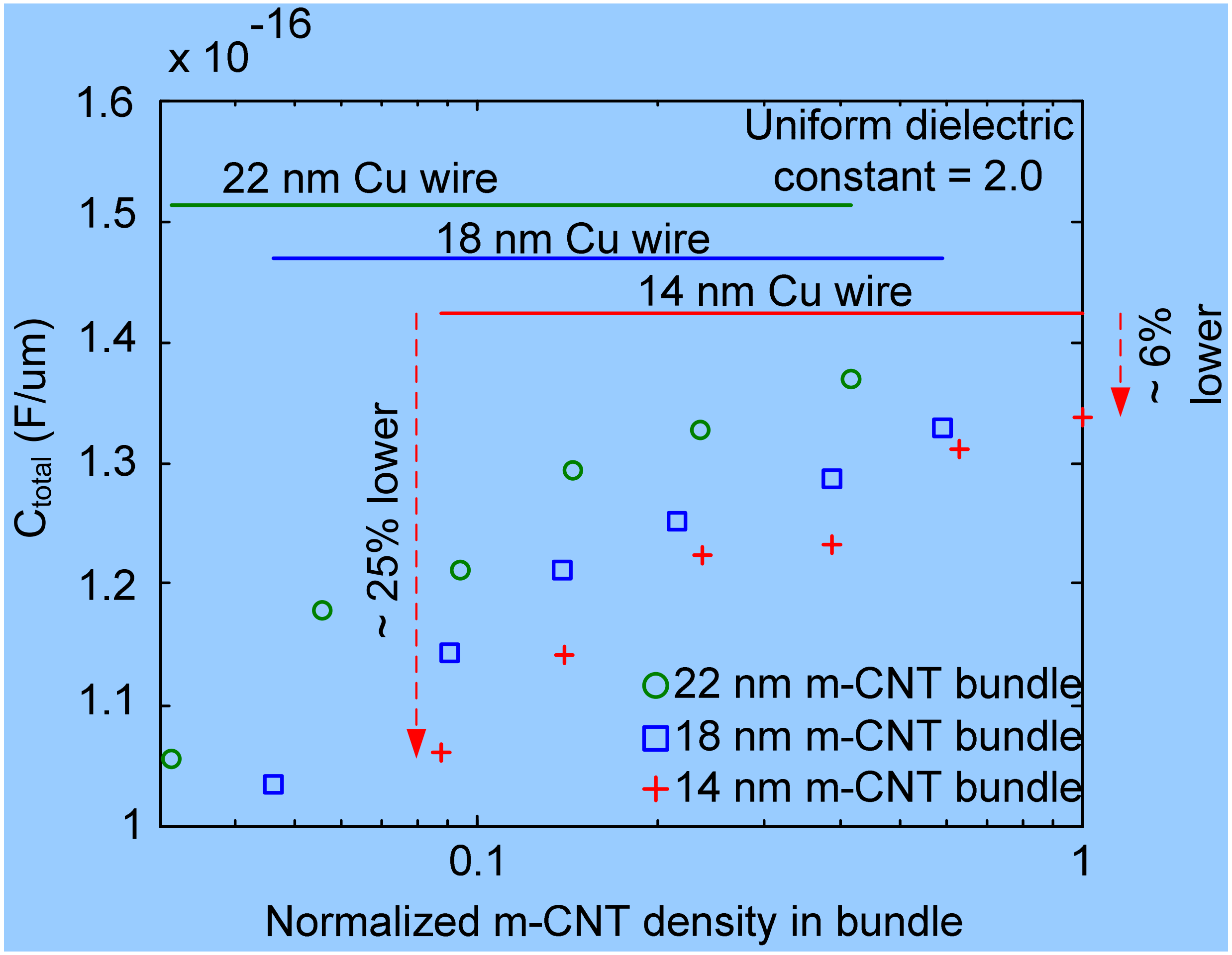
CNT Bundle Structure for Estimating C_E

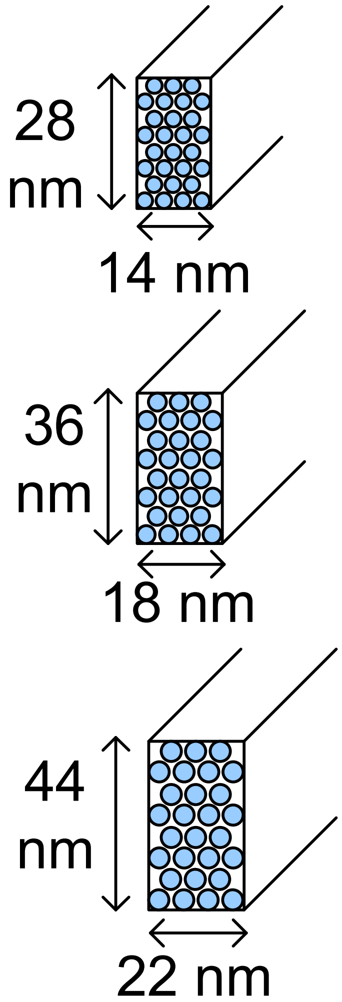




Inner CNTs are effectively screened from the surrounding interconnect geometry

CNT Bundle Electrostatic Capacitance





CNT Interconnect Equivalent Circuit

$\frac{R_C + R_Q}{2n_{CNT}}$ L_{bundle} L_{bundle} $\frac{R_C + R_Q}{2n_{CNT}}$

C_Q^{bundle} C_Q^{bundle}

C_E^{bundle} C_E^{bundle}

if $L \ll \lambda_{CNT}$

$\frac{R_C + R_Q}{2n_{CNT}}$ $\frac{R_S}{n_{CNT}}$ $\frac{R_S}{n_{CNT}}$ $\frac{R_C + R_Q}{2n_{CNT}}$

L_{bundle} C_Q^{bundle} L_{bundle} C_Q^{bundle}

C_E^{bundle} C_E^{bundle}

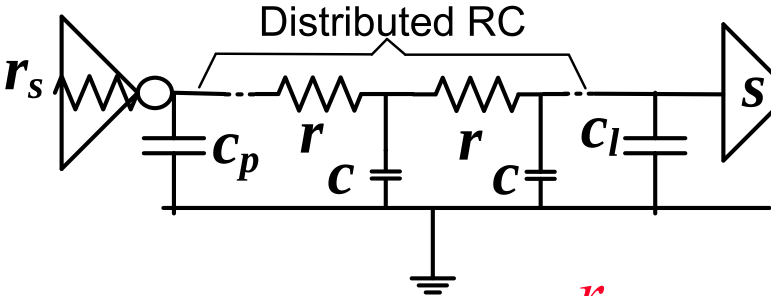
if $L > \lambda_{CNT}$

Banerjee et al., *DAC*, 2006

Carbon Nanotube Vs Copper Interconnects

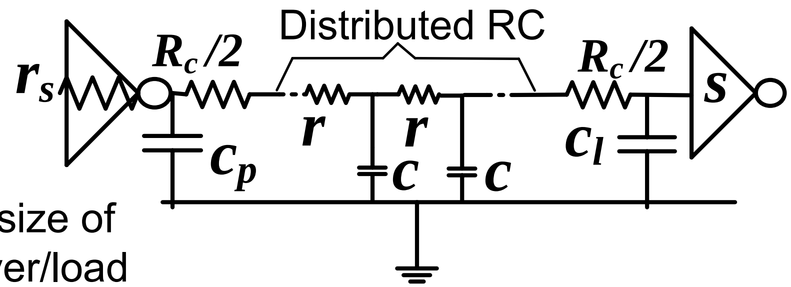
CNT vs Cu Interconnect Delay

Cu Interconnect



$$\tau = r_s(c_l + c_p) + \frac{r_s}{s} cl + \frac{1}{2} rcl^2 + rsc_l l$$

CNT Interconnect

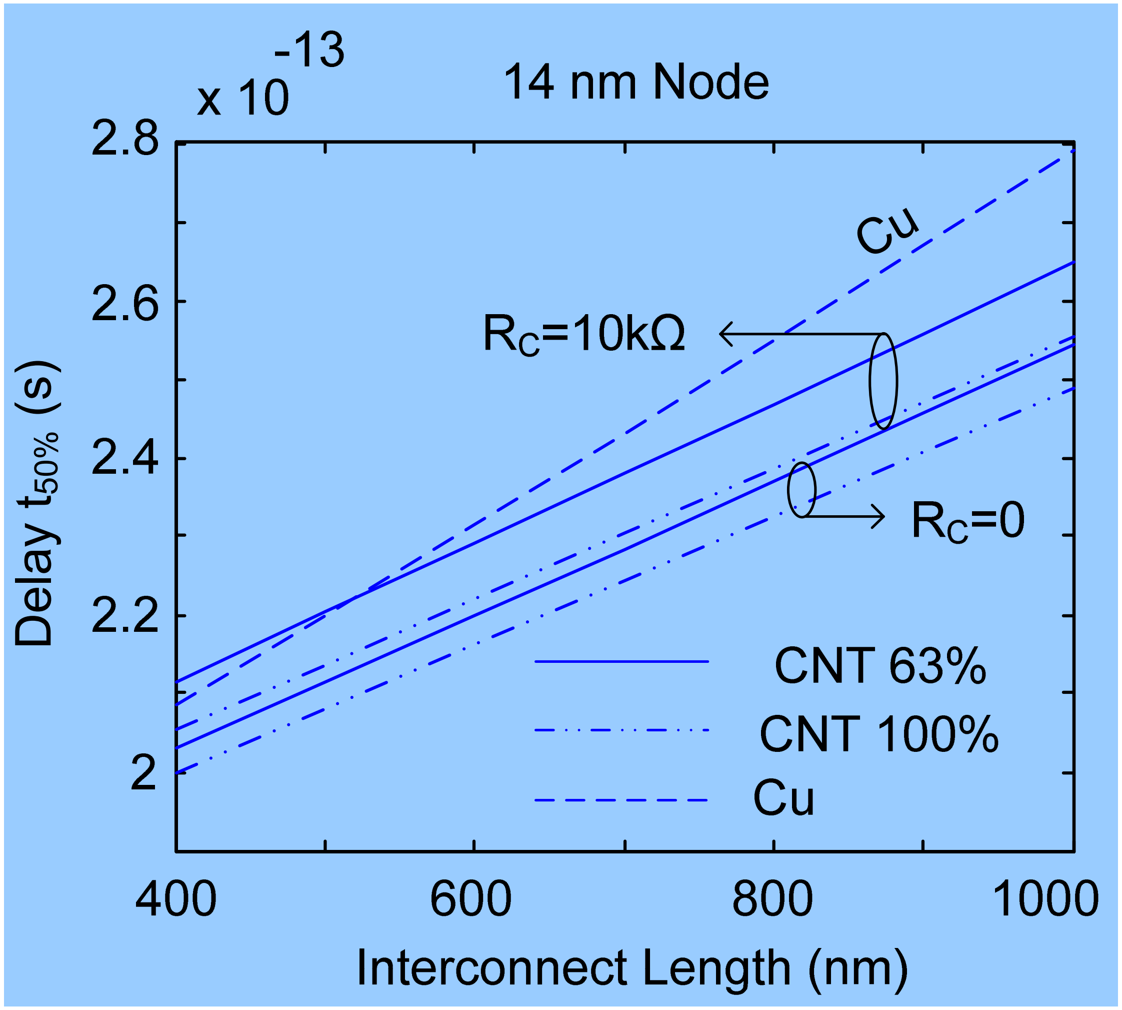


s: size of driver/load

$$\tau = r_s(c_l + c_p) + \frac{r_s}{s} cl + R_c cl + 2R_c c_l s + \frac{1}{2} rcl^2 + rsc_l l$$

- **Inductance is small; delay dominated by R-C**
- **Short (local) interconnects**
  - **Small drivers r_s > *interconnect resistance***
- **Long (global) interconnects**
  - **Large drivers r_s < *interconnect resistance***

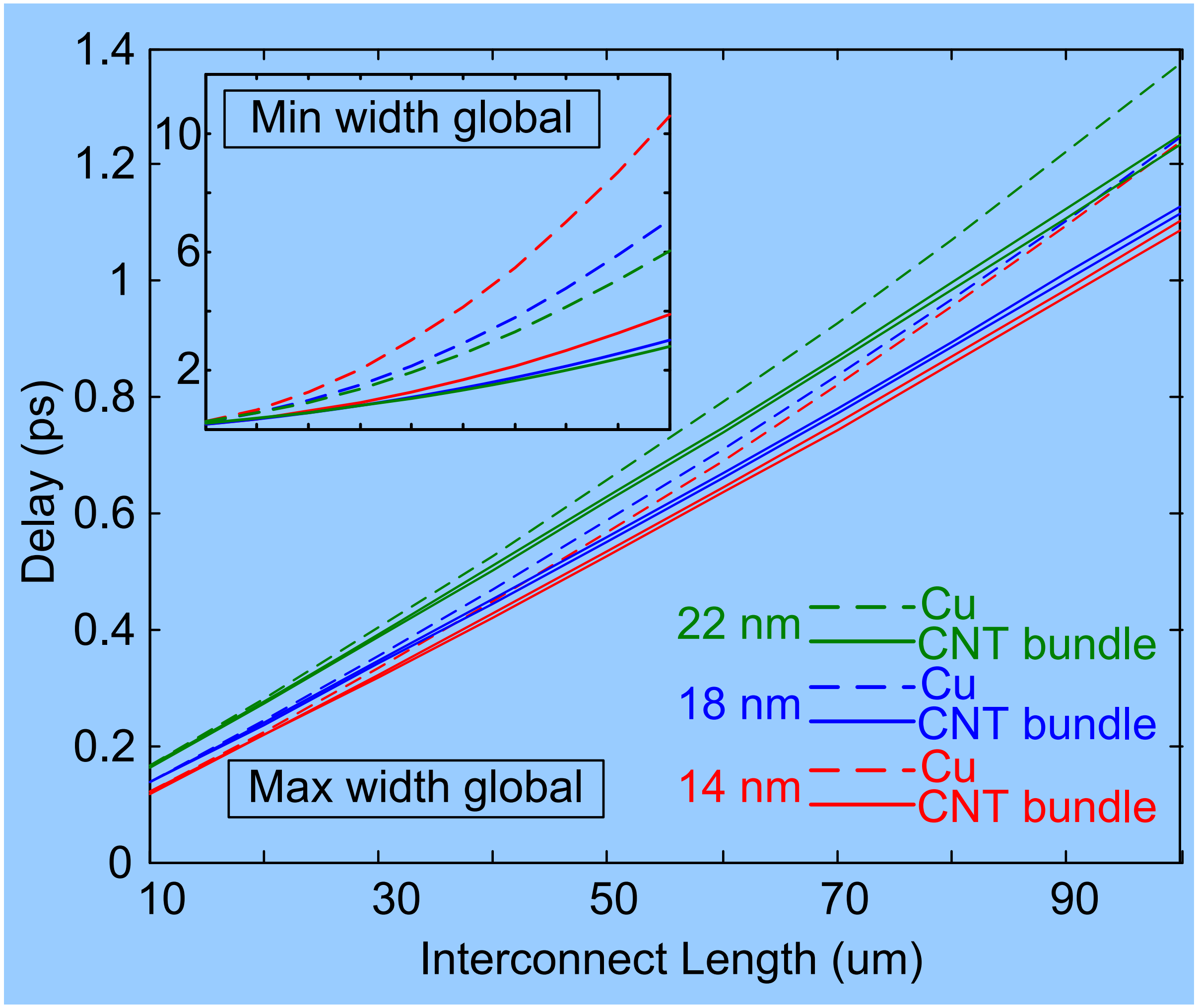
Local Interconnect Delay



about 5-10% lower than that with Cu….

At lower CNT densities, R increases but C decreases….hence 63% case is competitive with Cu

Global Int. Delay (Unbuffered)

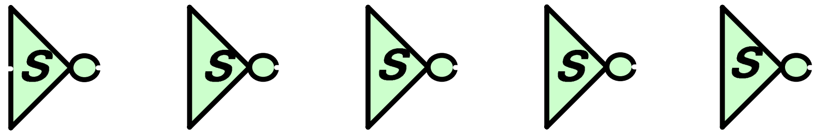


W_{max} = 1 um

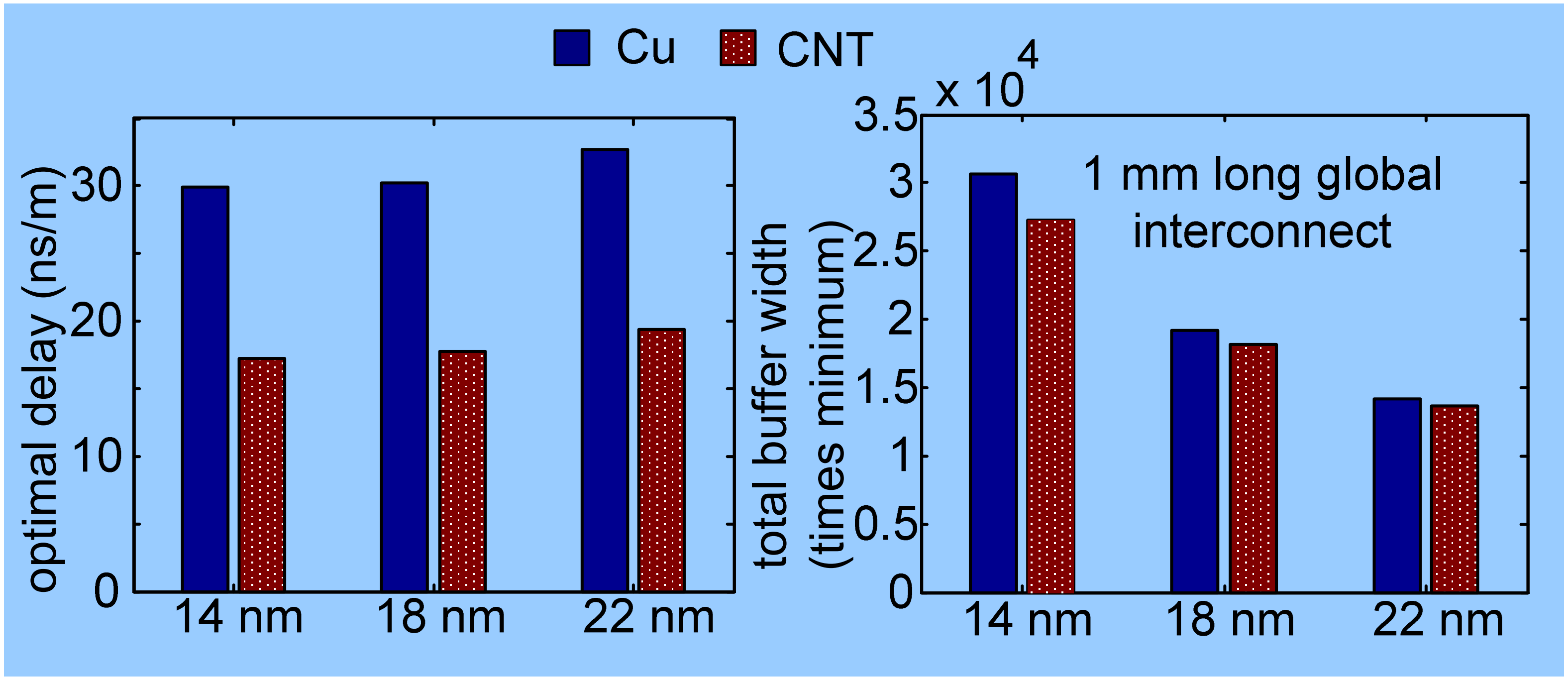
Twin solid lines represent $R_c = 0$ and 10KΩ…..hardly any difference!

As length increases, R_s becomes large and effect of R_c diminishes….

Optimally Buffered Global Interconnect: Delay and Power



Optimal s and l



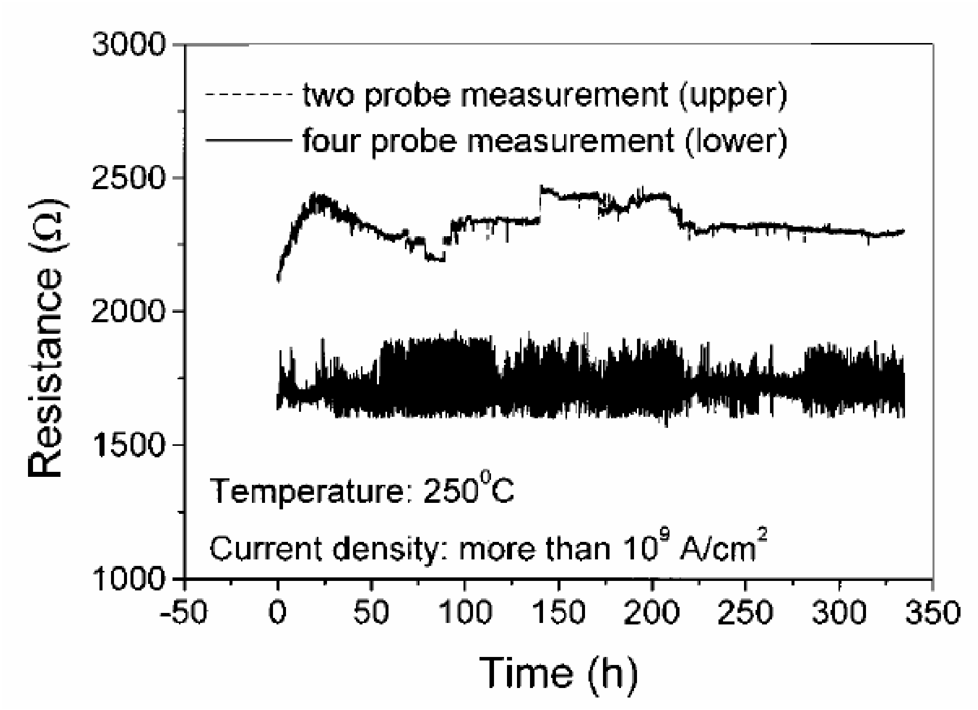
Optimal delay per unit length for global CNT bundles much lower than Cu.

Repeater power dissipation with CNT bundles is competitive (less than) with Cu

Assuming worst case electrostatic capacitance (~ Cu capacitance)....

CNT Interconnect Reliability
and
Back-End Thermal Management

Reliability and current carrying capacity of MWCNTs

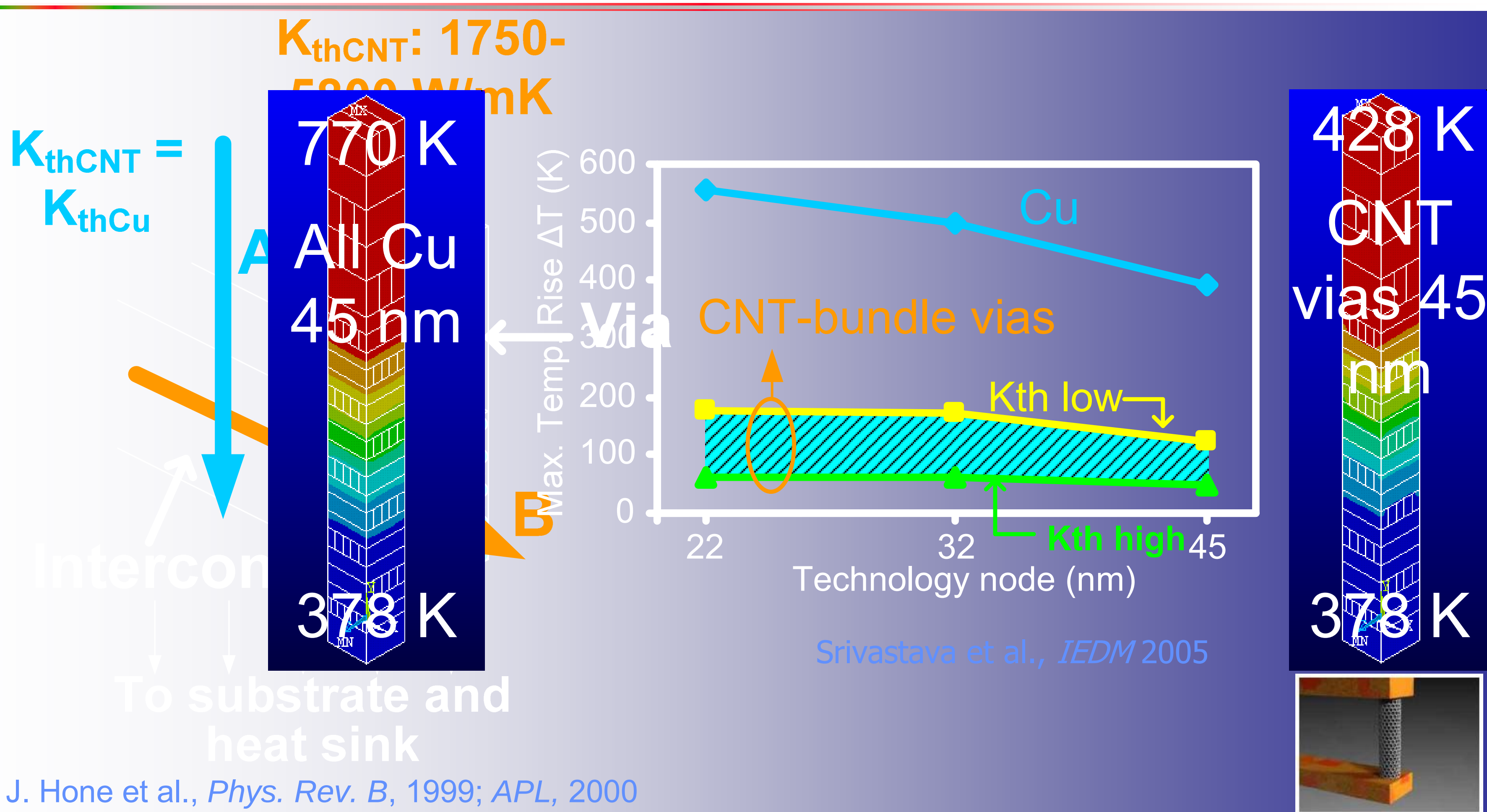


Wei et al. *APL* 79, 1172 (2001)

- Current density up to 10^{10} A/cm^2 without heatsink (not embedded in SiO_2)
- Equivalent Au-, Cu-, Al-wires deteriorate at 10^7 A/cm^2

SWCNTs show similar current carrying capacity… [Radosavljevic et al., *PRB*, 2001]

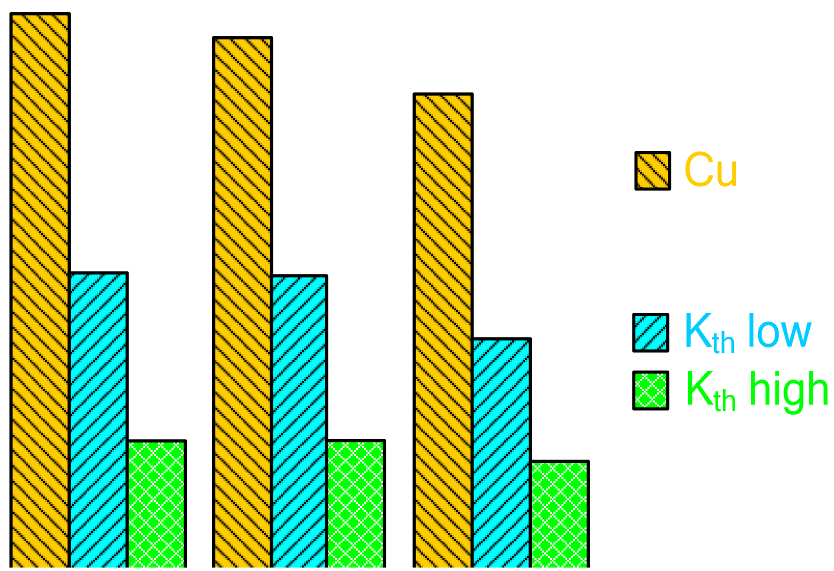
Back-end Thermal Management with CNT vias



J. Hone et al., *Phys. Rev. B*, 1999; *APL*, 2000

Maximum interconnect temperature rise is significantly smaller when CNT bundles are used as inter-layer vias

Impact of CNT Vias on Cu Interconnect Reliability and Performance



2 orders of magnitude improvement in the lifetime of Cu!

Srivastava et al. *IEDM* 2005

Hybridization of CNT vias with Cu lines can help extend the lifetime of Cu……

Delay also improves by 30%.....

CNT Interconnect Process Integration

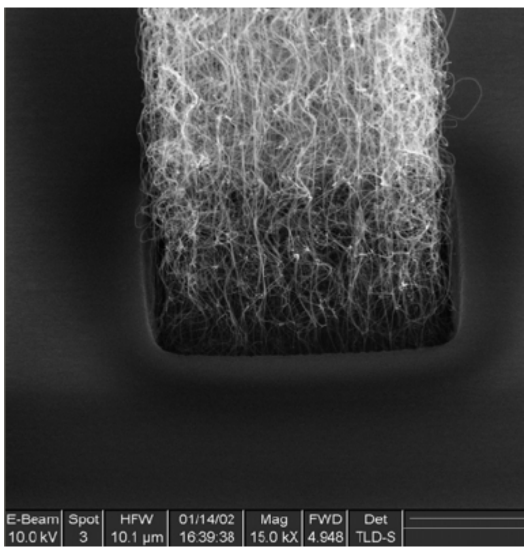
CNT interconnect (via) fabrication

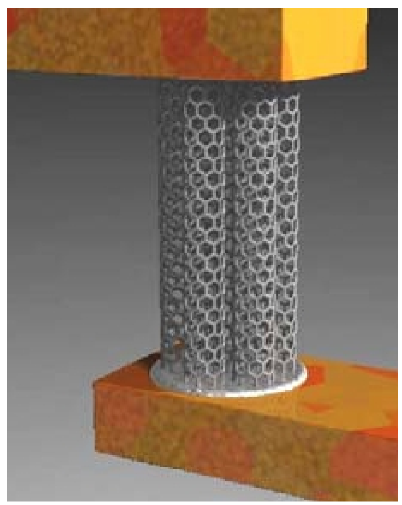
Catalytic CVD Growth

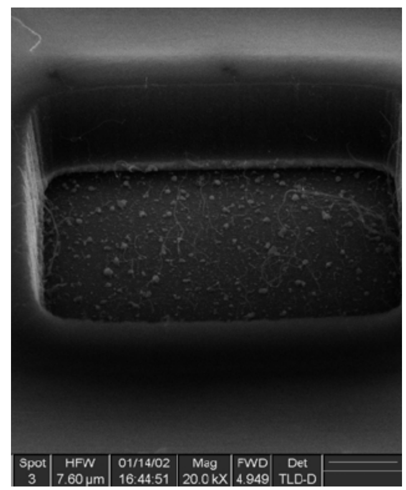
nature does it for you….all you need is 3 ingredients

1. Catalyst nanocluster: Fe, Ni or Co
2. Carbon containing compound (gas): CH4, C2H2, CH3CH2OH….
3. Energy (Temperature): 500-1400 ^{0}C

Substrate –catalyst interaction is also very important….





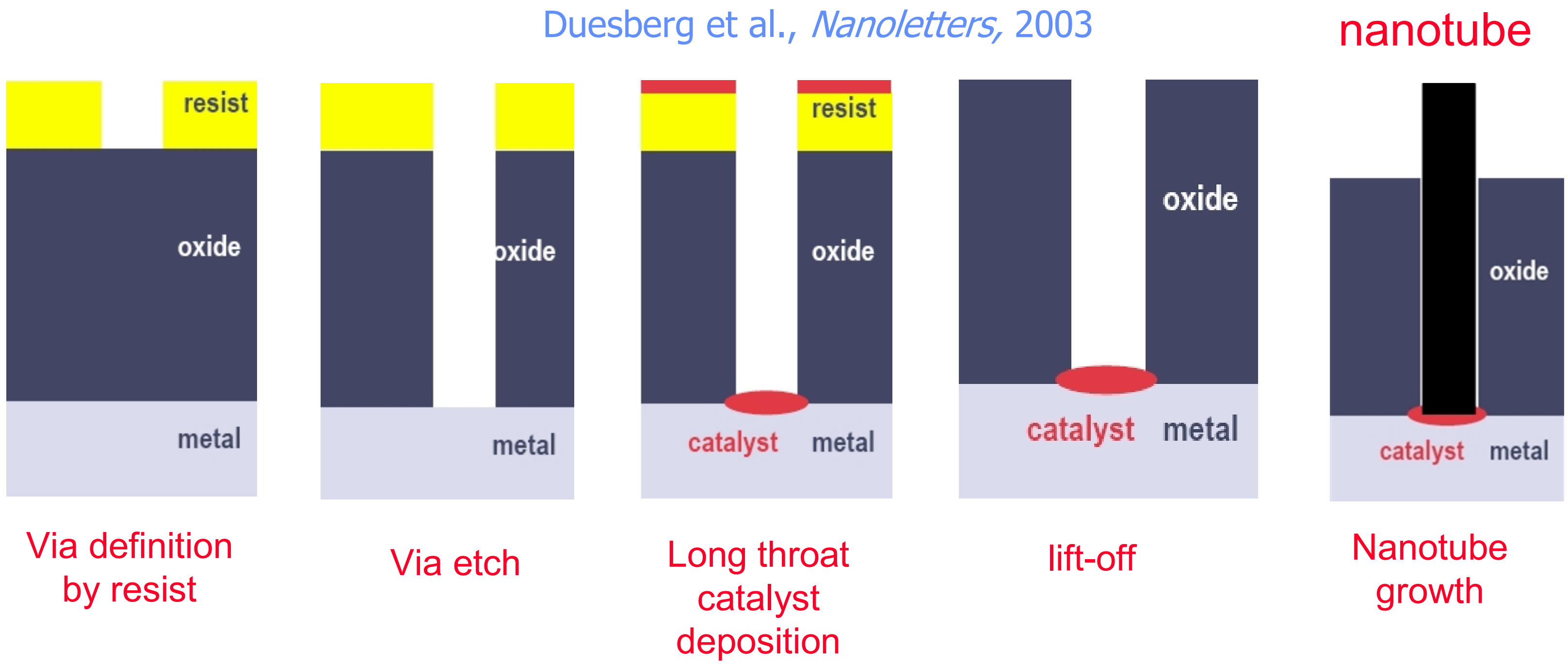


Courtesy: F. Kreupl, Infineon

Fabrication Techniques & Challenges-I

- Long throat catalytic deposition (via PVD) in high aspect ratio trenches

Duesberg et al., *Nanoletters,* 2003



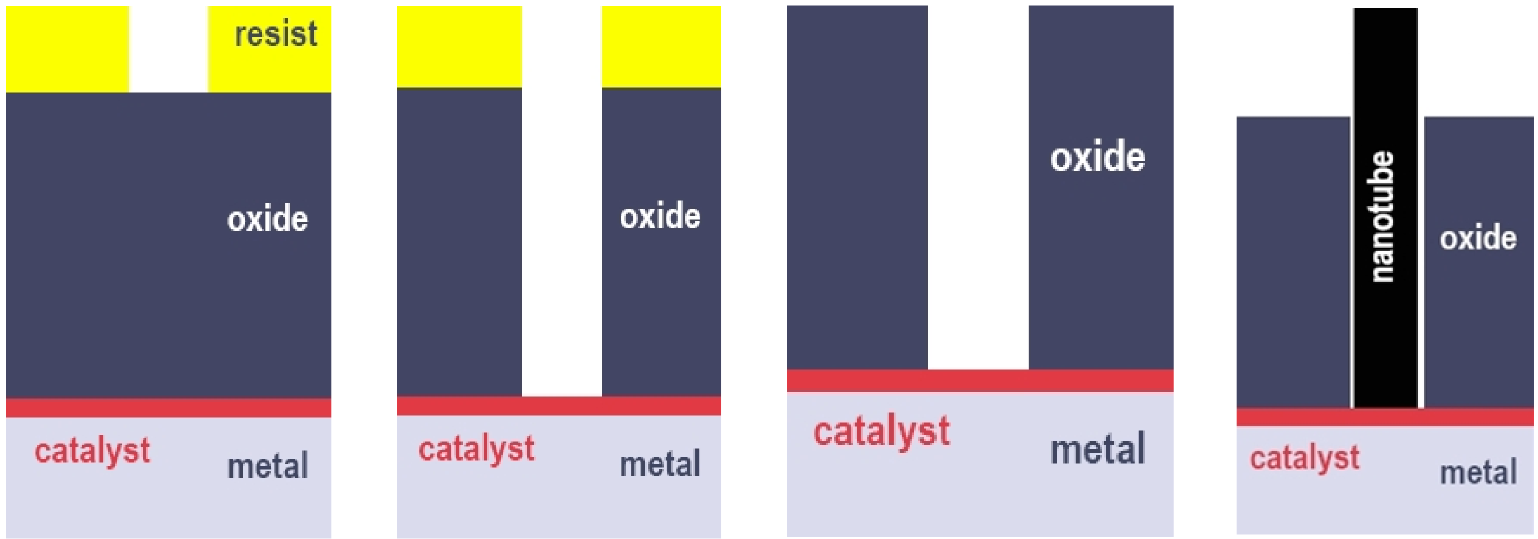
Challenges: i) sidewall deposition causes sidewall CNT growth---via filled but no electrical contact to the bottom!

ii) catalyst thickness and nucleation depends strongly on surface condition after etch, results are irreproducible….

Fabrication Techniques & Challenges-II

[Graham et. al., *Diamond and Related Materials*, 2004, Liebau et al., *AIP P.*, Kirchberg, 2004]

- Buried catalyst layer
- Etching of via stops on top of 1-3 nm thick catalyst layer



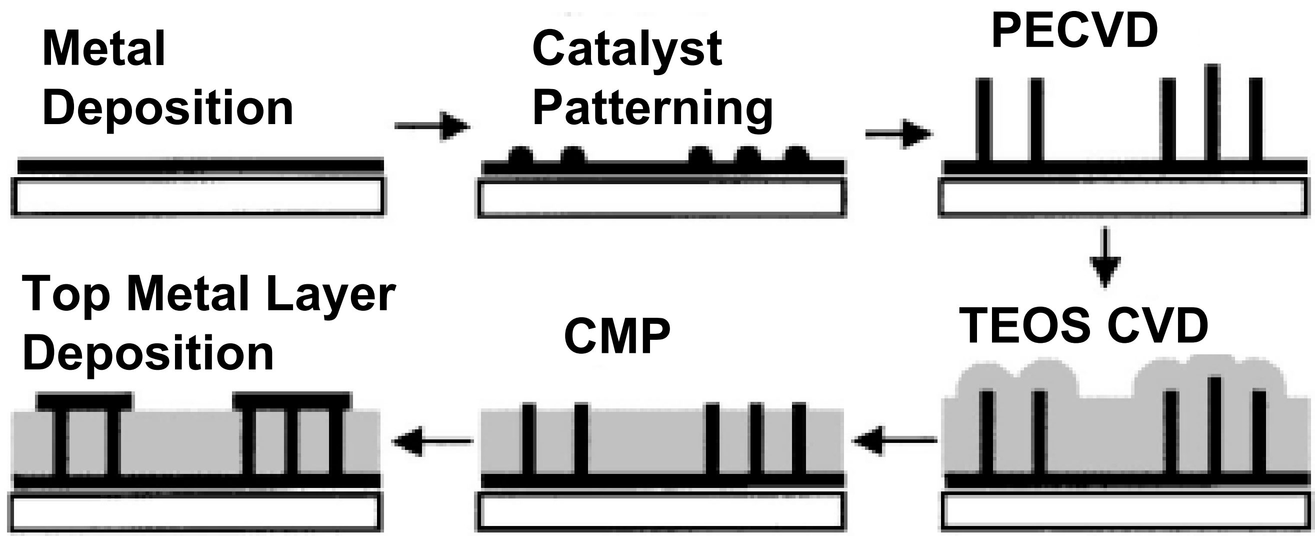
Via definition by resist | Via etch stop on catalyst | Resist strip | Nanotube growth

Challenges: i) etch stop on thin catalyst layer is critical
ii) Wafer/chip scale homogeneity not yet demonstrated

Fabrication Techniques & Challenges-III

- Overcomes the need for etching high aspect ratio vias needed in future technologies
- Can reliably grow MWCNT bundles

[Li et. al., (NASA) *APL*, 2003]



Challenges: i) quality of CNTs is low and so is electrical conductivity
ii) tilt for small diameter tubes is also considerable---subsequent litho step is difficult

CNT Integration Issues

- **Process Advantages vis-à-vis Copper**
  - **Diffusivity into Si/dielectric is not a problem---no need for barrier**
  - **Bottom-up growth processes can eliminate the need for etching high aspect ratio vias**
- **Key Issues:**
  - **Difficult to grow dense metallic SWCNT bundles**
  - **Most interconnect processes so far employ MWCNTs which have been easier to grow--recently it has become possible to grow bundles of SWCNTs also by adding water or oxygen to increase activity (to 84%) of the growth catalyst**
    - [Futaba et al., *J. Phys. Chem. B*, 2006]
  - **High temperatures involved in CNT growth**
  - **Metal-CNT contact resistance**
  - **Control over growth mode (substrate-catalyst interaction)**

Summary: Dense CNT Bundle vs Cu

	Local	Intermediate	Global	Via/Contact
Performance	**Exceeds Cu**	**Exceeds Cu**	**Exceeds Cu**	**Comparable to Cu**
Power	**---**	**---**	**Comparable to or less than Cu**	**---**
Reliability	**Far superior to Cu**	**Far superior to Cu**	**Far superior to Cu**	**Far superior to Cu**
Process Tech Requirement	**Dense metallic SWCNT bundle; Low contact res.**	**Dense metallic SWCNT bundle**	**Dense metallic SWCNT bundle**	**Dense metallic SWCNT bundle; Low contact res.**

CNT interconnects look promising….

Process development and modeling must happen concurrently…..a lot of work still remains!!