ECE 225
High-Speed Digital IC Design
Lecture 10

CMOS Devices: Alpha-power Model, Sub-micron Effects, Leakage Mechanisms, Parasitic Effects

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Alpha-Power MOSFET Model

T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its application to CMOS inverter delay and other formulas," IEEE J. Solid-State Circuits, vol. 25, pp. 584–593, 1990.

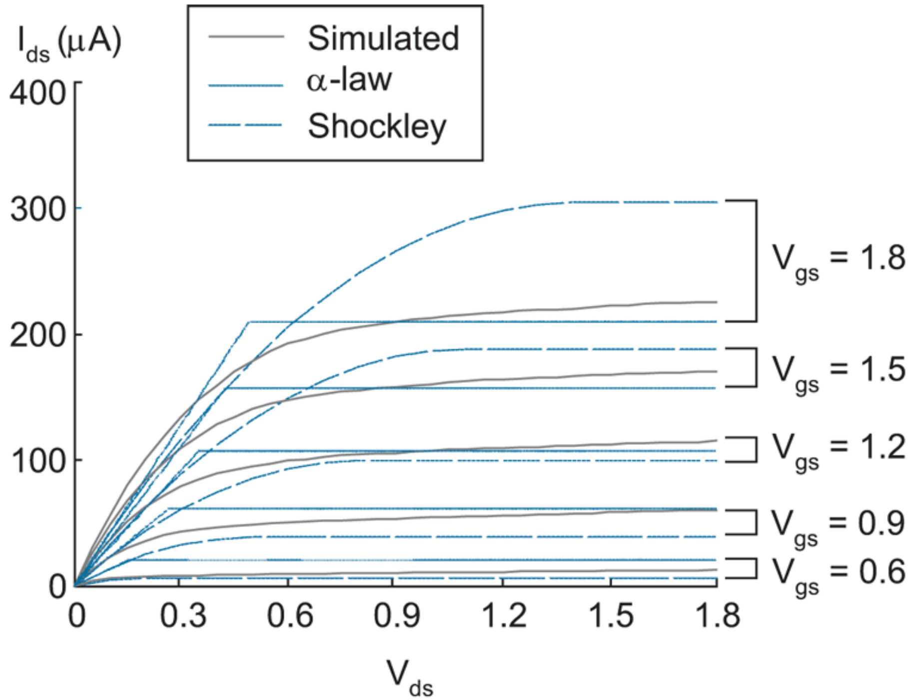


FIG 2.17 I-V characteristics for nMOS transistor with velocity saturation

At low lateral E-fields, V_{ds}/L, current increases linearly with E-field

At high fields, E= E_{sat}

Carrier velocity saturates due to carrier scattering = v_{sat} (= μE_{sat})

$I_{ds} = \mu C_{ox} W/L (V_{gs} - V_t)^2$

---no velocity saturation

$I_{ds} = C_{ox} W (V_{gs} - V_t) v_{sat}$

---complete velocity saturation

Practical situation: carrier velocity doesn't increase linearly with field but is not completely velocity saturated….

Sakurai Model: $I_{ds} \propto (V_{gs} - V_t)^{\alpha}$

1<α<2, is the velocity saturation index, determined by curve fitting…..also accounts for mobility degradation due to high vertical field (V_{gs}/t_{ox})

The Sub-Micron MOS Transistor

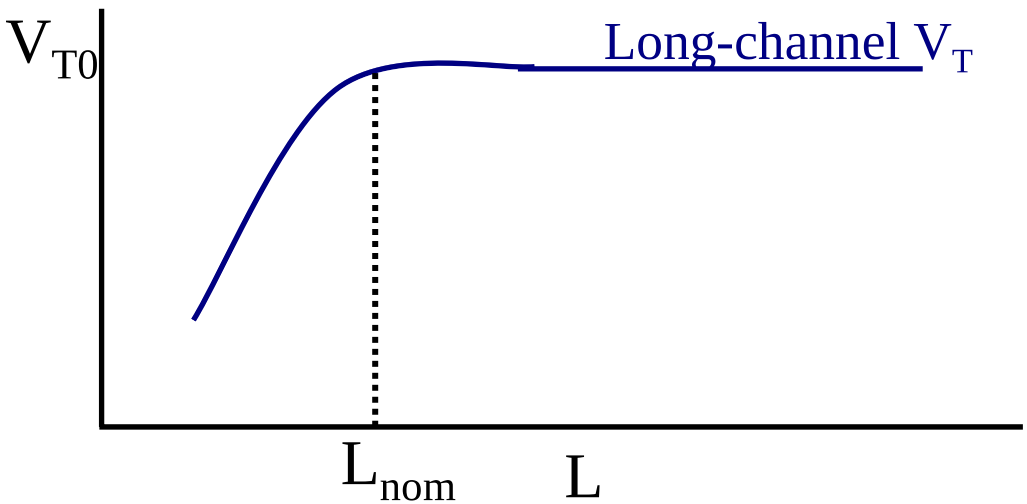
- Short-Channel Effects:
  - Threshold Voltage Dependence on L
  - DIBL
- Leakage Mechanisms
- Parasitic Resistances

Threshold voltage dependence on L

- Until now, threshold voltage assumed constant
  - V_T changed only by substrate bias V_{SB}
- In threshold voltage equations, channel depletion region assumed to be created by gate voltage only
- Depletion regions around source and drain neglected: valid if channel length is much larger than depletion region depths
- In short-channel devices, depletion regions from drain and source extend into channel

Threshold voltage roll-off…

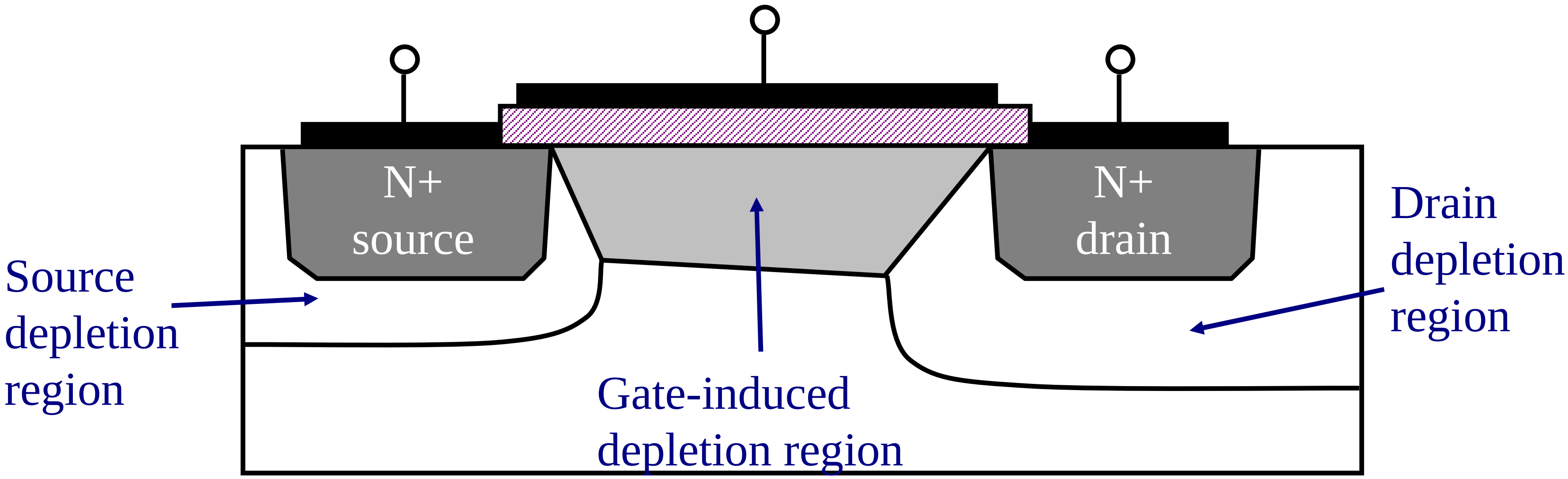
Graphically: V_{T0} versus channel length L



V_T Roll-off:

V_T decreases rapidly with channel length

Reason for Vt Roll-Off….



- Even with V_{GS}=0, part of channel is already depleted
- Bulk depletion charge is smaller in short-channel device → V_t is smaller

Threshold voltage roll-off….

- Change in V_{t0}:
  - x_{dS}, x_{dD}: depth of depletion regions at S, D
  - x_j: junction depth

$$\Delta V_{t0} = \frac{1}{C_{ox}}\sqrt{2q\varepsilon_{Si}N_A|2\phi_F|} \bullet \frac{x_j}{2L}\left[\left(\sqrt{1+\frac{2x_{dS}}{x_j}}-1\right)+\left(\sqrt{1+\frac{2x_{dD}}{x_j}}-1\right)\right]$$

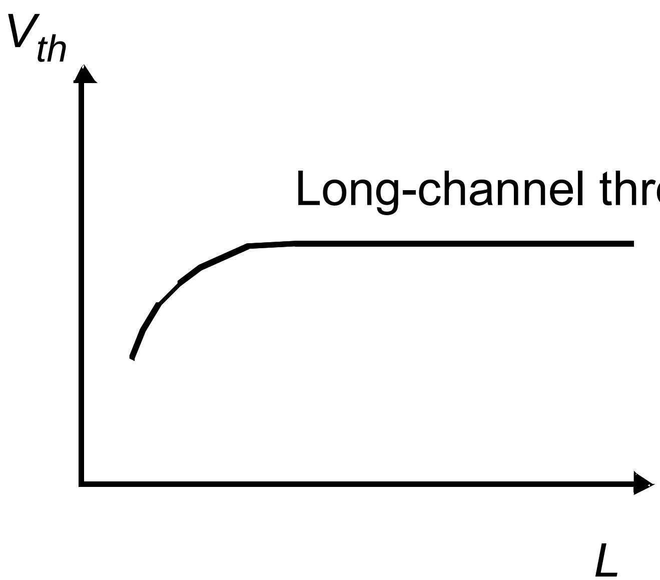
- ΔV_{t0} is proportional to (x_j/L)
  - For short channel lengths, ΔV_{t0} is large
  - For large channel lengths, term approaches 0

DIBL

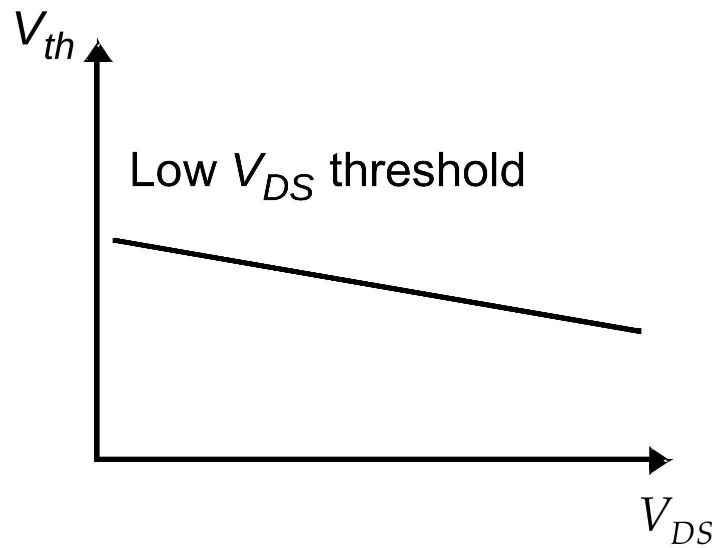
- Drain-induced barrier lowering (DIBL)
  - Drain voltage V_{DS} causes change in threshold voltage
  - As V_{DS} is increased, threshold voltage decreases
- Cause: depletion region around drain
  - Depletion region depth around drain depends on drain voltage
  - As V_{DS} is increased, drain depletion region gets deeper and extends further into channel
  - For very large V_{DS}, source and drain depletion regions can meet → *punch-through*!
- Issue: results in uncertainty in circuit design

Effect of SCE and DIBL on Vth…..

- $V_{th} = V_{th\_long\text{-}channel}$ – SCE - DIBL



Threshold as a function of the length (for low V_{DS})



Drain-induced barrier lowering (DIBL) (for low L)

Threshold voltage variation

Short-channel effects cause threshold voltage variation:

- V_t rolloff
  - As channel length L decreases, threshold voltage decreases
- Drain-induced barrier lowering
  - As drain voltage V_{DS} increases, threshold voltage decreases
- Hot-carrier effect
  - Threshold voltages drift over time
- Negative-Bias Temperature Instability (NBTI)
  - Issue in PMOS transistors
  - Vt drifts over time
  - Typical stress temperature 100-150 C
  - Typical oxide electric fields of 5-6 MV/cm

Threshold voltage variation

- Hot-carrier effect
  - increased electric fields causes increased electron velocity
  - high-energy electrons can tunnel into gate oxide
  - This changes the threshold voltage (increases V_t for NMOS)
  - Can lead to long-term reliability problems

Threshold voltage variation

- Hot electrons
  - High-velocity electrons can also impact the drain, dislodging holes
  - Holes are swept towards negatively-charged substrate → cause substrate current
  - Called *impact ionization*
  - This is another factor which limits the process scaling → voltage must scale down as length scales

Threshold voltage variations

- Summary of threshold variations in short-channel devices
  - V_t rolloff: threshold voltage reduces as channel length L reduces
  - DIBL: threshold voltage reduces as V_{DS} increases
  - Hot-carrier effect: threshold voltage drifts over time as electrons tunnel into oxide
  - NBTI—causes Vt increase in PMOS transistors, strong dependence on Temperature.

Subthreshold Leakage

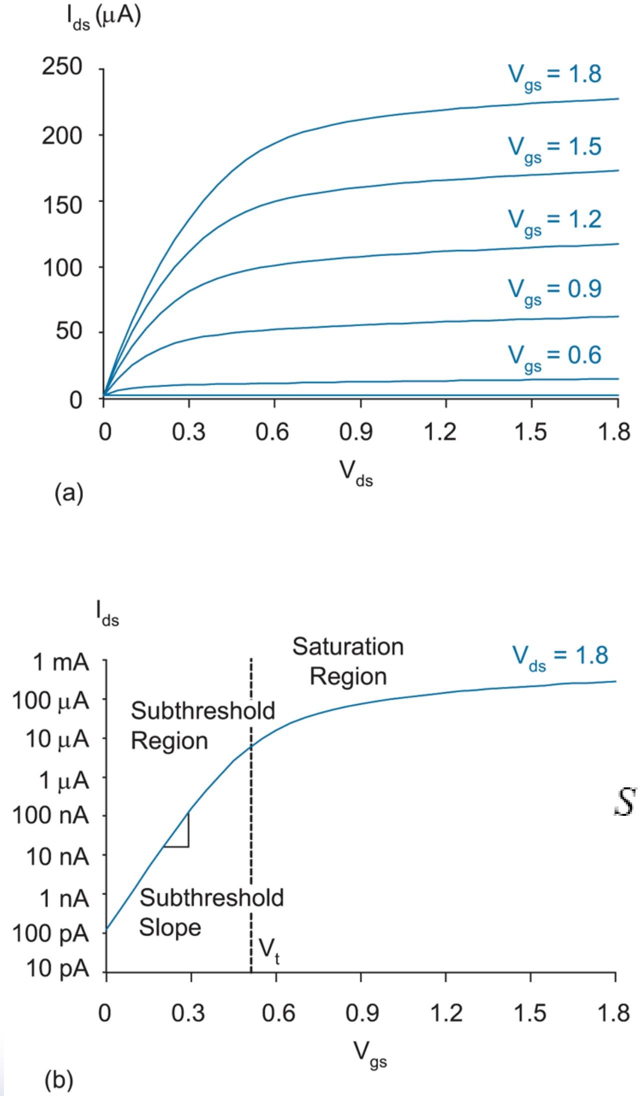


FIG 2.15 Simulated I-V characteristics

- *Dominant leakage mechanism*
- *Increases exponentially with temperature and Vt*

$$S = \left(\frac{d(\log I_d)}{dV_g} \right)^{-1} = \left(\frac{\partial V_g}{\partial \psi_s} \right) \left(\frac{\partial \psi_s}{\partial (\log I_d)} \right) = \left(1 + \frac{C_{dm}}{C_{ox}} \right) \frac{kT}{q} \ln(10)$$

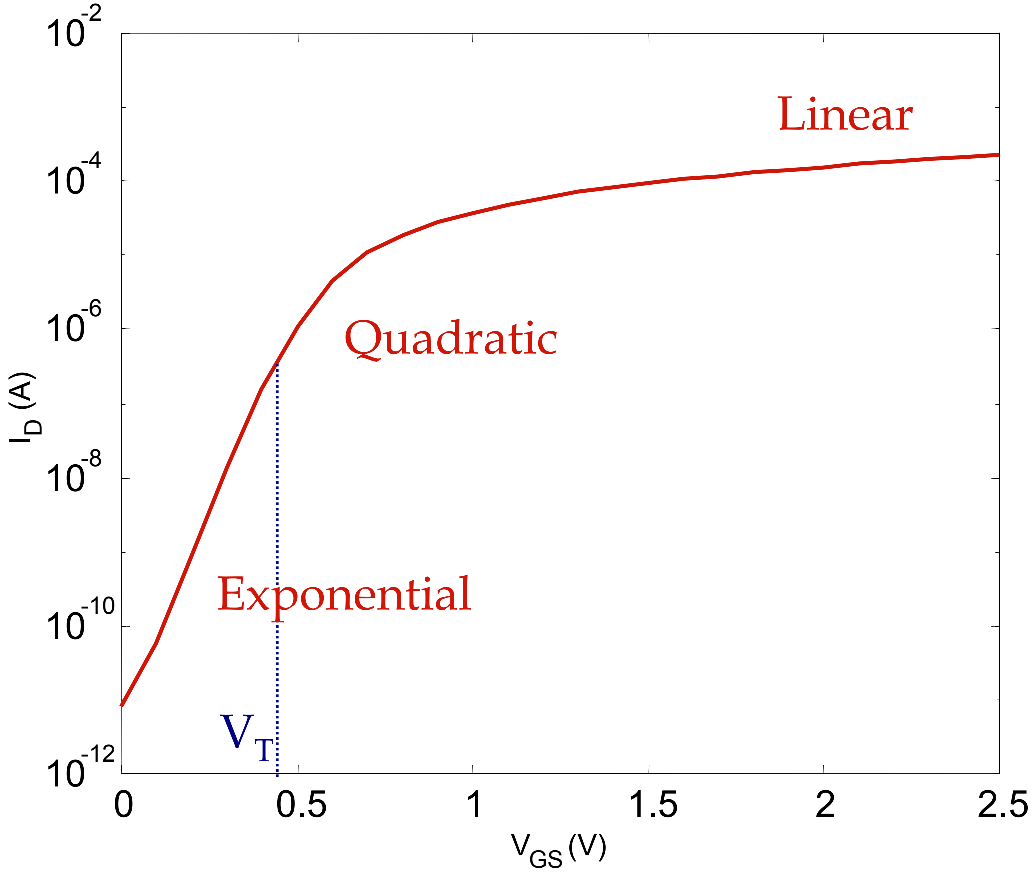
Sub-threshold conduction (1)

- When $V_{GS} < V_T$, transistor is “off”
  - However, small drain current I_D still flows
  - Called *subthreshold leakage* current
- Model for subthreshold current:

$$I_D(subthreshold) = I_S W e^{\frac{q}{kT}(AV_{GS} + BV_{DS})}$$

  - Increases as V_{GS} increases (potential barrier lowered)
  - Increases as V_{DS} increases (DIBL)

Sub-Threshold Conduction (2)



The Slope Factor

$$I_D \sim I_0 e^{\frac{qV_{GS}}{nkT}}, \quad n = 1 + \frac{C_D}{C_{ox}}$$

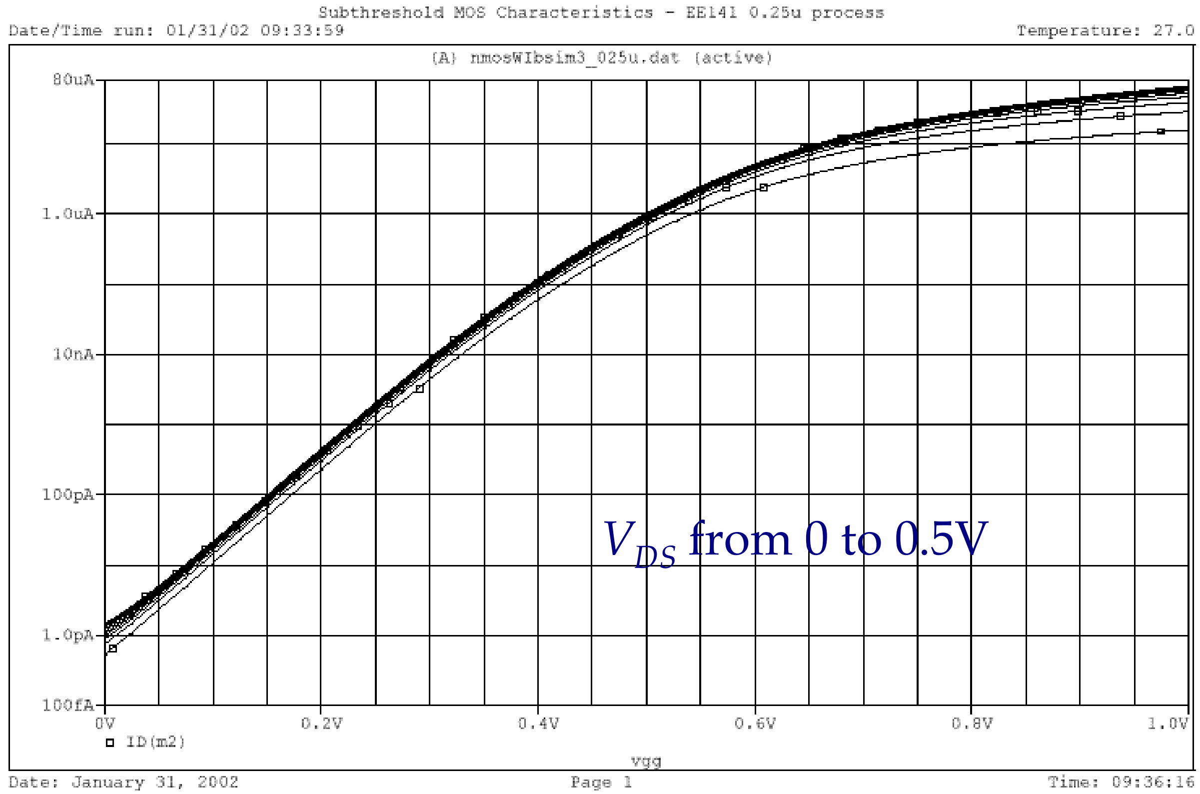
S is ΔV_{GS} for $I_{D2}/I_{D1} = 10$

$$S = n\left(\frac{kT}{q}\right)\ln(10)$$

Typical values for S:
60 .. 100 mV/decade

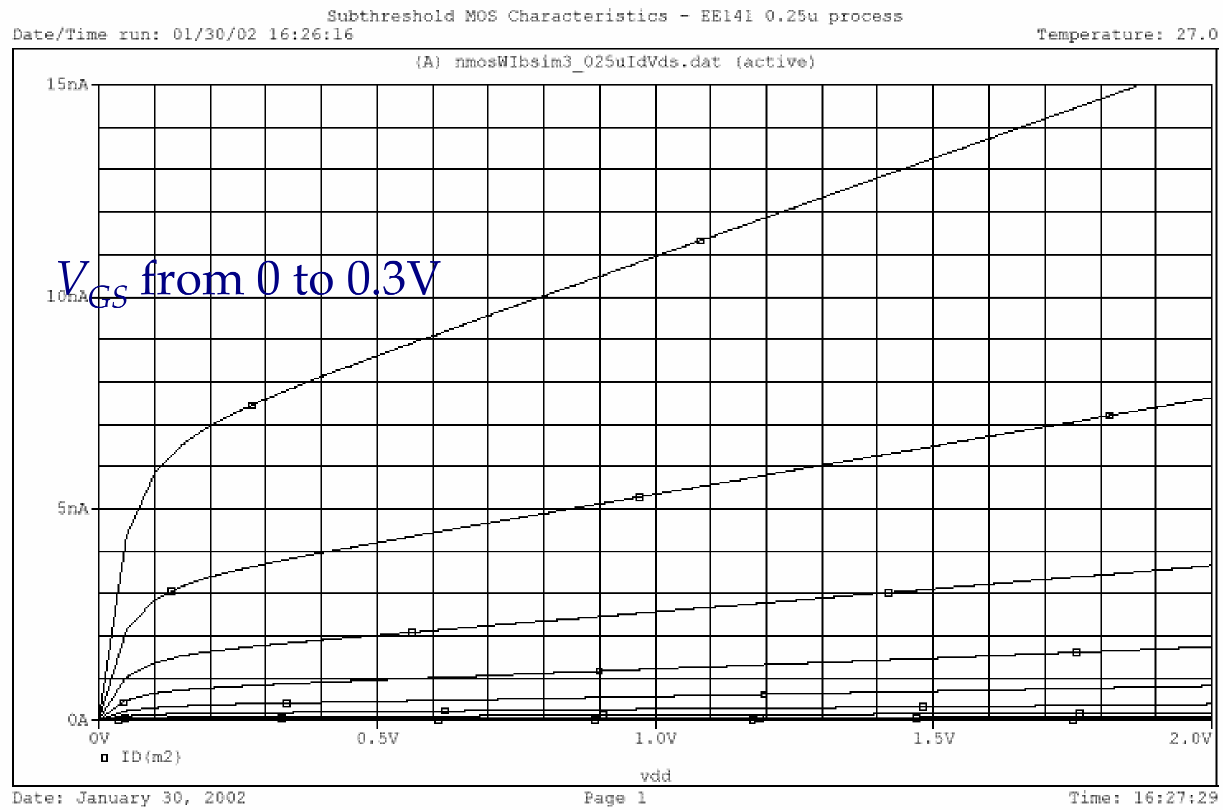
Sub-Threshold I_D *vs* V_{GS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}}\left(1 - e^{-\frac{qV_{DS}}{kT}}\right)$$



Sub-Threshold I_D *vs* V_{DS}

$$I_D = I_0 e^{\frac{qV_{GS}}{nkT}} \left(1 - e^{-\frac{qV_{DS}}{kT}} \right) \left(1 + \lambda \cdot V_{DS} \right)$$



Gate Leakage

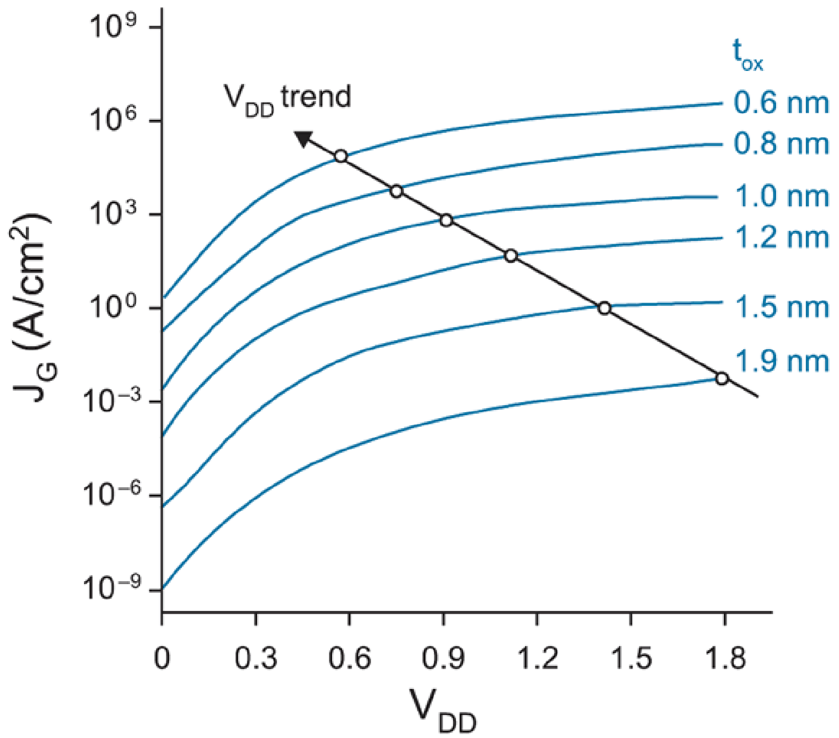


FIG 2.20 Gate leakage current from [Song01]

- *Increases with gate oxide (SiO2) scaling*
- *High-k gate oxides can be used to lower gate leakage*
- *Independent of temperature*

Junction Leakage

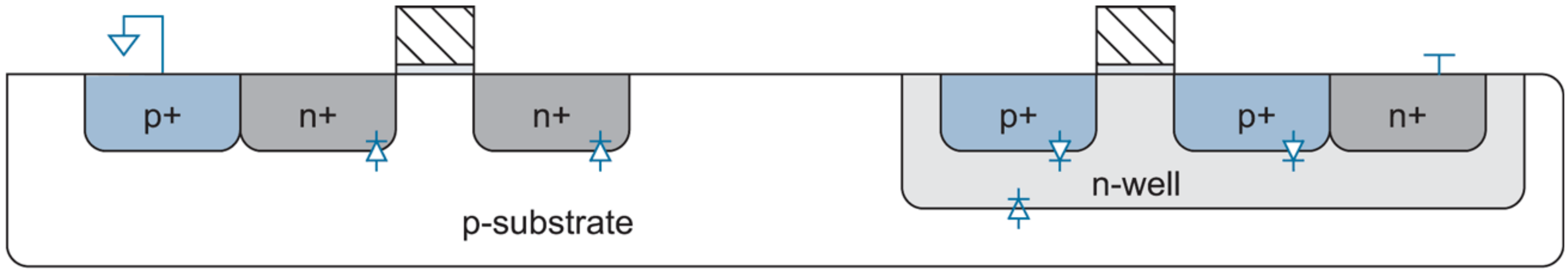


FIG 2.19 Reverse-biased diodes in CMOS circuits

- *Less significant than gate and subthreshold leakage*
- *Increases with temperature*

Leakage

- Effect of leakage current
  - "Wasted" power: power consumed even when circuit is inactive
  - Leakage power raises temperature of chip
  - Can cause functionality problem in some circuits: memory, dynamic logic, etc.
- Reducing transistor leakage
  - Long-channel devices
  - Small drain voltage
  - Large threshold voltage V_T

Leakage

- Leakage vs. performance tradeoff:
  - For high-speed, need small V_T and L
  - For low leakage, need high V_T and large L
- Process scaling
  - V_T reduces with each new process (historically)
  - Leakage increases ~10X!
- One solution: dual-V_T process
  - Low-V_T transistors: use in critical paths for high speed
  - High-V_T transistors: use to reduce power

Temperature Effects

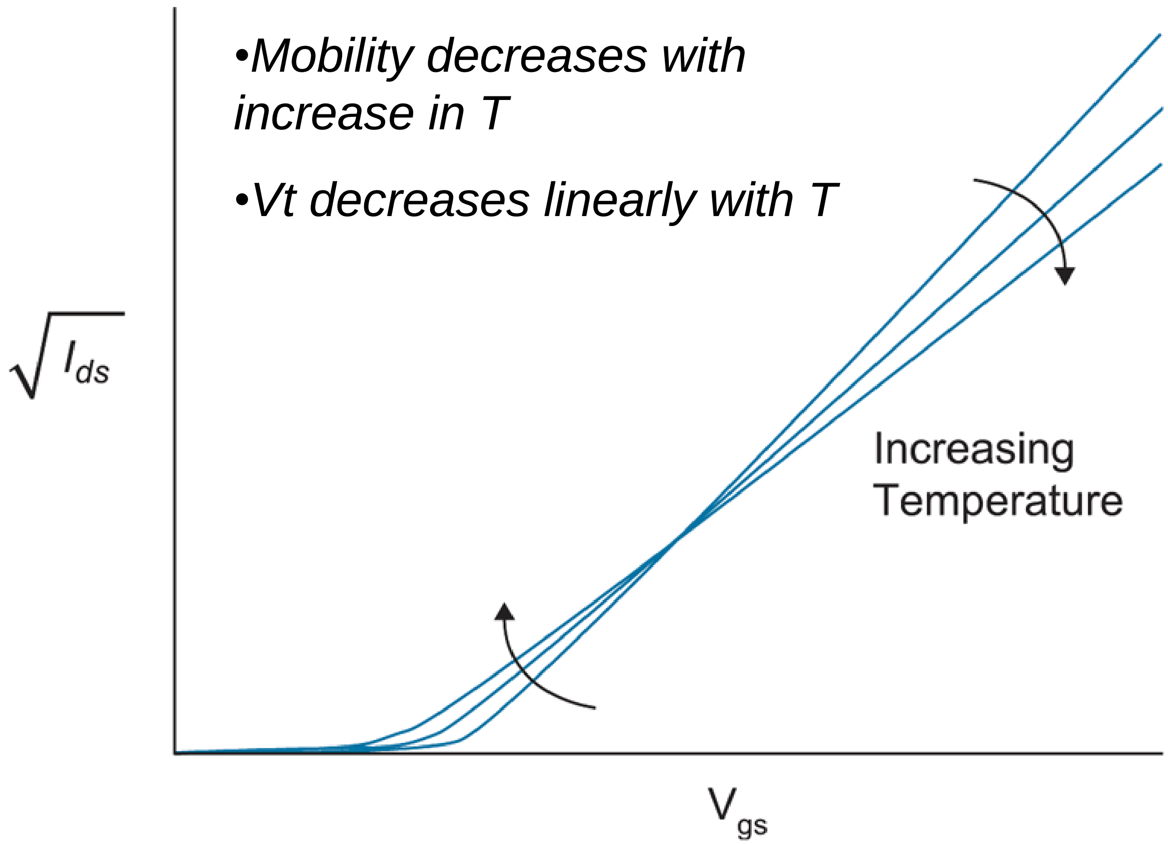


FIG 2.21 I–V characteristics of nMOS transistor in saturation at various temperatures

What happens in ultra low-voltage designs?

See paper by Sakurai…

Temperature Effects

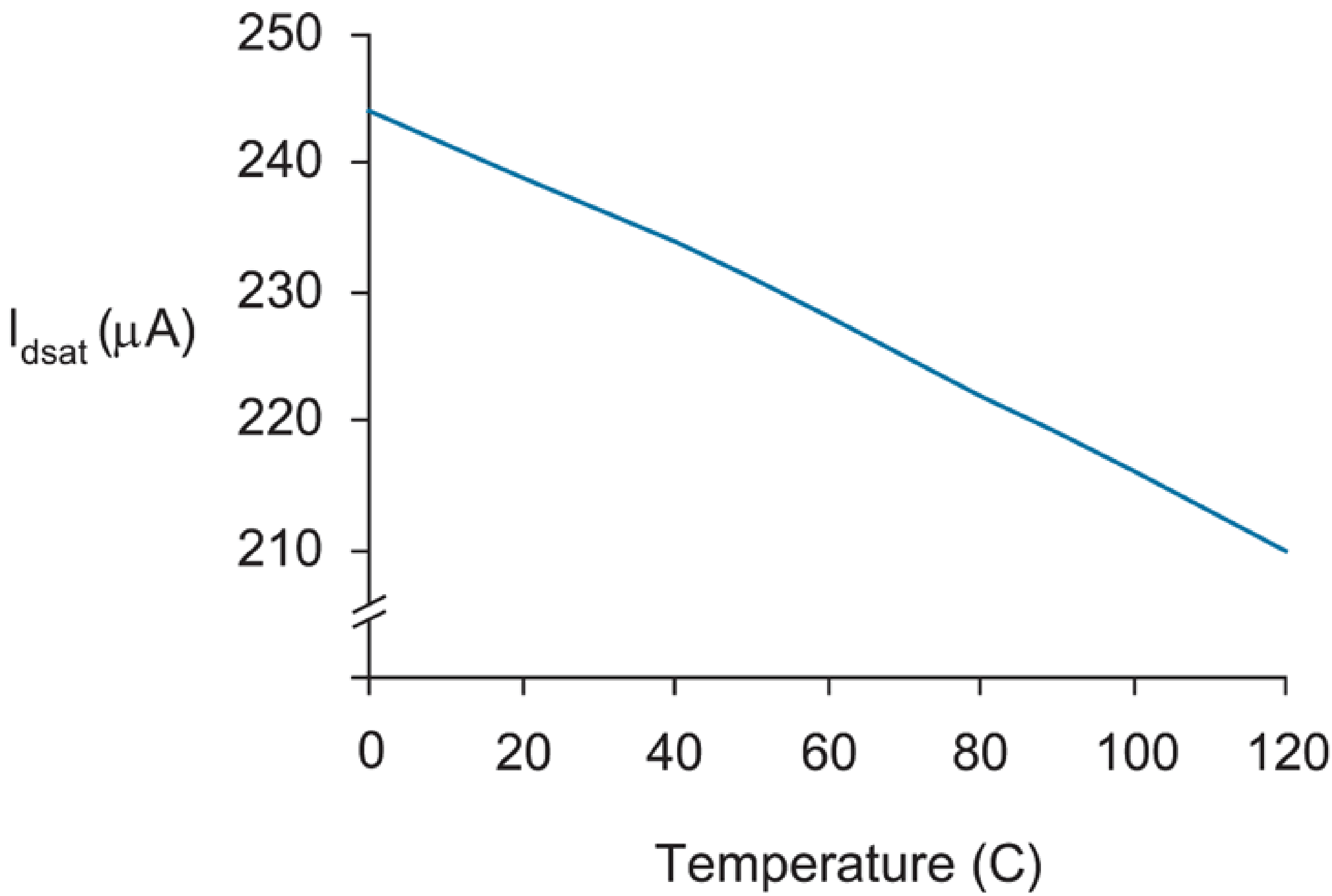


FIG 2.22 I_{dsat} vs. temperature

Temperature Effects

S-C. Lin and K. Banerjee, "Cool Chips: Opportunities and Implications for Power and Thermal Management", IEEE Transactions on Electron Devices, vol. 55, No. 1, 2008, 245-255.

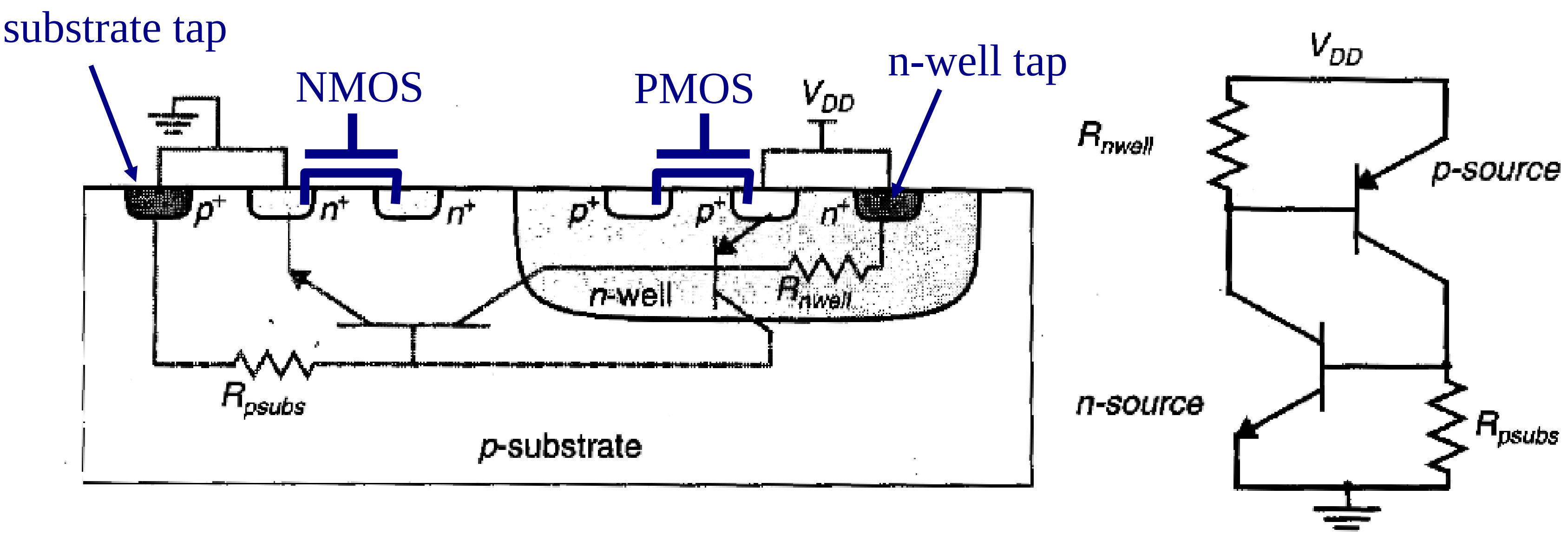
Chip Cooling can:

1. *Improve Circuit performance*
   - *speed up transistors*
   - *decrease the delay of interconnects since metal resistance decreases with temperature*
   - *Lowers junction capacitance (increases depletion width)*
2. *Decrease leakage (mainly subthreshold)*
3. *Improve reliability of the chip*

Latchup

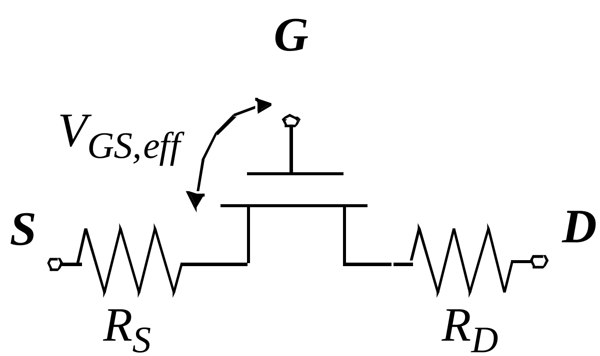
- CMOS process contains parasitic bipolar transistors
- Under certain conditions, these parasitic transistors can turn on, shorting power and ground rails and usually destroying the chip → *latchup*
- Avoiding latchup requires certain layout design rules, and careful control of process
- Latchup was a major problem in early CMOS processes
- Now, latchup is mainly issue for I/O circuits, with high current demands and possibly noisy voltages

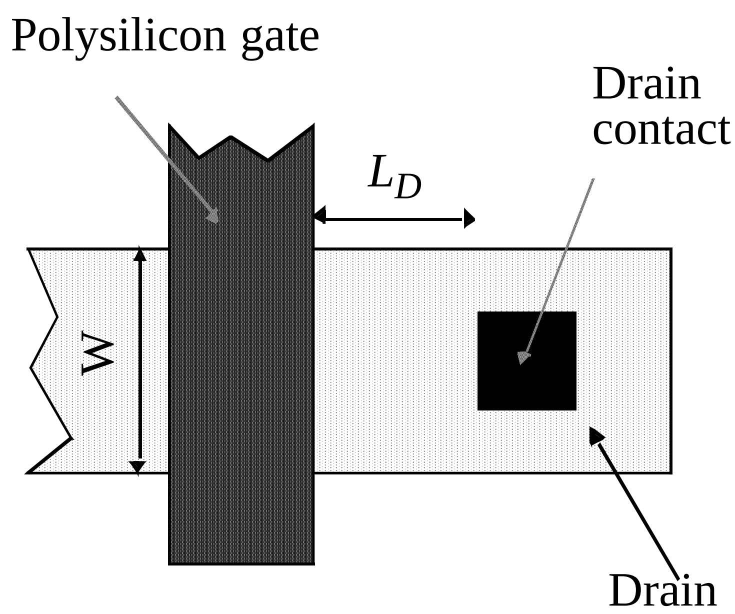
Latchup



- Current flowing in well or substrate can forward-bias bipolar transistor
- Positive feedback between transistors: when one turns on, V_{dd} and Gnd are connected
- Solution: reduce R_{nwell} and R_{psubs}: use many substrate taps in layout
- High-current circuits use *guard rings*

Parasitic Resistances





*Problem can be alleviated by silicided source/drain contacts….but still needs S/D contact engineering….**see D. Scott in JSSC, 1982.***

*Silicide thickness is an important factor….**see K. Banerjee et al., IEDM 97.***