ECE 225
High-Speed Digital IC Design

Lecture 16

Latch based Design, Clock Synthesis and Synchronization

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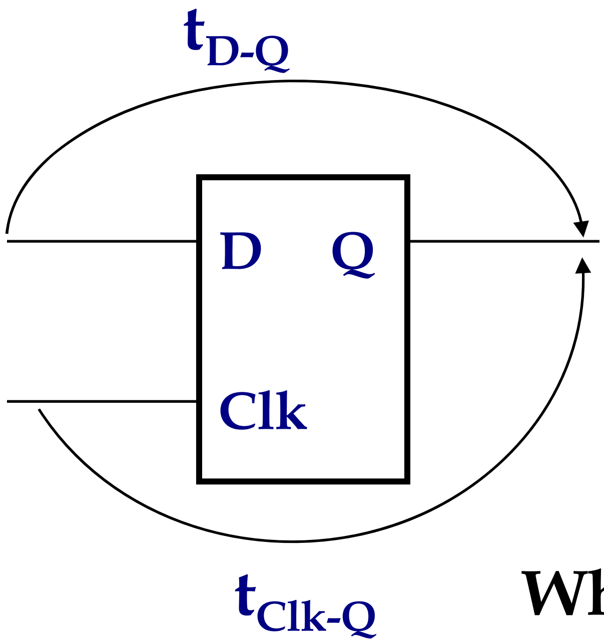
Latch timing



When data arrives to transparent latch

Latch is a 'soft' barrier

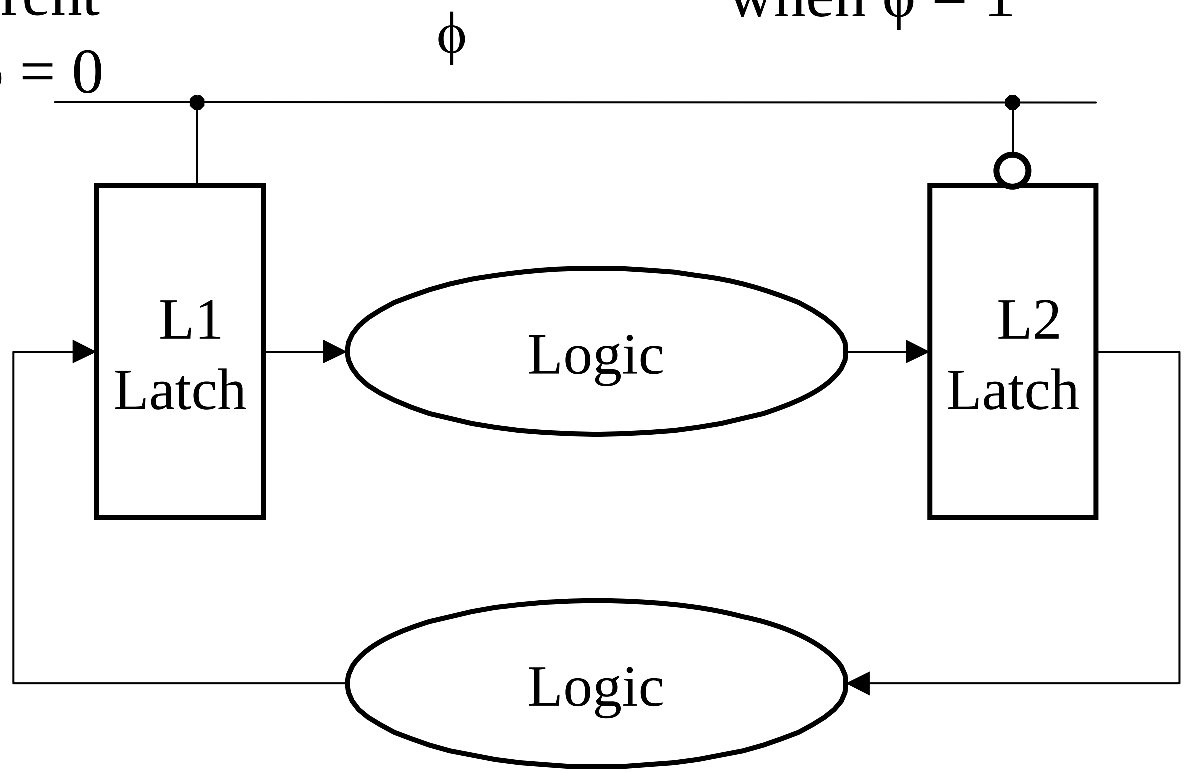
When data arrives to closed latch

Data has to be 're-launched'

Latch-Based Design

L1 latch is transparent when $\phi = 0$

L2 latch is transparent when $\phi = 1$

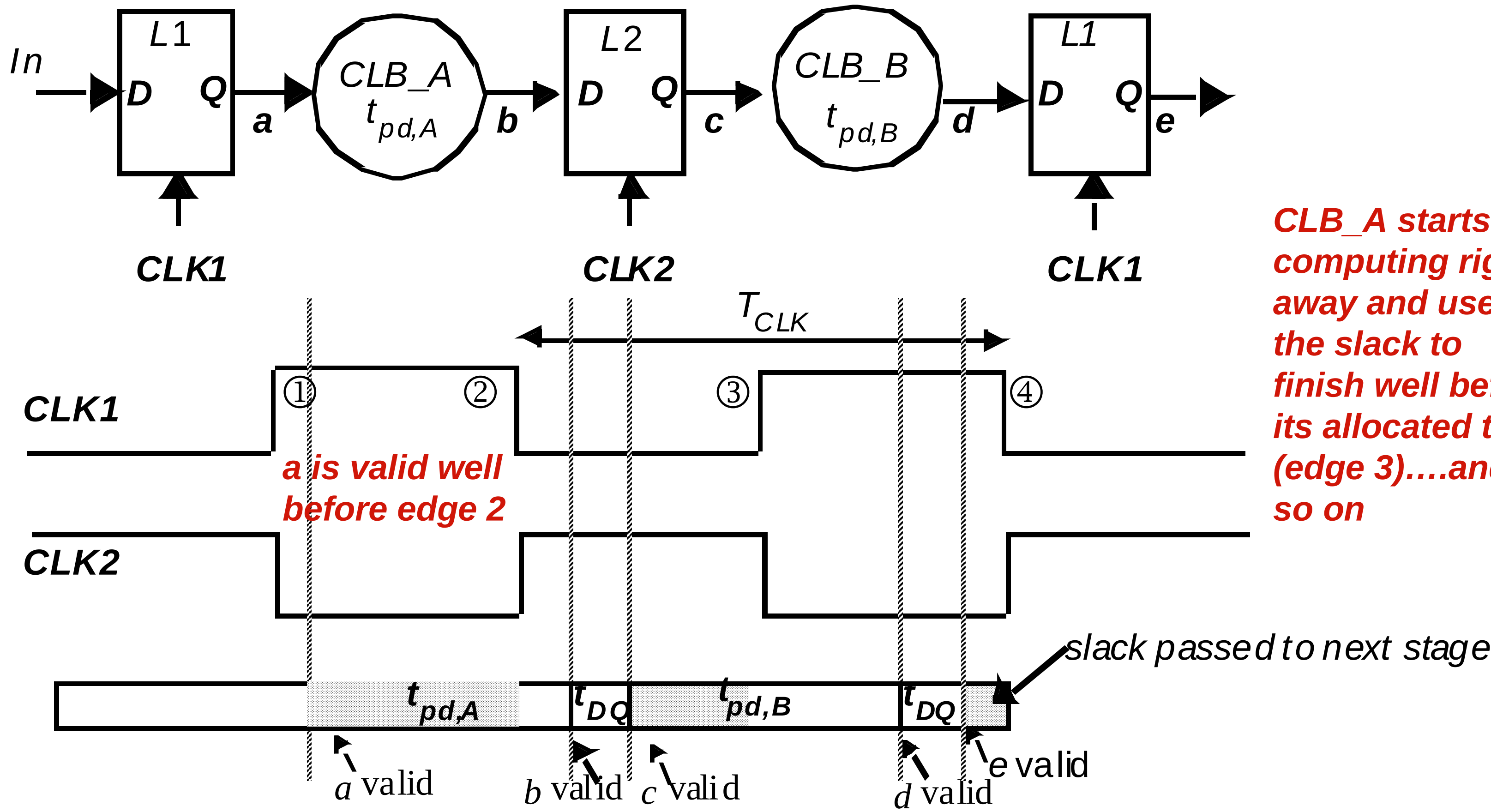


Register vs Latch Based Clocking…

- In an edge-triggered system, the worst case logic path between two registers determines the minimum CLK period for the entire system….
- If the logic block finishes before the end of the CLK period, it has to sit idle until the next CLK edge…
- Latch based design offers more flexibility….one stage can *pass slack* or *borrow time* from other stages…

Slack-borrowing

In a latch based system, it is possible for a logic block to utilize time that is left from a previous logic block…

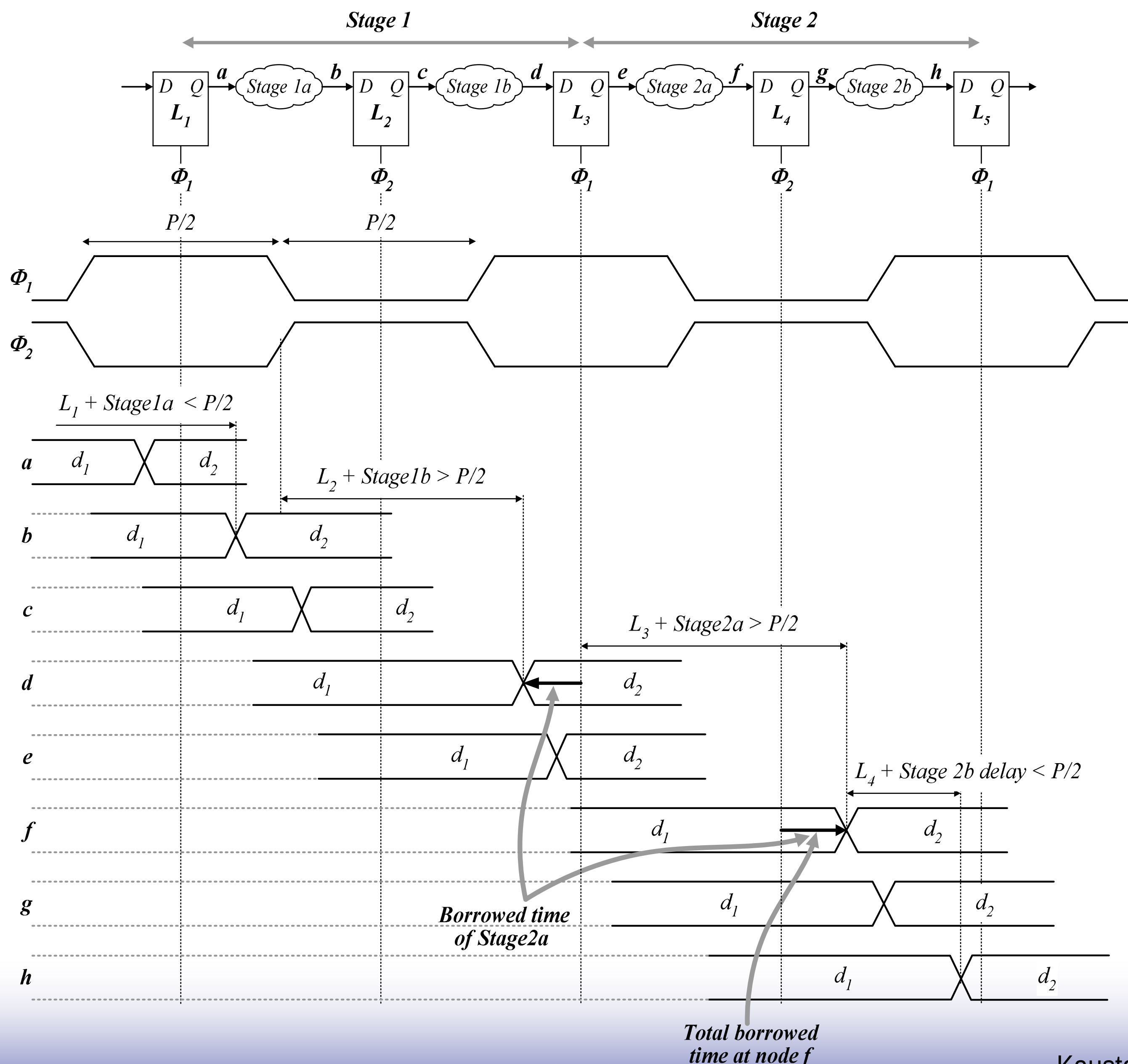


CLB_A starts computing right away and uses the slack to finish well before its allocated time (edge 3)….and so on

If $T_{clk} < t_{pd,A} + t_{pd,B}$ -----slack-passing has taken place

$T_{clk}/2$ = maximum time that can be borrowed from previous stage

Timing of two-phase level-sensitive pipeline with time borrowing

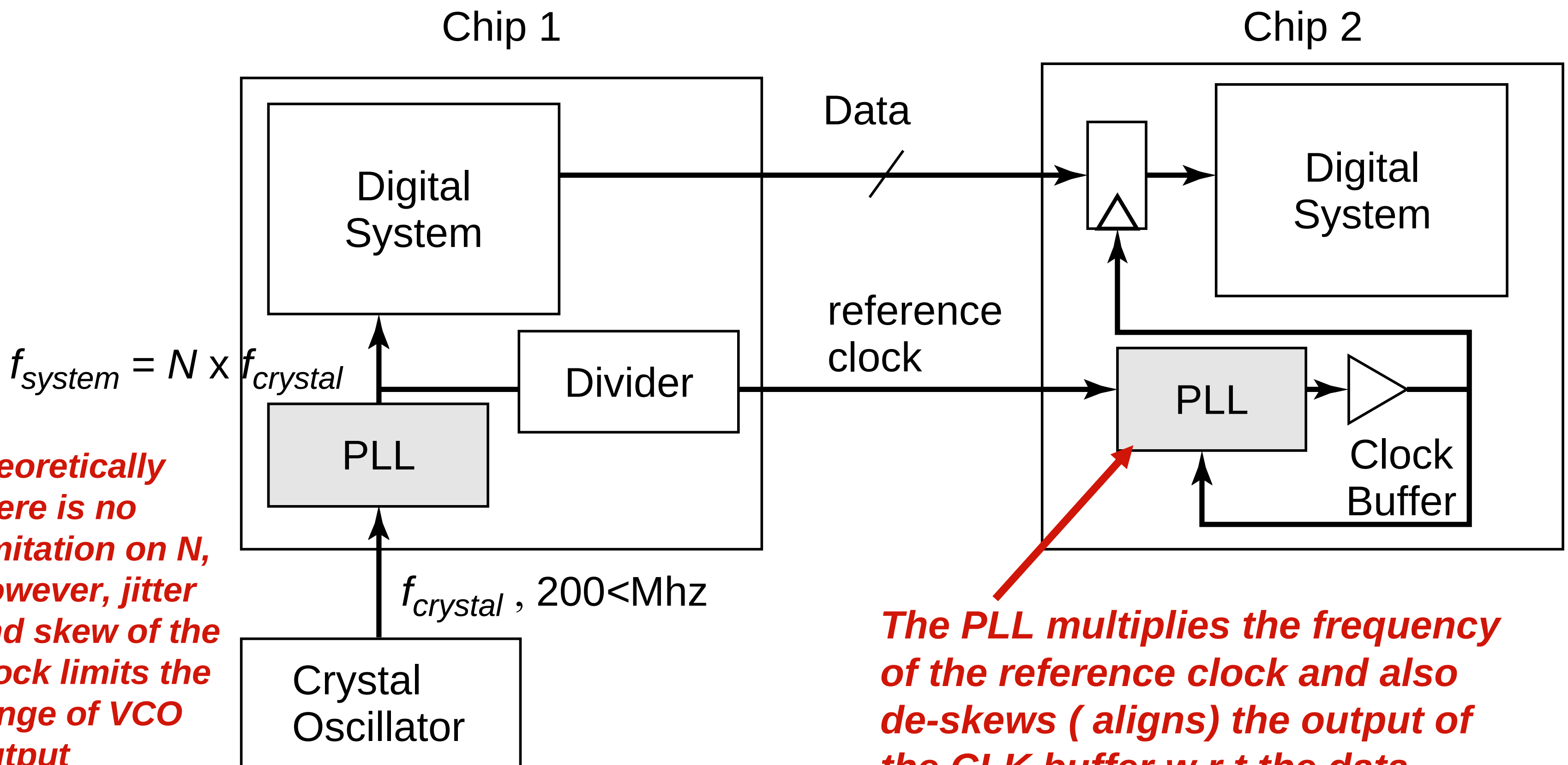


Clock Synthesis and Synchronization

- Synchronous circuits require a global periodic clock
- Microprocessor CLK frequencies are in the GHz range
- Crystal oscillators have low frequency: 10's of MHz to approx. 200 MHz
- A Phase Locked Loop (PLL) is used to generate the high frequency---multiplies the low oscillator frequency by a a rational number N

PLL-Based Synchronization

PLLs are also used to synchronize communication between chips….

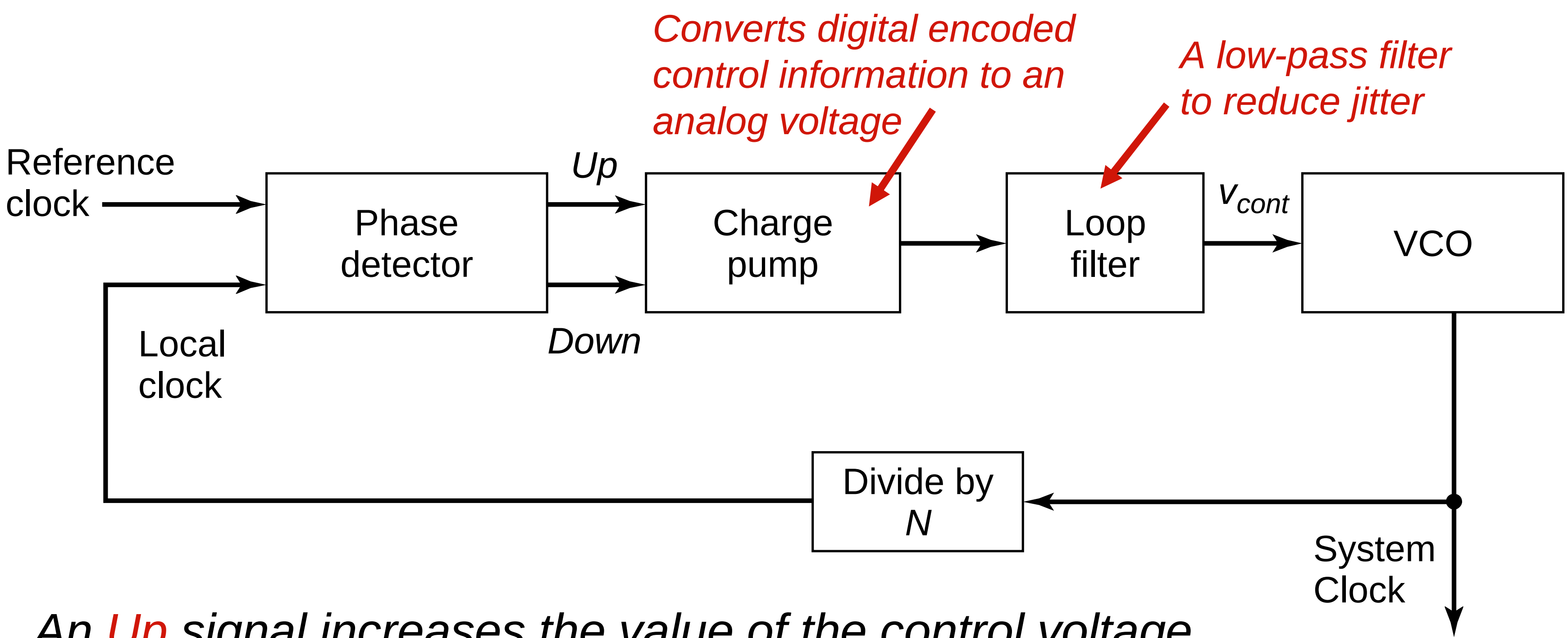


theoretically there is no limitation on N, however, jitter and skew of the clock limits the range of VCO output frequency….

The PLL multiplies the frequency of the reference clock and also de-skews (aligns) the output of the CLK buffer w.r.t the data

PLL Block Diagram

PLL is a complex non-linear feedback circuit…



An Up signal increases the value of the control voltage and speeds up the VCO, which causes the local signal to catch up with the reference clock.

A Down signal slows down the VCO and eliminates the phase lead of the local CLK

Loop Acquisition

- When an external signal enters the phase comparator it mixes with the VCO output signal.

- Initially the two frequencies are not equal and the loop is unlock.

- Because the phase comparator is a non-linear device, the external and VCO output signals mix and produces cross-products frequencies (i.e., sum and differences).

- The low pass filter blocks the two input frequencies and the sum of their frequencies. The only signal allowed to pass is the difference of the two signal. This signals is sometimes called the beat frequency.

Loop Acquisition

- The beat frequency is amplified and then inputted to the VCO, where it changes the output frequency of the VCO by an amount proportional to its polarity and amplitude.

- As the VCO output frequency changes the, the amplitude and frequency of the beat frequency changes proportionately.

- After several cycles around the loop, the VCO output frequency (divided by N) equals the external frequency, and the loop is said to acquire a lock.

Loop Acquisition

- Once frequency lock has occurred, the beat frequency at the output of the LPF is 0Hz (a dc voltage), and its magnitude and polarity is proportional to the difference in phase between the external signal and the VCO output signal.

- The dc voltage provides an input bias to the VCO, keeping it locked onto the frequency of the external input signal.

- In essence the phase comparator is a frequency comparator until frequency acquisition is achieved, then it becomes a phase comparator.

PLL Capture and Lock Ranges

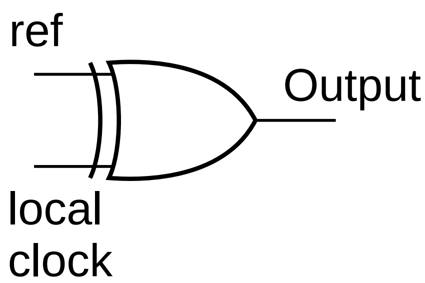
- Capture range is defined as the band of frequencies centered around the VCO natural frequency where the PLL can initially establish or acquire frequency lock with an external input signal from an unlocked condition.

- Lock range is defined as the band of frequencies centered on the VCO's natural frequency over which a PLL can maintain frequency lock with an external input signal.

Capture Range

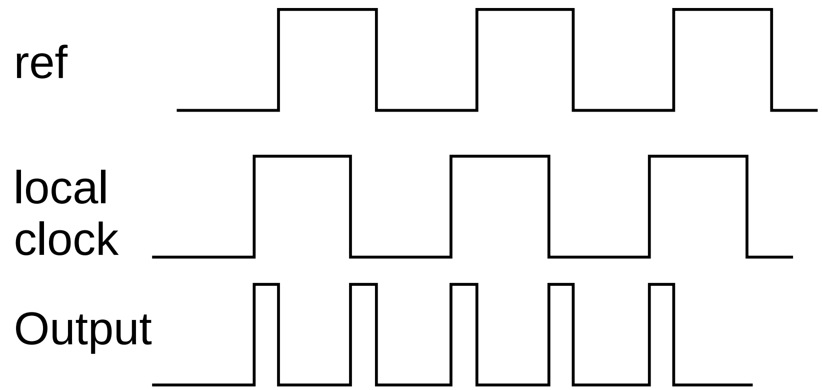
- The capture range is generally between 0.5 and 1.7 times the VCO's natural frequency.
- Capture rage is sometimes called the acquisition range.
- Pull-in range is the capture range expressed as a peak value.
- The lowest frequency the PLL can lock onto is called the lower capture limit (f_{cl}), and the highest frequency the PLL can lock onto is called the upper capture limit (f_{cu}).

Phase Detector

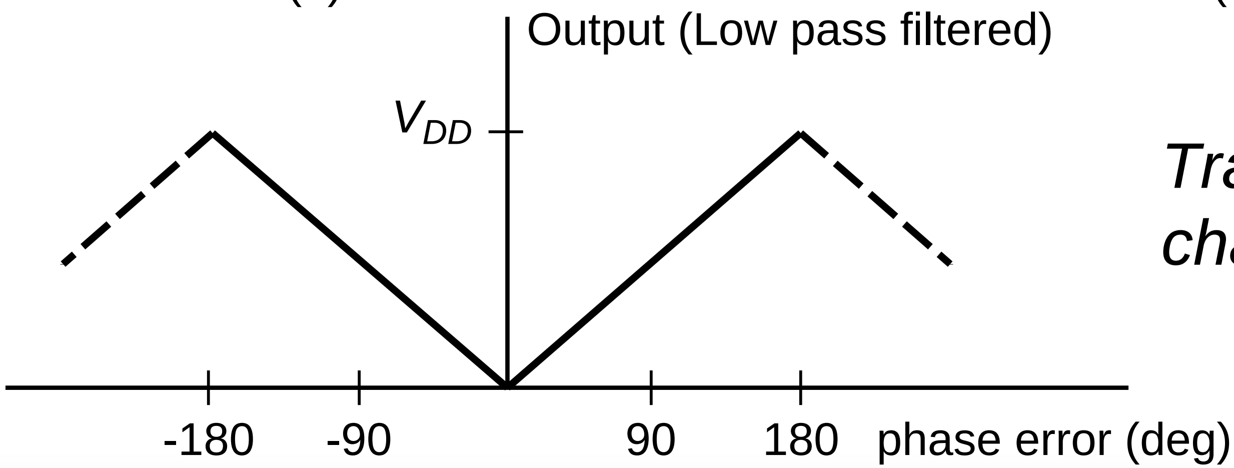


(a)

Output before filtering



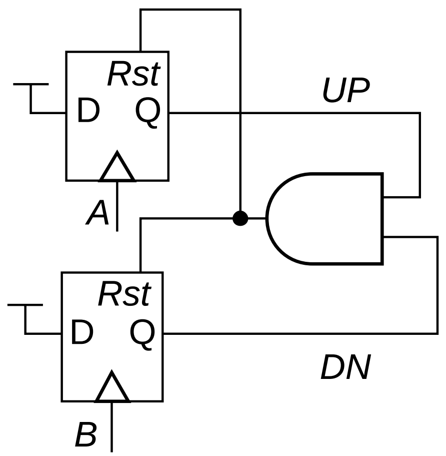
(b)



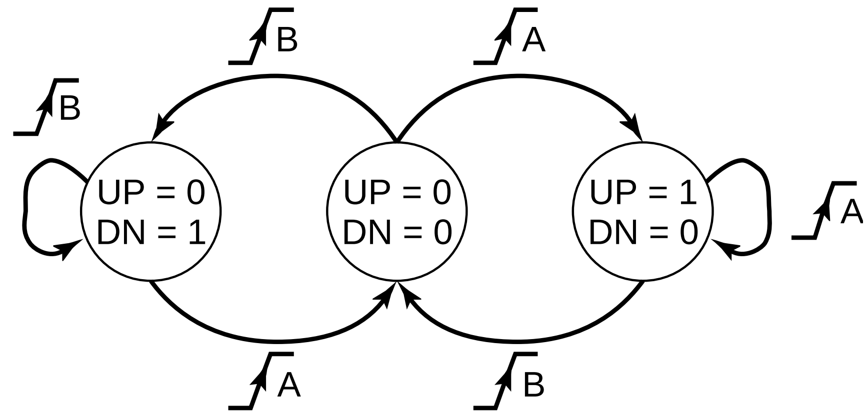
(c)

Transfer characteristic

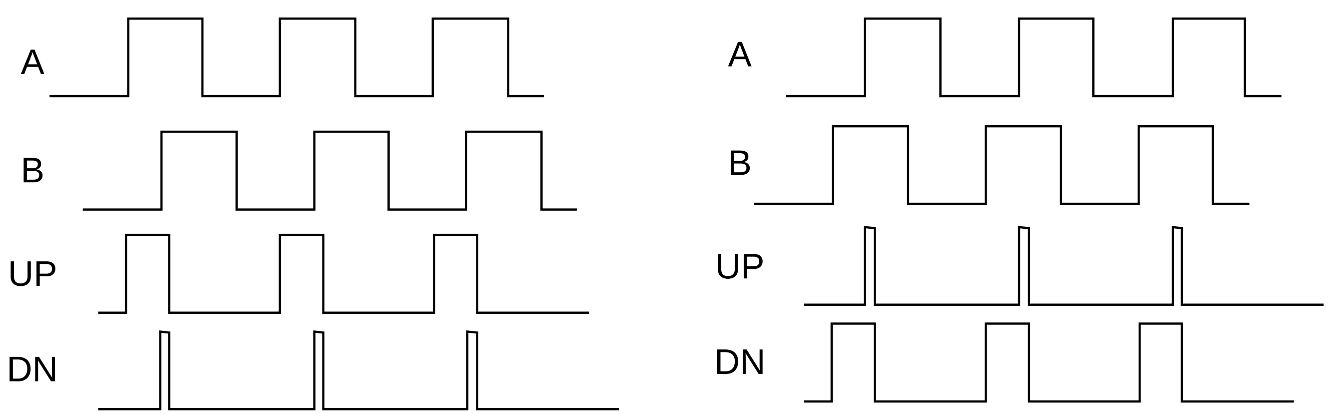
Phase-Frequency Detector



(a) schematic

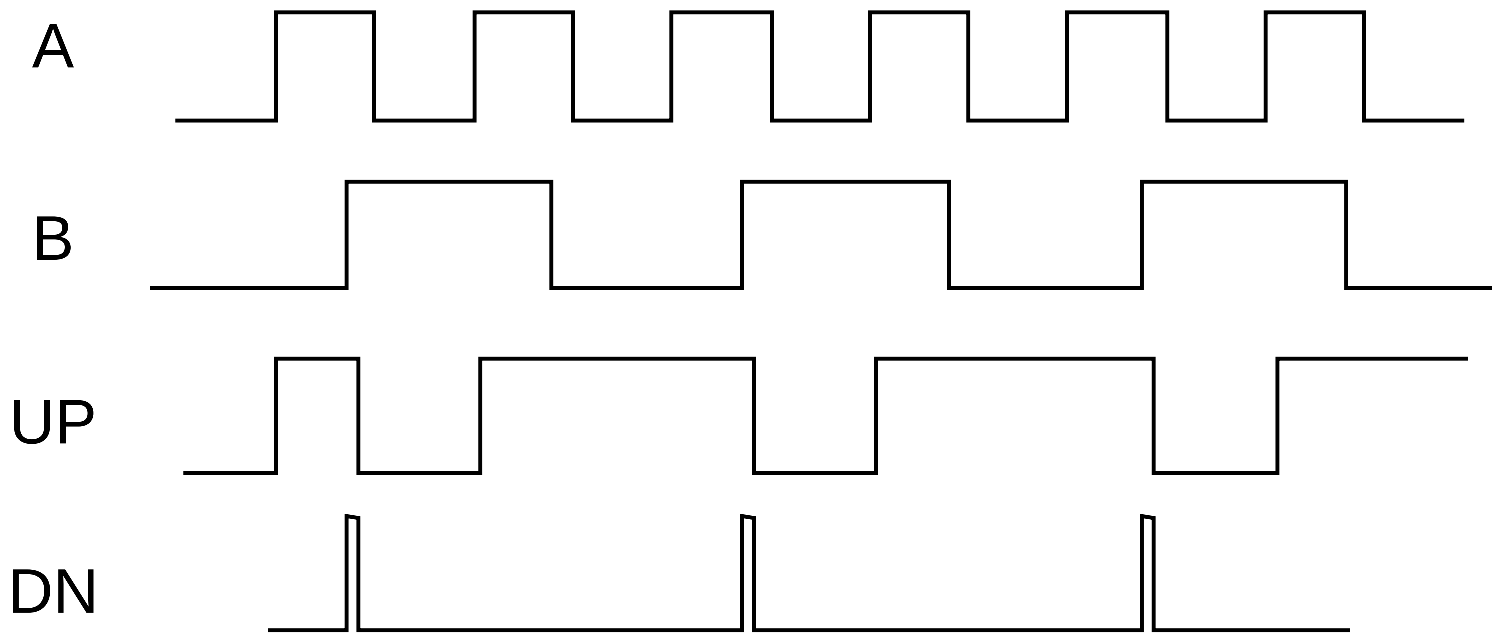


(b) state transition diagram

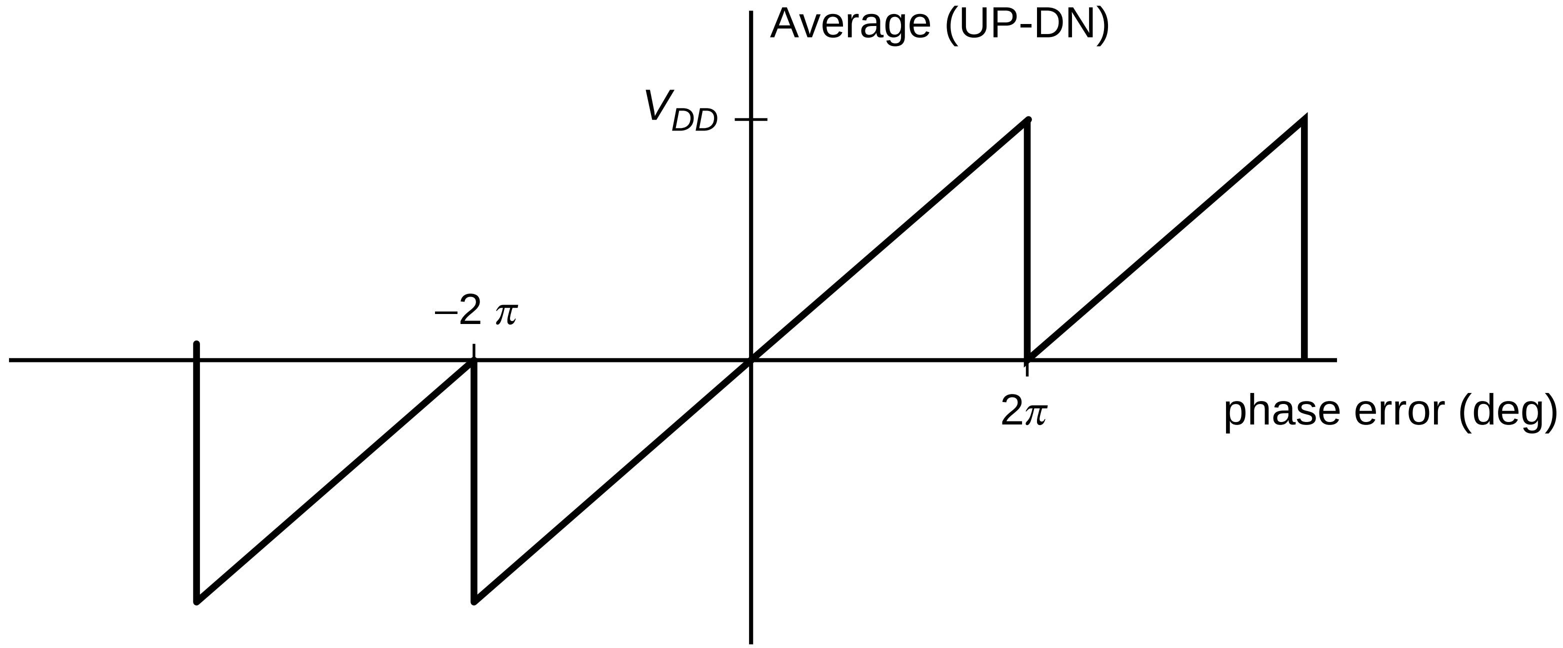


(c) Timing waveforms

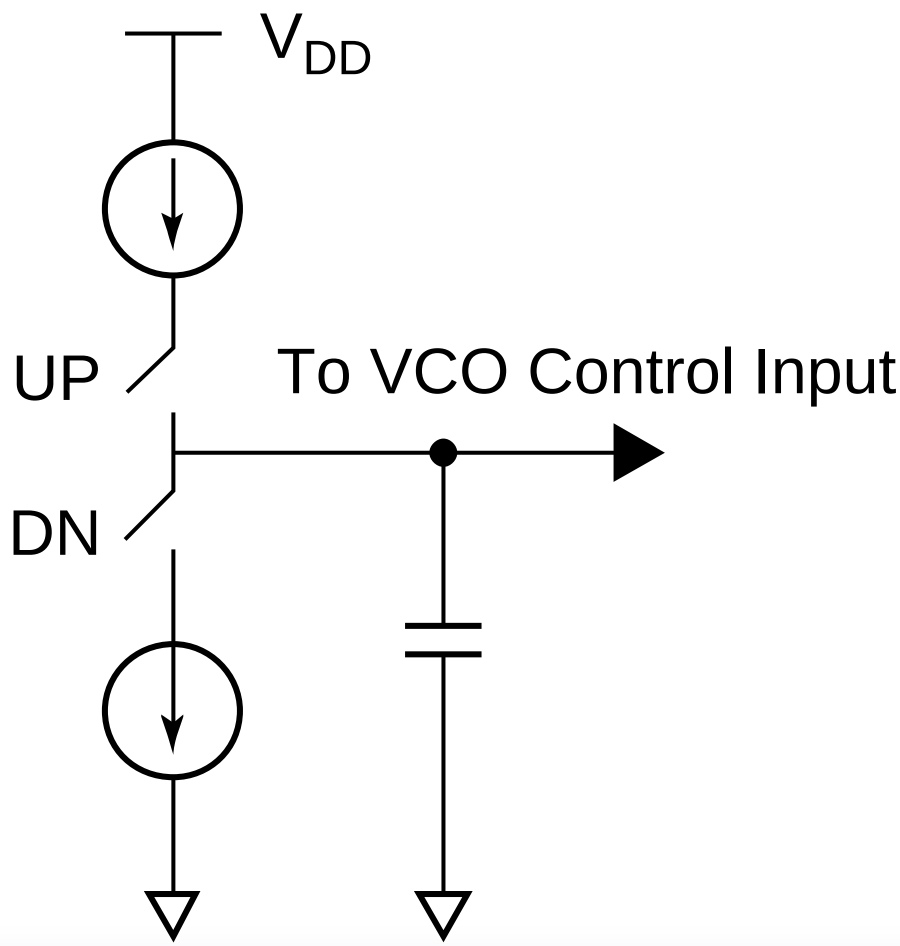
PFD Response to Frequency



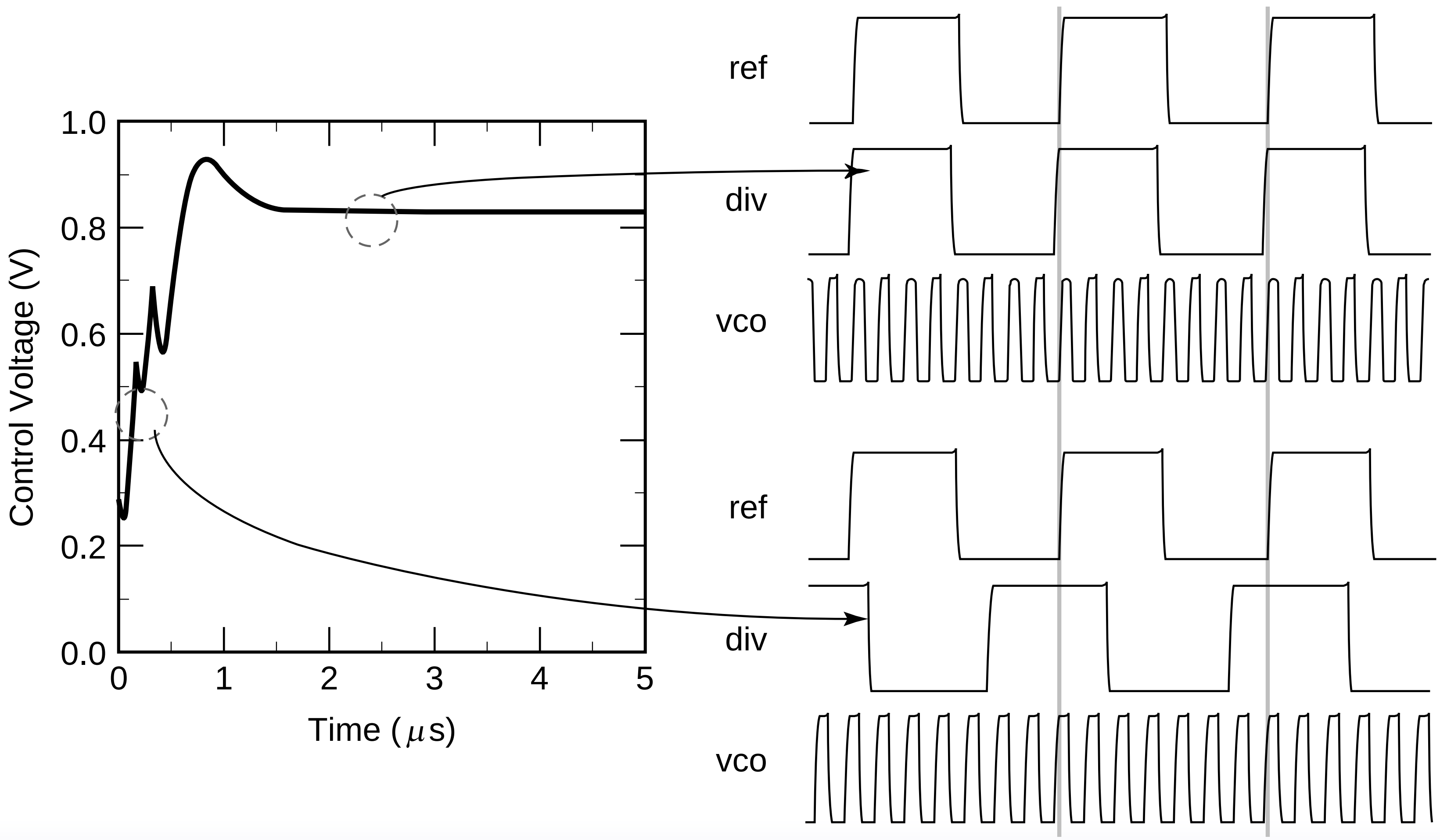
PFD Phase Transfer Characteristic



Charge Pump



PLL Simulation

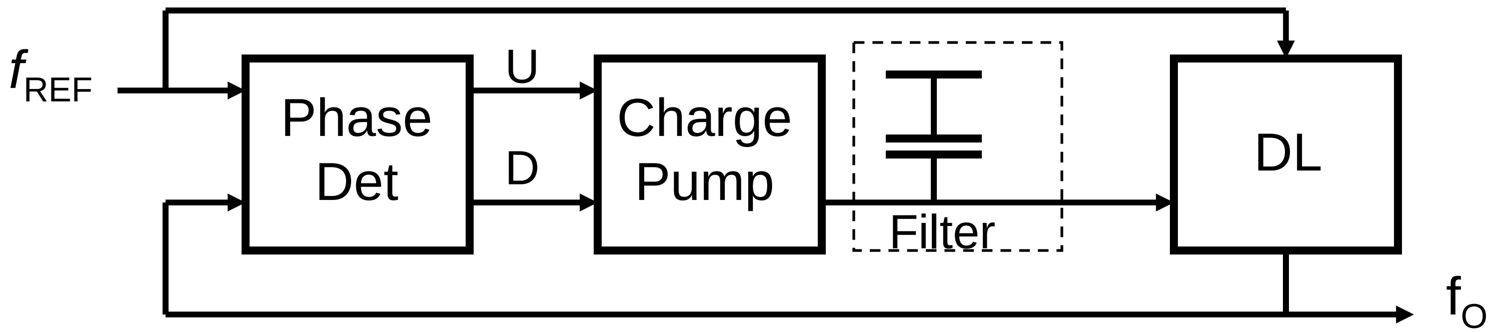


Clock Generation using DLLs

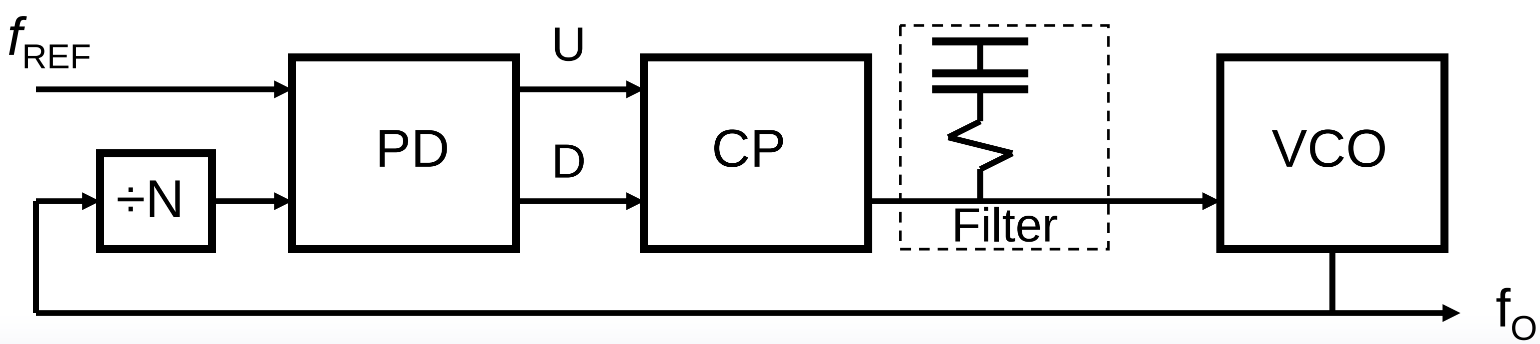
Main idea is to delay the output clock so that it lines up perfectly with the reference….

Delay-Locked Loop (Delay Line Based)

Consists of a cascade of delay elements

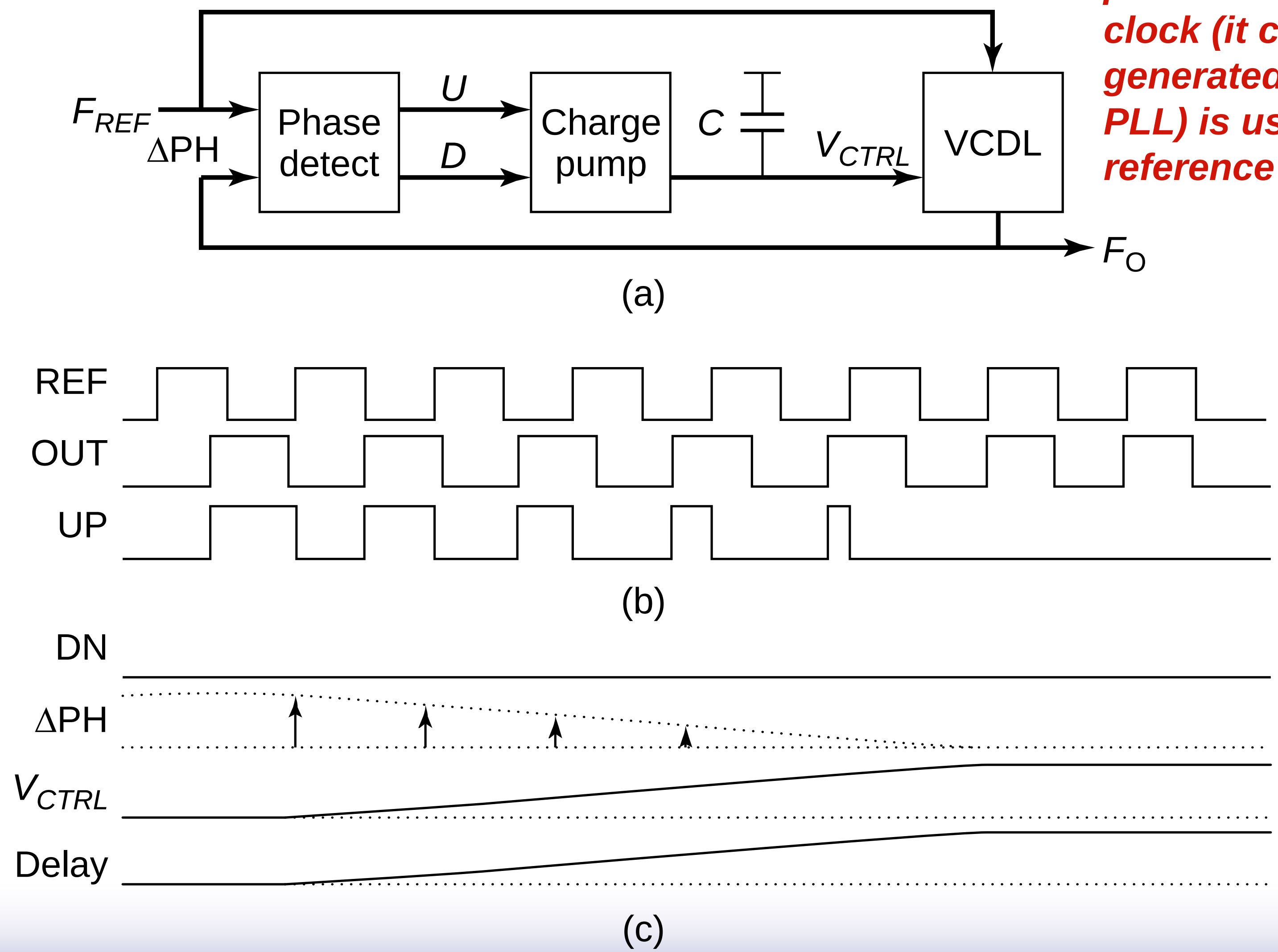


Phase-Locked Loop (VCO-Based)

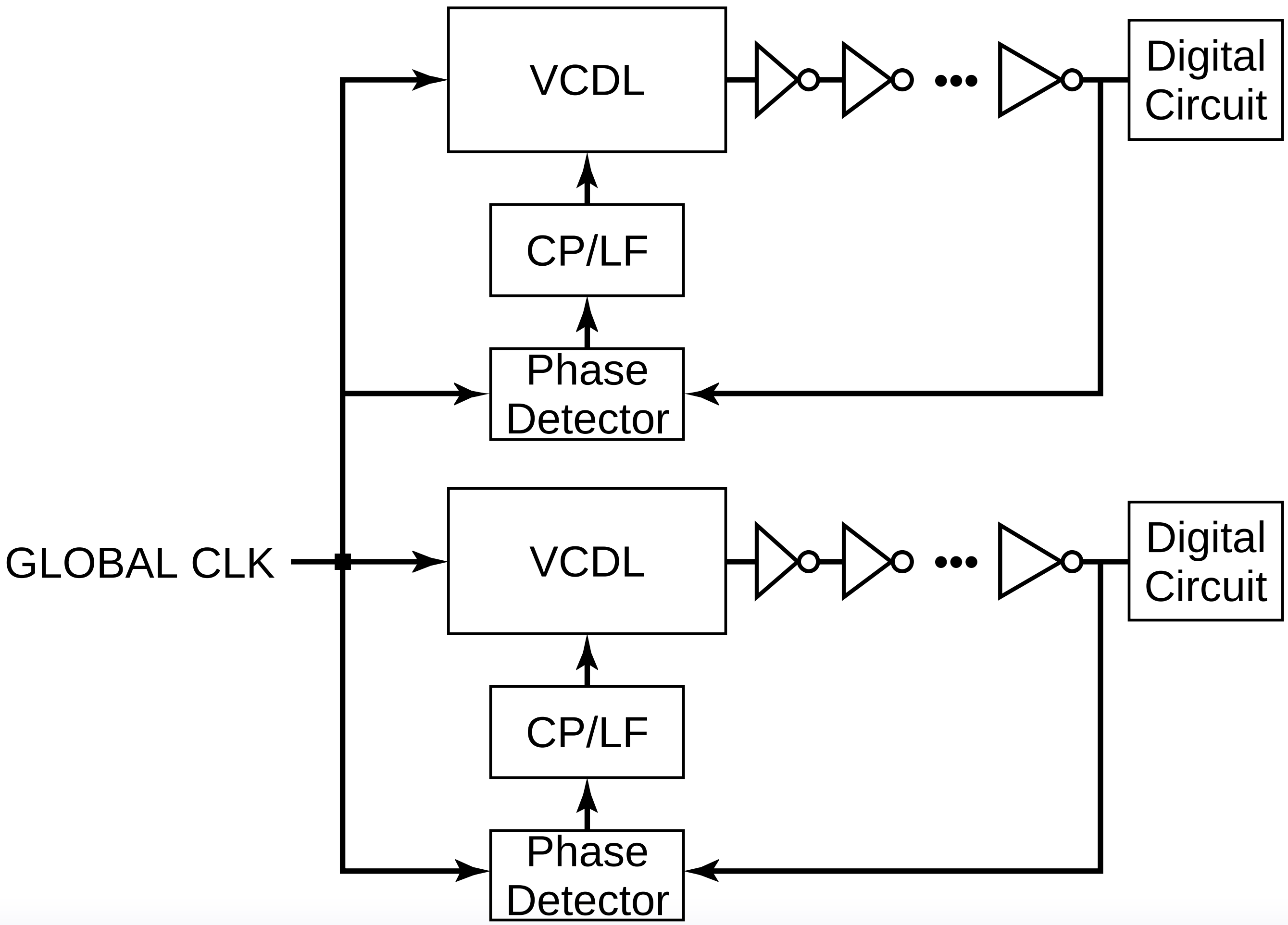


Delay Locked Loop

Does not alter the freq. of input reference…only adjusts the phase…a local clock (it can be generated by a PLL) is used as a reference for DLL

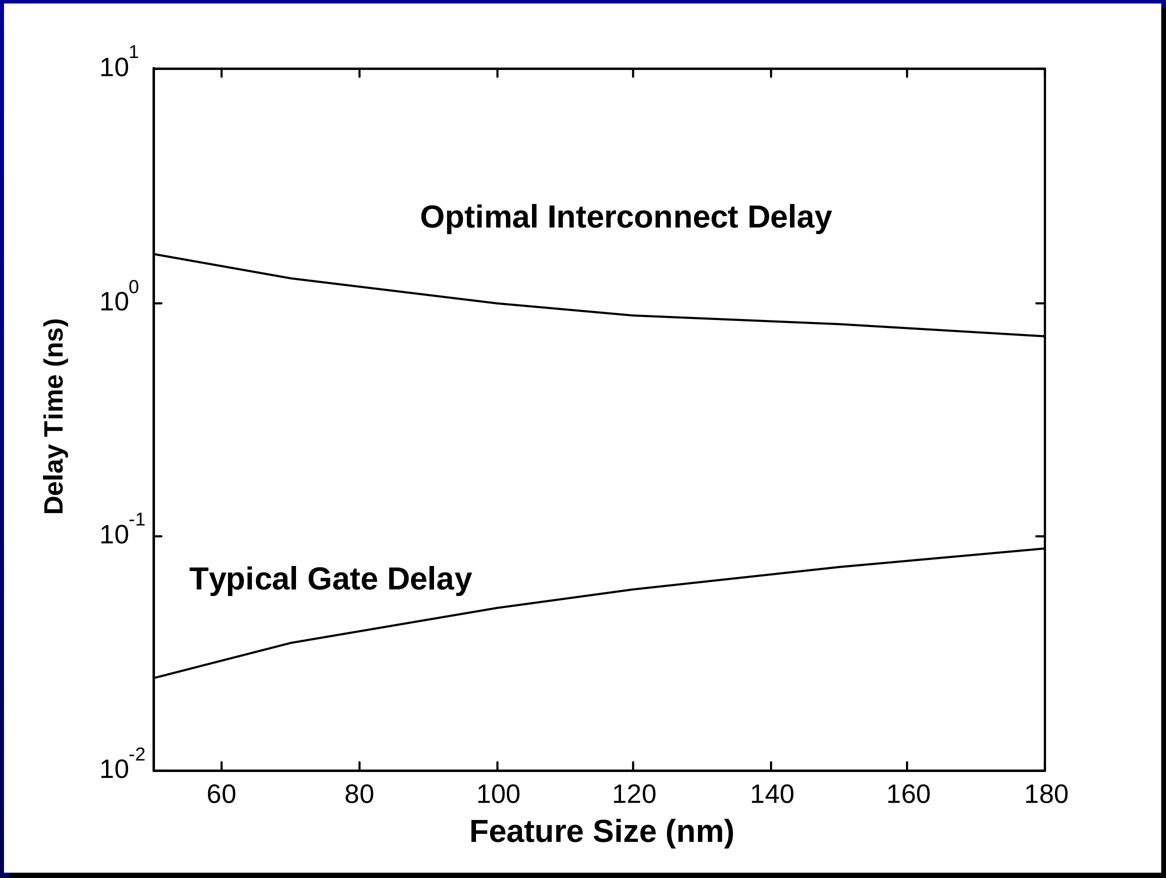


DLL-Based Clock Distribution



3-D ICs: Extending Moore's Law in the Z-Dimension, and more….

Interconnect Delay is Increasing (ITRS ’99)



K.Banerjee et al., Proc. IEEE, 2001.

If we can reduce both R and C, we can reduce wire delay…..

Will better materials like copper and low-k dielectrics solve the interconnect problem?

Cu has lower resistivity than Al, and is more robust (reliable) than Al…….

Changing Interconnect Materials

- Replace Al wires by Cu wires
- Resistivity of Al = 2.65 $\mu\Omega$-cm

  @ Room Temp. (20-25 ^{0}C)
- Resistivity of Cu = 1.67 $\mu\Omega$-cm

  @ Room Temp. (20-25 ^{0}C)
- Reduction in R is not even a factor of 2…..

Low-k Dielectrics

IBM Says Process Can Make Chips More Powerful

By Bruce Meyerson
ASSOCIATED PRESS

NEW YORK — IBM Corp. has developed a method for insulating the tiny circuits on a computer chip so they can be placed even closer together, making room for more computing power on each semiconductor.

The new process, which coats the circuits with a chemical polymer instead of silicon dioxide, can either improve a chip's processing speed by as much as 30 percent or halve the amount of power it uses, IBM said yesterday.

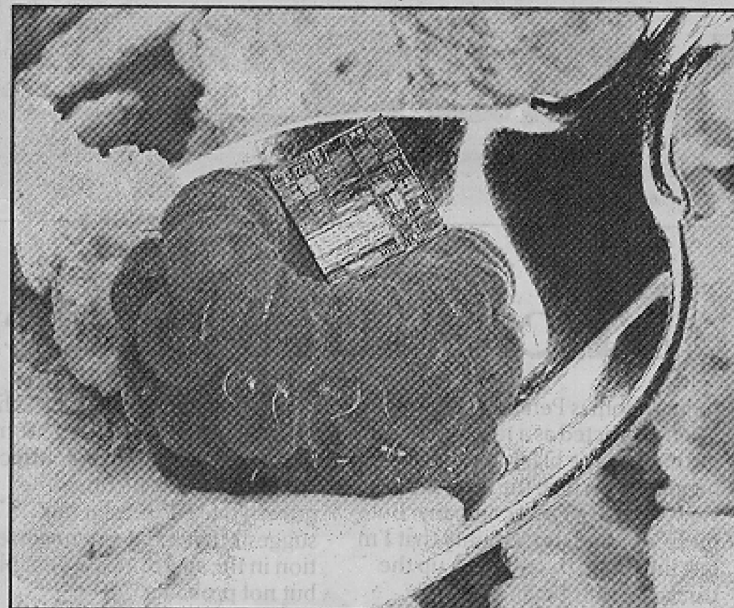
The insulation cuts down on magnetic interference, or "crosstalk," between the electrical pulses that travel along the millions of copper circuits that a chip uses to crunch data.

Because the electrical pulses are better shielded from the magnetic fields generated by neighboring pulses, the distance between circuits can be reduced by more than a quarter to 0.13 microns — a measurement 600 times thinner than a human hair.

Thanks to the space savings, chipmakers can double the number of transistors they cram onto a piece of silicon to about 400 million, said Bijan Davari, a vice president of IBM's semiconductor research and development center in East Fishkill, N.Y.

Chips made with the new insulation are expected to be available next year, IBM said.

The first application will be to produce powerful microprocessors for major business systems like those used to run Web sites and communications networks.



Associated Press

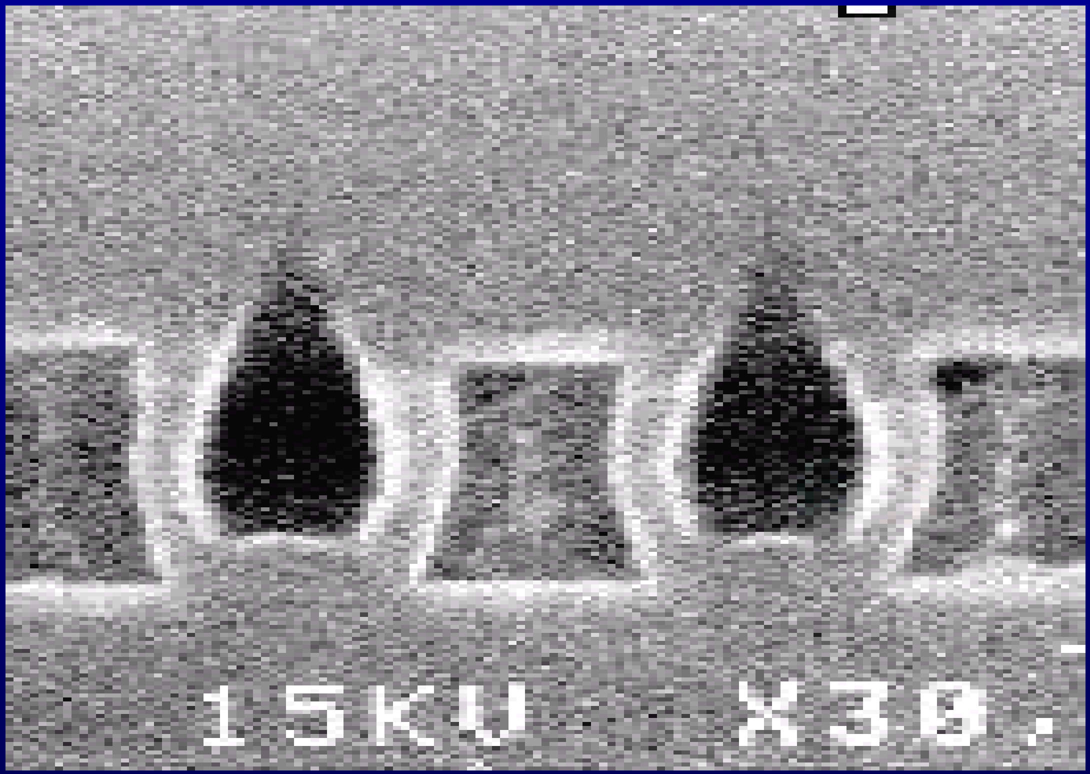
IBM said its new process for insulating circuits on small computer chips (such as this planted in a spoon of fruit and cereal for size comparion) should increase computing speed and performance by as much as 30 percent.

Old dielectric SiO_2 K = 4

New dielectric Silk K = 2.5

The difference is not even a factor of 2!

Limit of Low-k Dielectrics (Air: K =1)

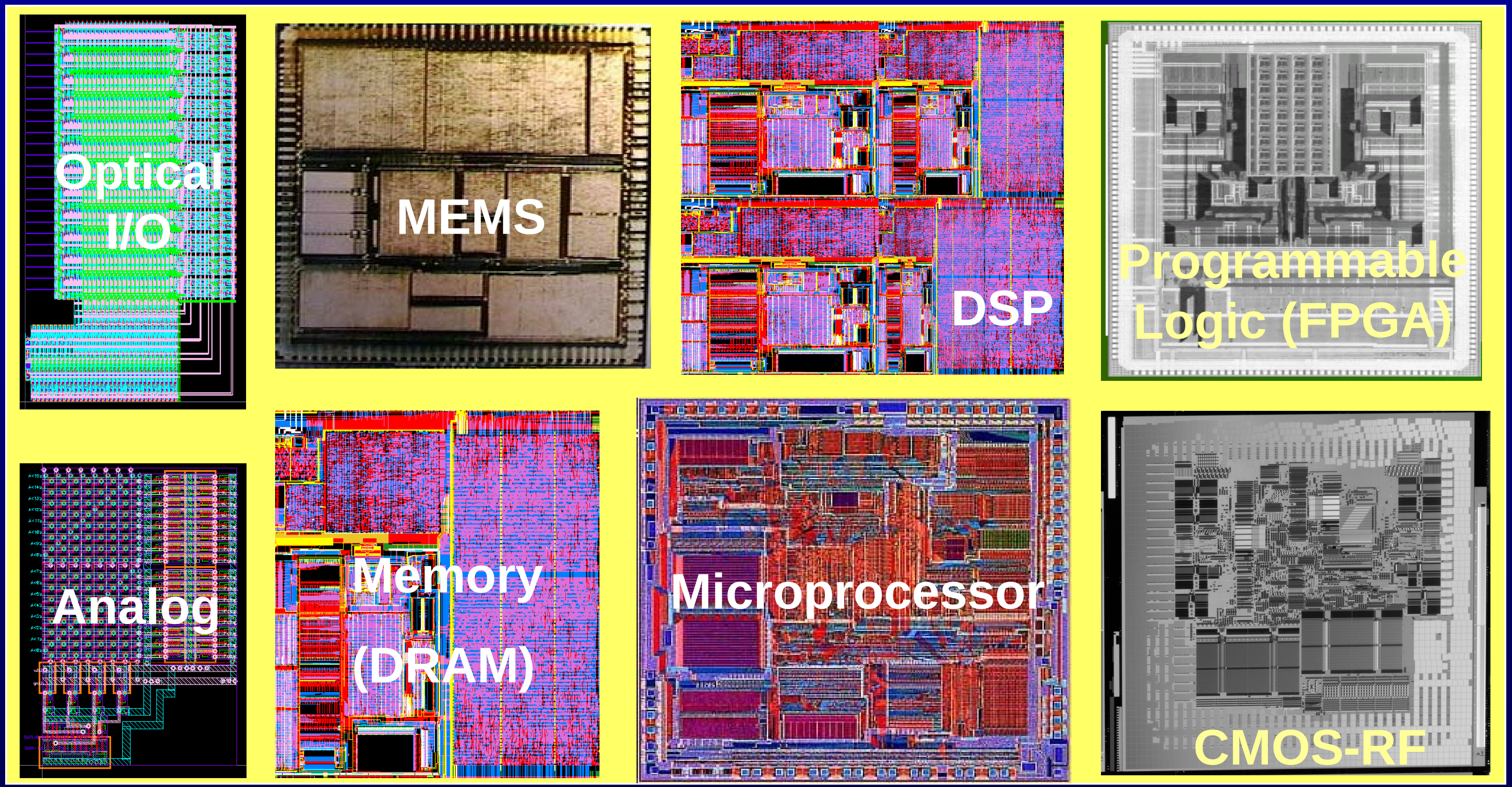


Air-Gap Interconnect Structure

Effects on Design Process

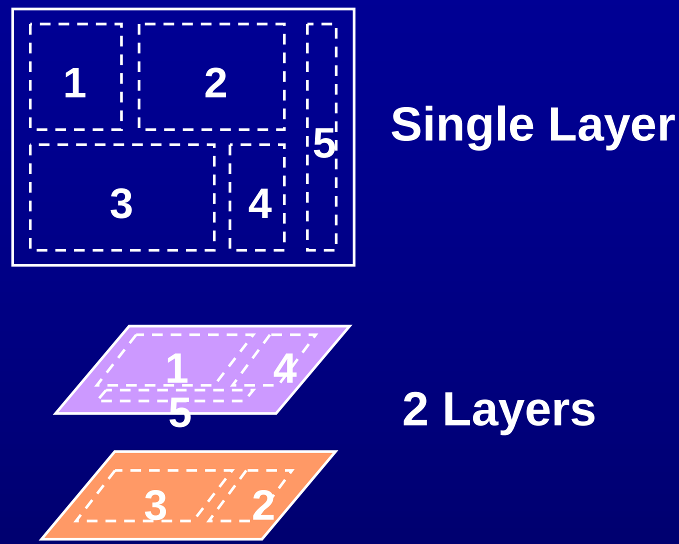
- Increasing wire delay causes timing closure problem
- Prevents CAD methodologies to adopt higher levels of abstraction to simplify and accelerate the design process

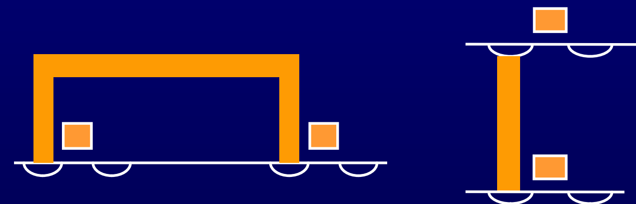
Integrated SoC to Sense, Process, and Collaborate



Difficult in Planar IC Technology

Novel Design Architectures Needed!





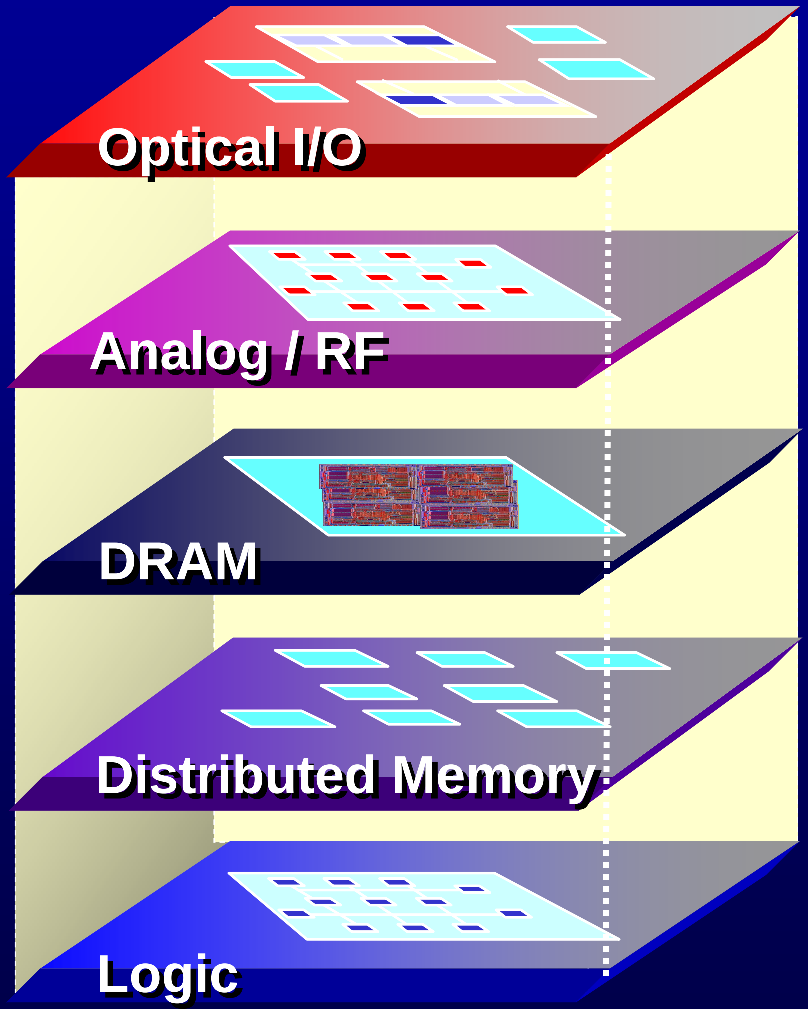
Replace horizontal by vertical interconnect

3-D ICs utilize the vertical dimension

3-D ICs : Multiple Active Si Layers

(DAC 2000)

- **Advantages**
  - Reduce Interconnect Length by Vertically Stacking Multiple Si Layers
  - Improve Chip Performance
  - Reduce Chip Area
  - Heterogeneous integration possible, e.g., memory, digital, analog, optical, etc.



Performance Analysis Strategy

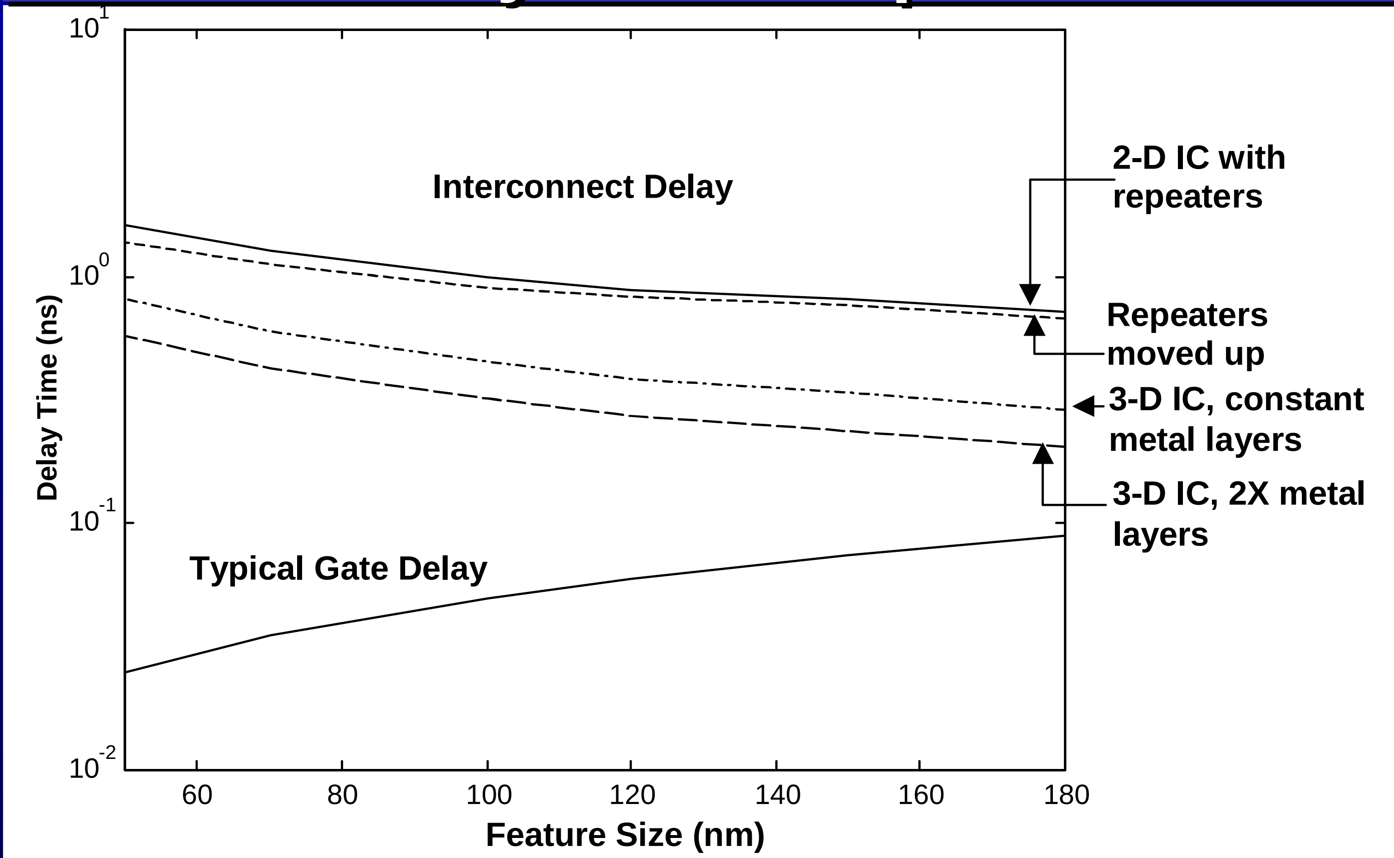
- **Estimate Chip Area**
- **Estimate Interconnect Delay**

Chip Area Determined from Wiring Requirement

(Used 50 nm ITRS Data)

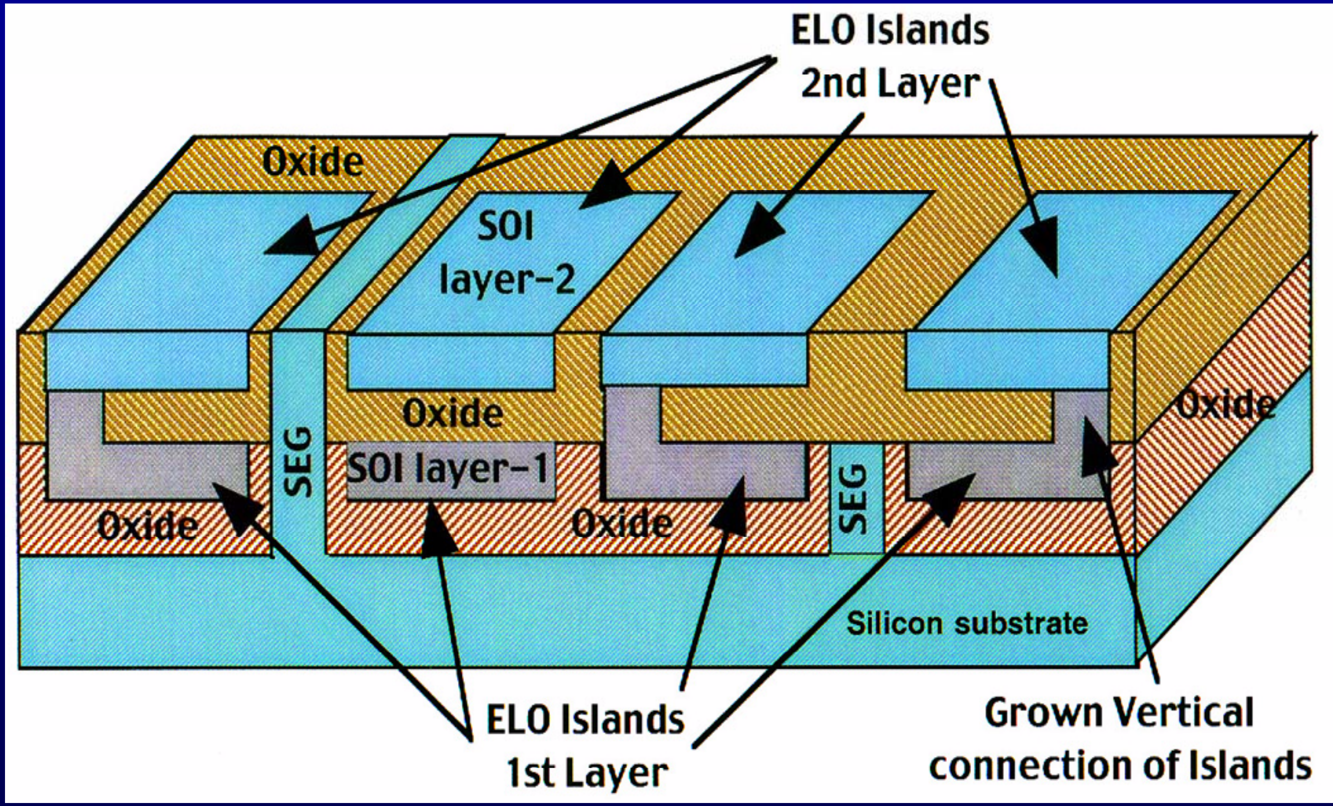
Performance Summary

2-Layer 3-D Chip

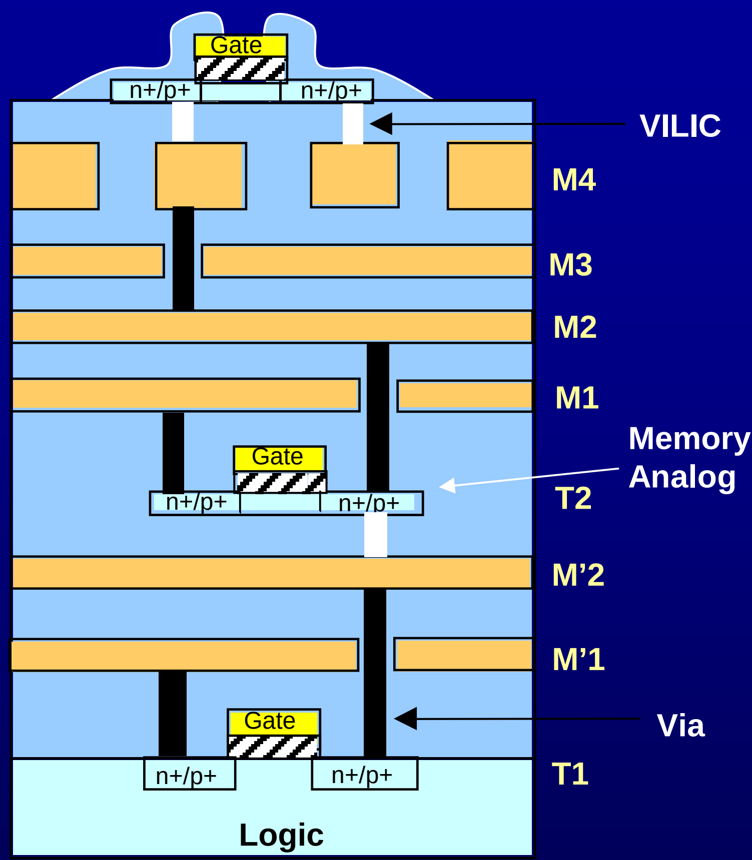


3-D Technologies

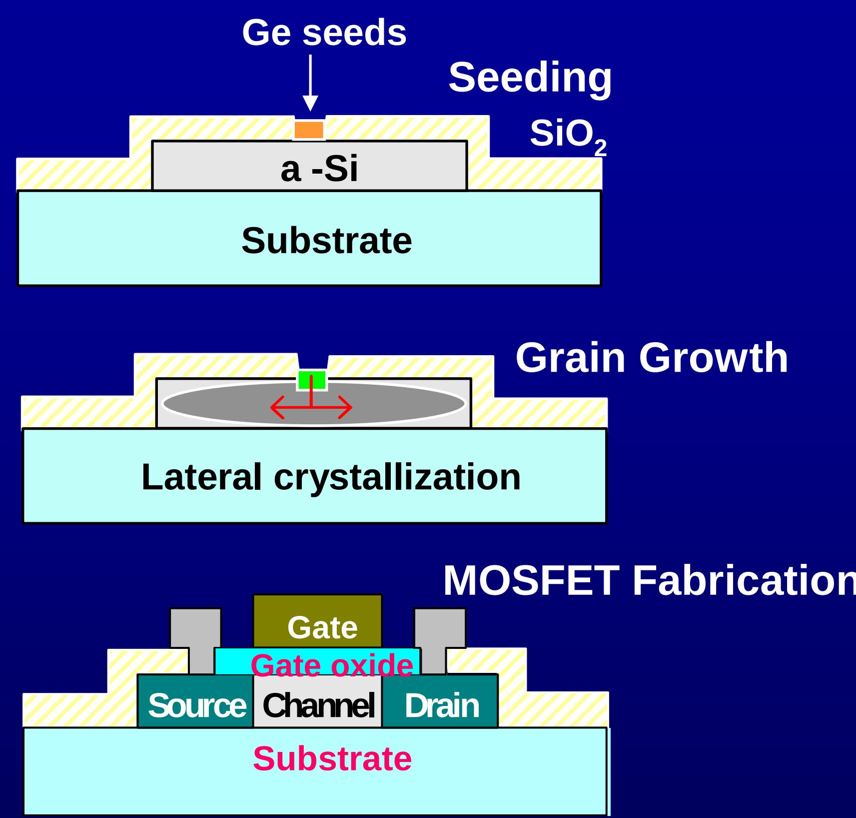
Epitaxial Lateral Overgrowth



3-D Technologies

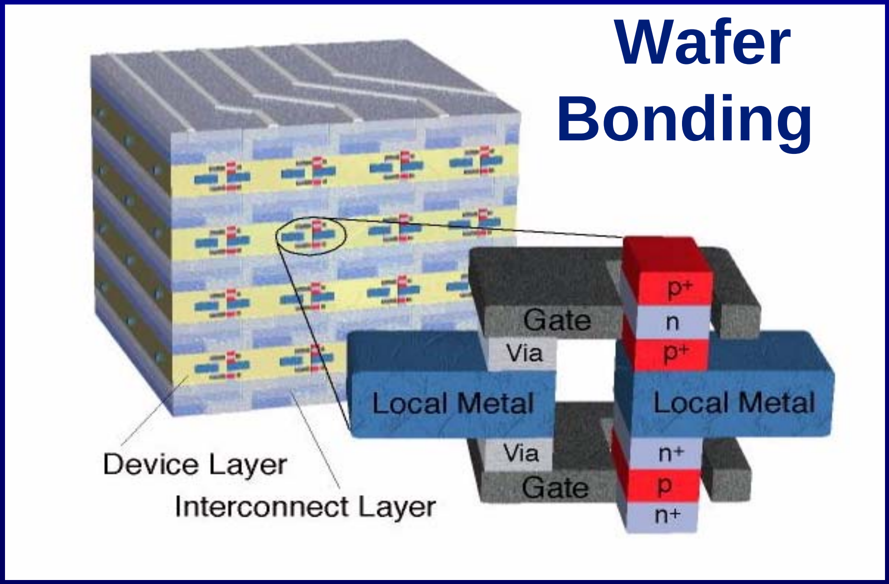


Solid Phase Crystallization of α-Si

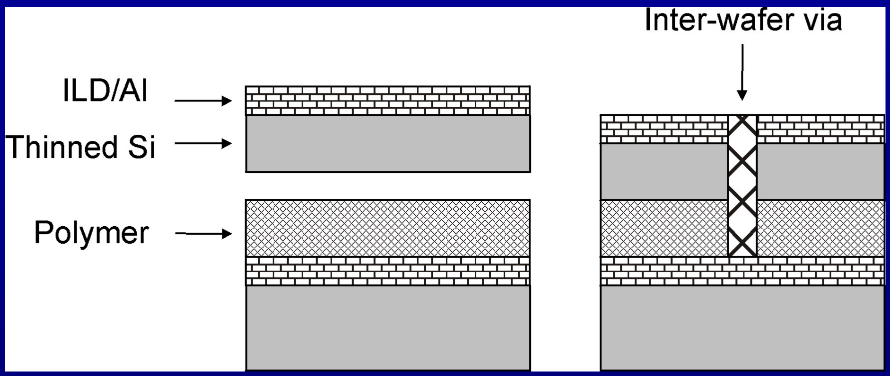


- Locally induce nucleation
- Grow laterally, inhibiting additional nucleation
- Build MOSFET in a single grain with SOI like performance

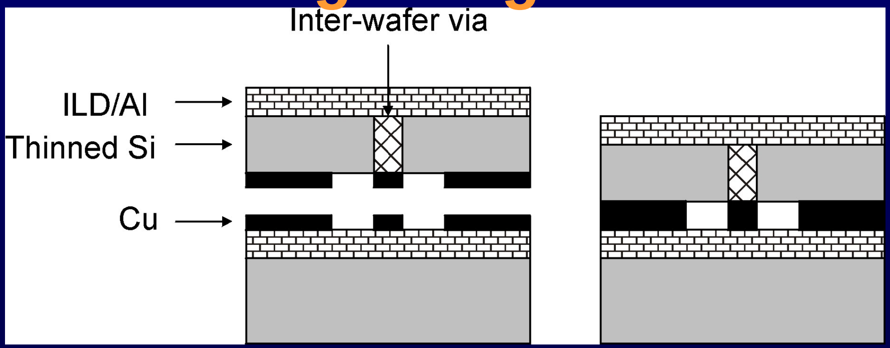
3-D Technologies



Bonding using Glue Layer



Thermocompression Bonding using Cu Pads



3D ICs: Implications for Circuit Design

- **Critical Path Layout:** By vertical stacking, the distance between logic blocks on the critical path can be reduced to improve circuit performance.
- **Repeaters:** Some chip area can be saved by placing repeaters (~ 10,000 for high performance circuits) on the higher active layers.

3D ICs: Implications for Circuit Design

- **Microprocessor Design: on-chip caches on the second active layer will reduce distance from the logic and computational blocks.**

"3-D Shared Memory using Wafer Stacking"

K.W. Lee et al., (Tohoku Univ. Japan) IEDM 2000

- ***3-D integration technology --wafer stacking***

- ***Parallel processor system with three memory layers --multiport memory, overcomes bus bottleneck***

3D ICs: Implications for Circuit Design

- Integration of Disparate Technologies Easier
- RF and Mixed Signal ICs: Substrate isolation between the digital and RF/analog components can be improved by dividing them among separate active layers - ideal for system on a chip design.
- Optical Devices and I/Os can be integrated on the top layer

3D ICs: Implications for Circuit Design

- ISSCC 2001-- Session on 3-D Technologies...

- Neuromorphic Vision Chip: Tohoku Univ.

  Achieved an image processing and pattern recognition system with parts of functions of the retina and visual cortex using Si

- 3-D Systems-on-a-Chip: MIT, Lincoln Labs

- 3D ring oscillators and back-illuminated 64X64 active pixel sensor arrays with fully parallel A/D conversion

- 3-D Assembly Technology: North Corp., Japan

Summary

- **Cu/low-k alone will not solve interconnect problems in complex VLSI designs**
- **New design architectures will be needed**
- **Performance modeling of 3-D ICs shows significant improvement over 2-D**
- **Wafer Bonding is a promising technique to implement 3-D ICs**
- **Thermal issues in 3-D ICs will require innovative packaging/cooling solutions….but not a show stopper**
- **Exciting applications are emerging…….**