ECE 225
High-Speed Digital IC Design

Lecture 18
Semiconductor Memory Design-II

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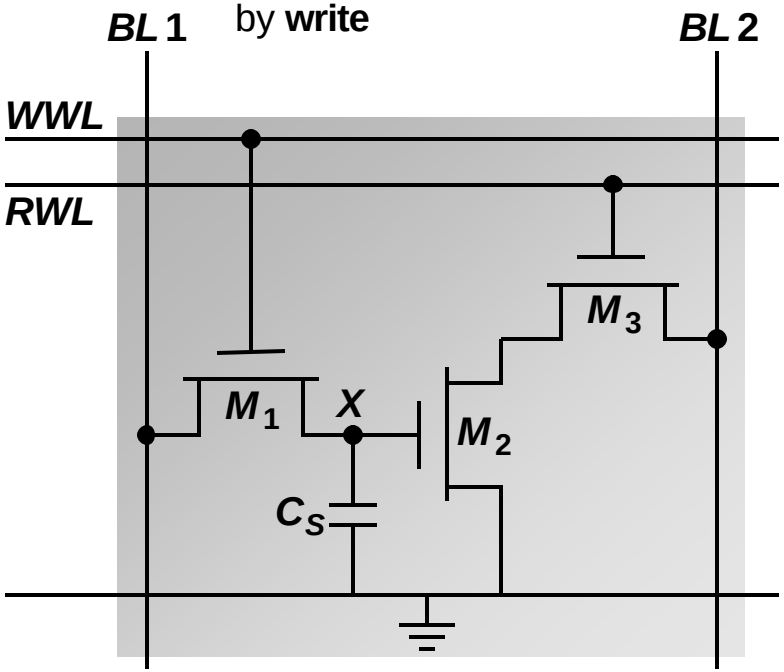
3-Transistor DRAM Cell (Early Days)

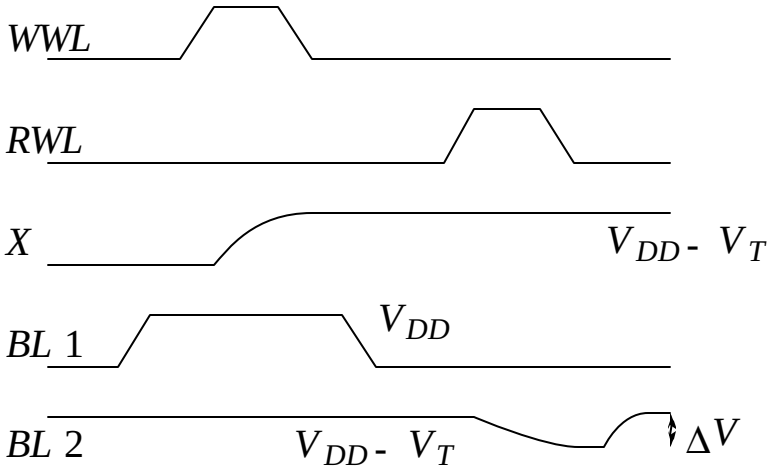
1 Kbit memory: Intel

Still used in some ASICs

Periodic refresh operation consists of **read** followed by **write**

Dynamic: since it involves charge storage on a capacitor





Cell is written by placing value on BL1 and asserting Write Word Line (WWL=1)

Data retained as charge stored on Cs once WWL=0

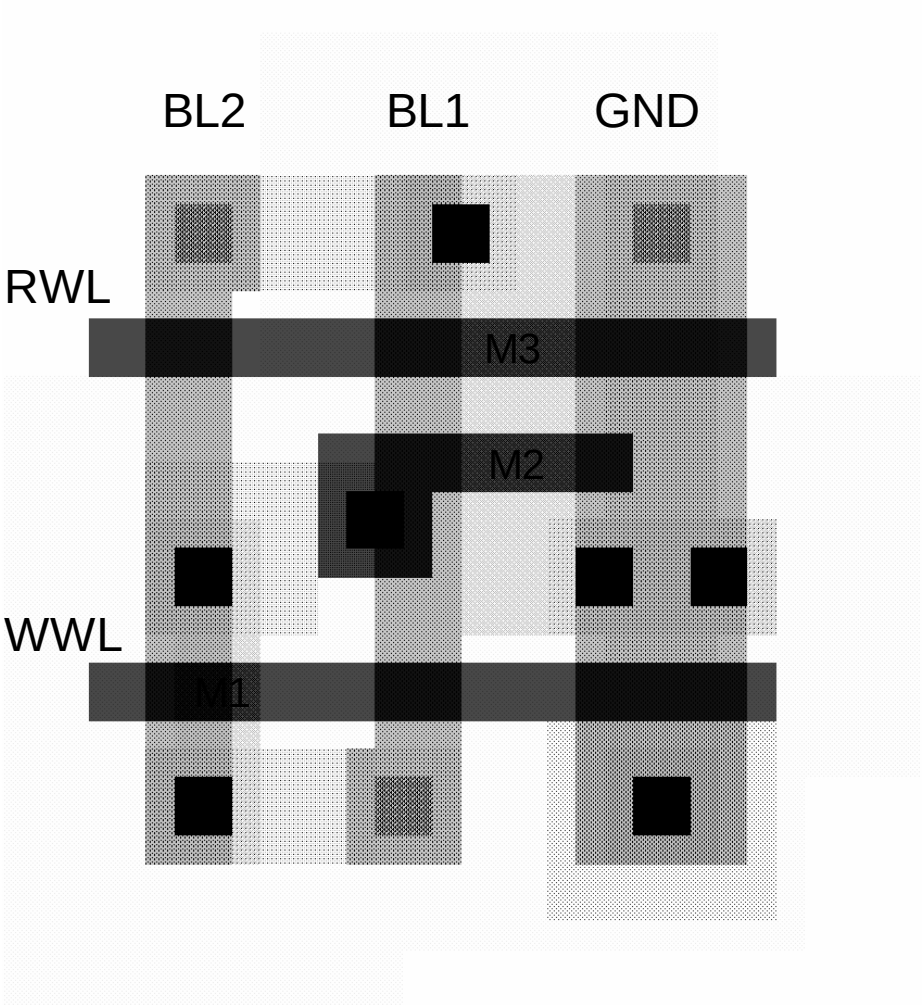
For reading the cell, RWL=1

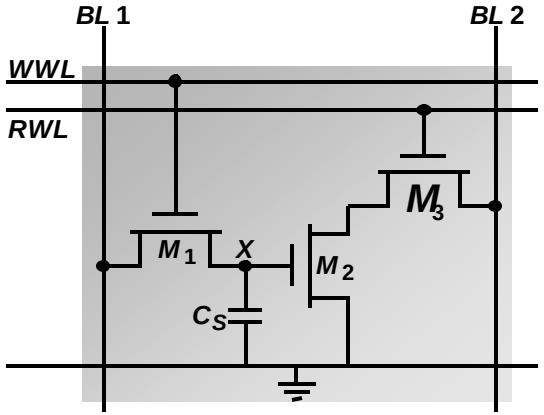
M2 can be on or off depending on stored value

BL2 is either clamped to Vdd or is precharged to either Vdd or Vdd-Vt

M2-M3 pulls BL2 low when X=1, otherwise BL2 remains high (cell is inverting: senses the inverse value of the stored signal)

3T-DRAM — Layout





Unlike SRAM, no constraint on device sizes

Read operation is non-destructive

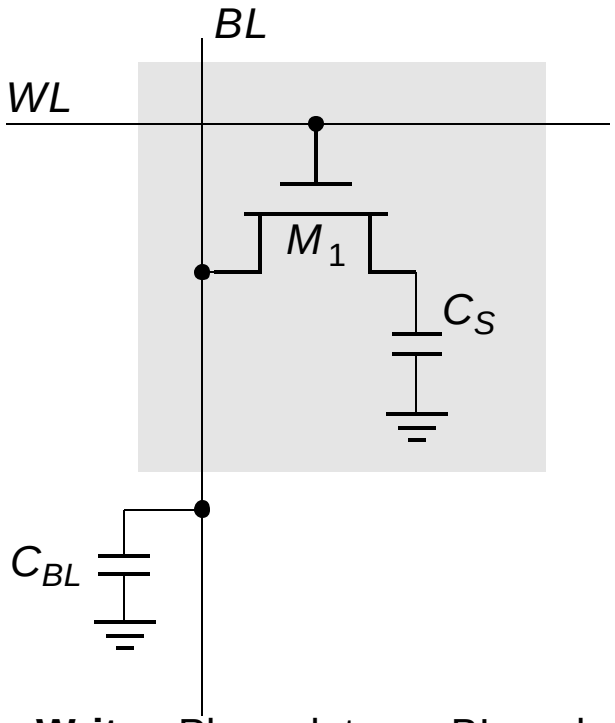
No special process steps needed

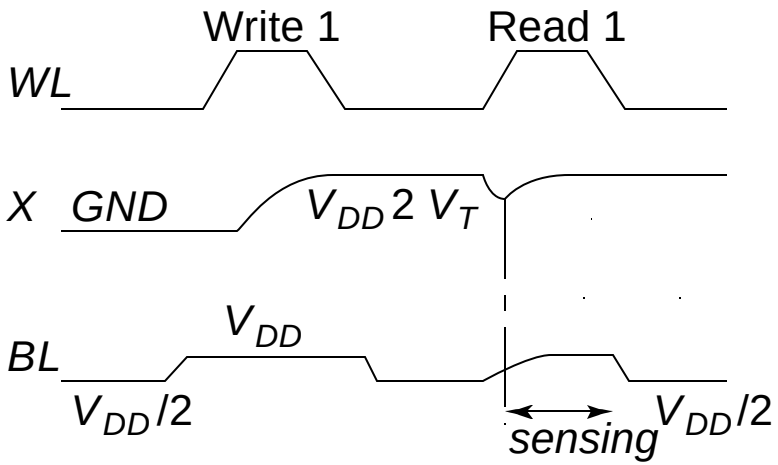
Value at node X = V_{WWL} - V_{tn}

This reduces the current through M2 during read operation and increases read access time: can use a higher value of V_{WWL} to avoid this

1-Transistor DRAM Cell

Most pervasive in commercial memory design





Write: Place data on BL and assert WL, depending on data value Cs is 1 or 0

Read: before read, precharge BL to V_{PRE}

After WL=1, charge redistribution takes places between bit line and storage capacitance resulting in a voltage change on BL

$$\Delta V = V_{BL} - V_{PRE} = V_{BIT} - V_{PRE} \frac{C_S}{C_S + C_{BL}}$$

Charge transfer ratio (1-10%)

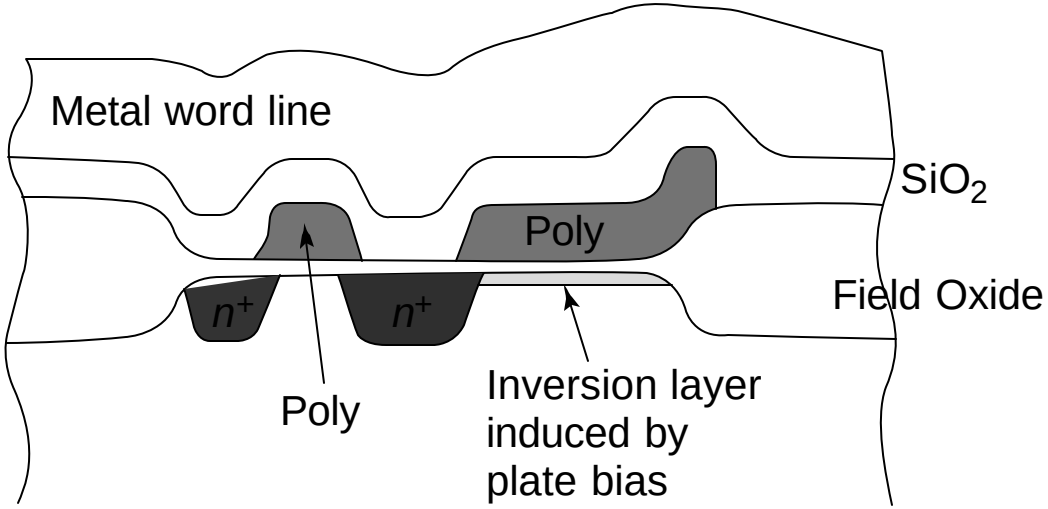
V_{BIT} is initial voltage on C_s. V_{BL} is final voltage on BL after charge redistribution.

Voltage swing is small since $C_s << C_{BL}$; typically around 250 mV.

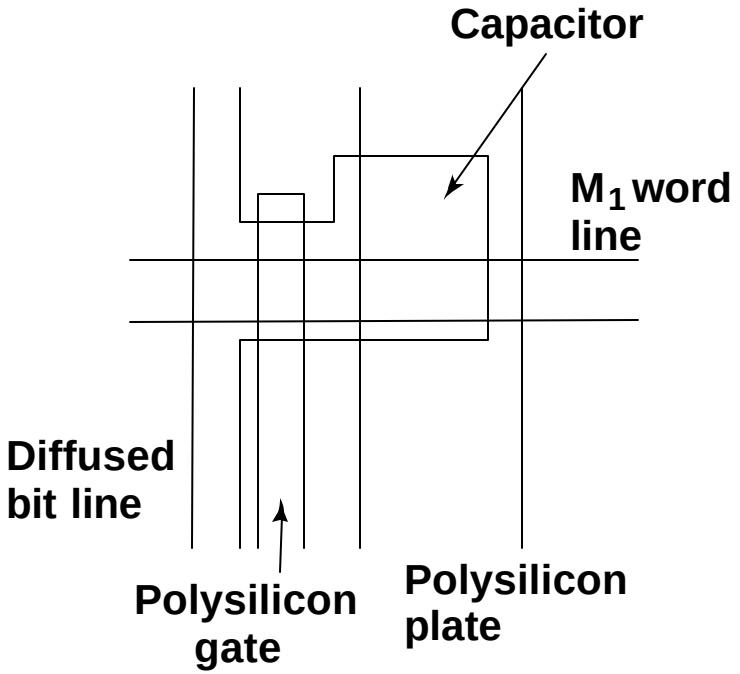
DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design.
- When writing a “1” into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than V_{DD}

1-T DRAM Cell



Cross-section

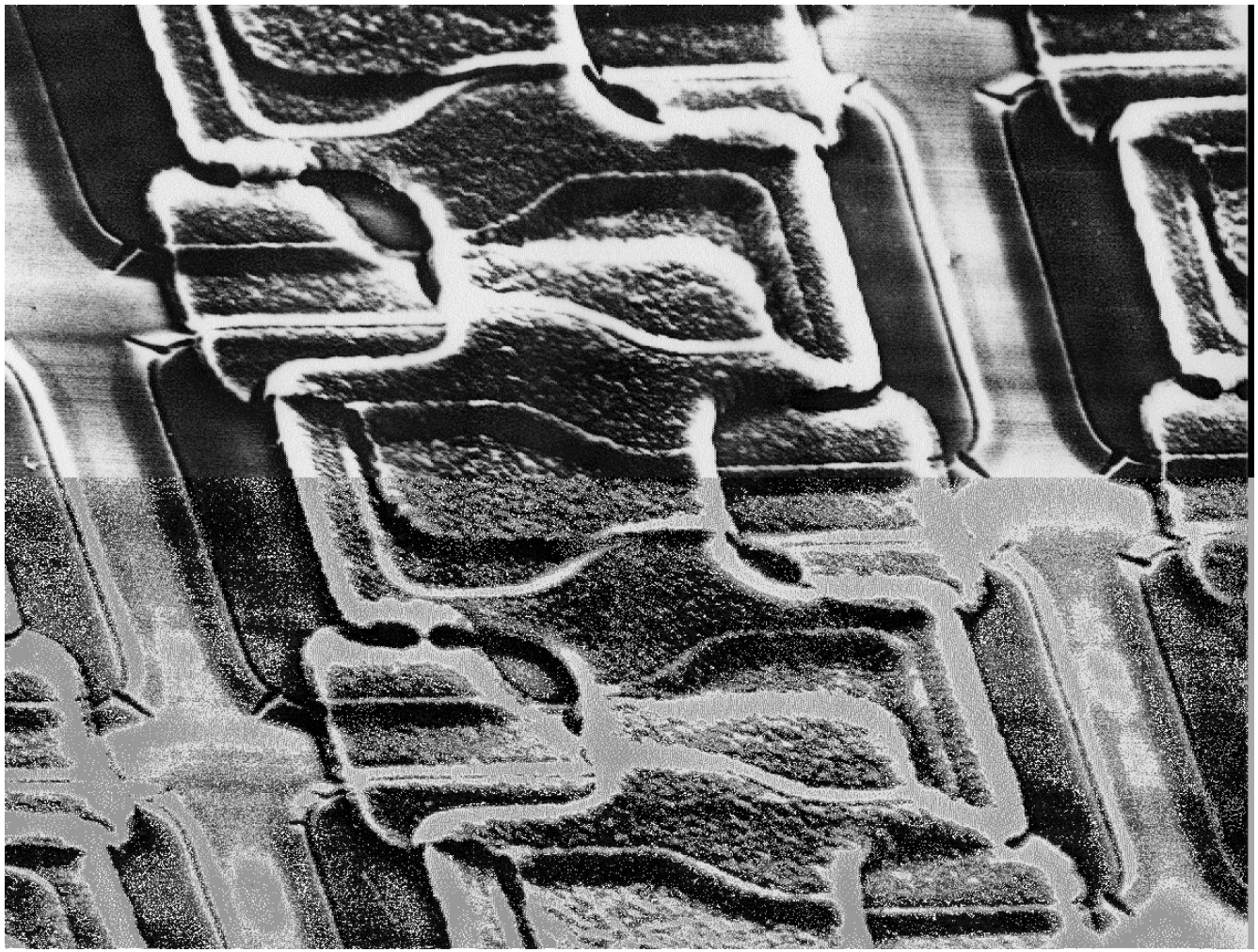


Layout

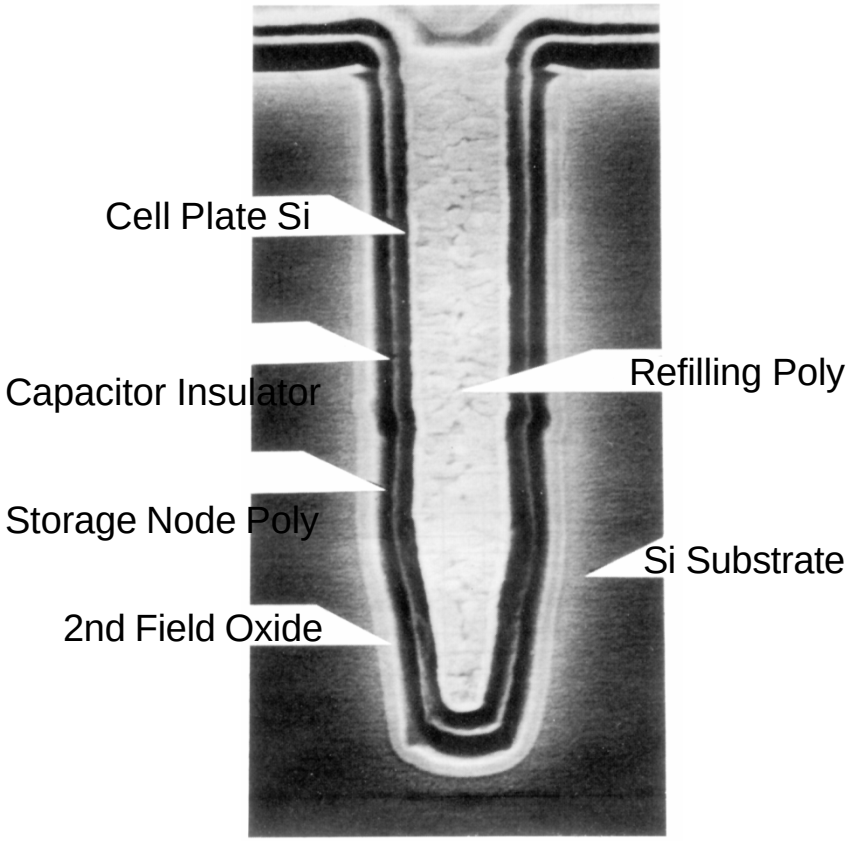
Uses Polysilicon-Diffusion Capacitance

Expensive in Area

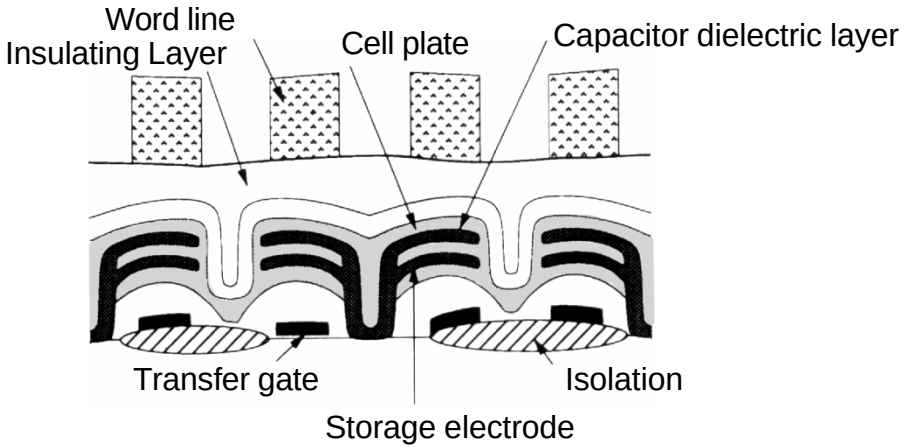
SEM of poly-diffusion capacitor 1T-DRAM

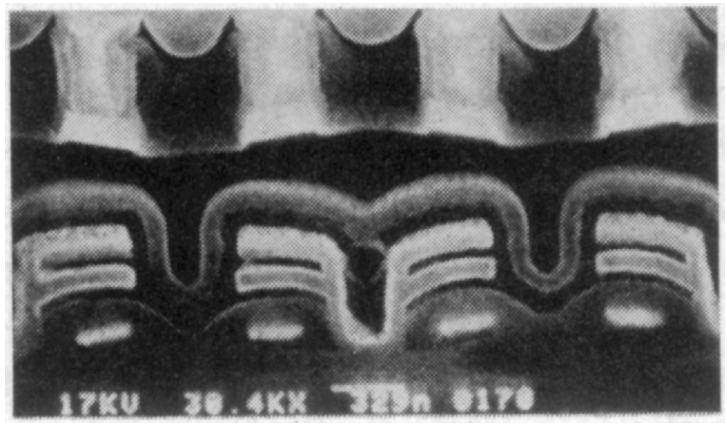


Advanced 1T DRAM Cells



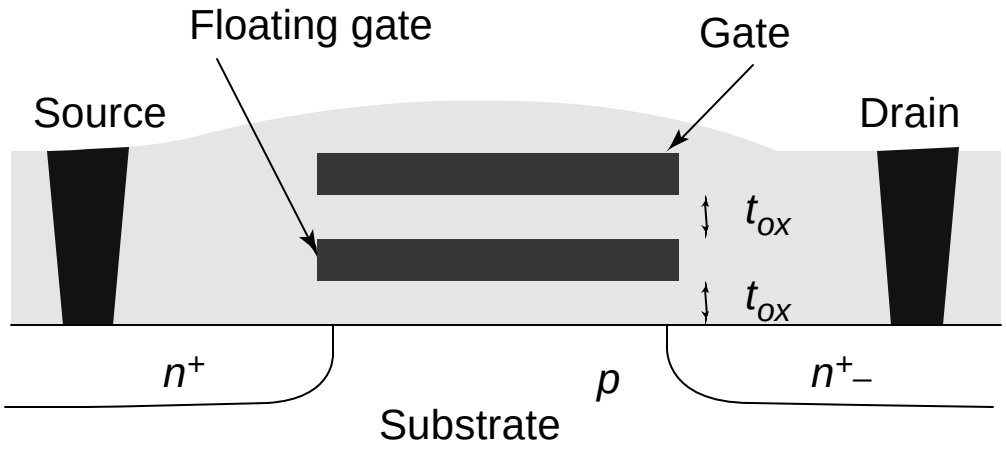
Trench Cell



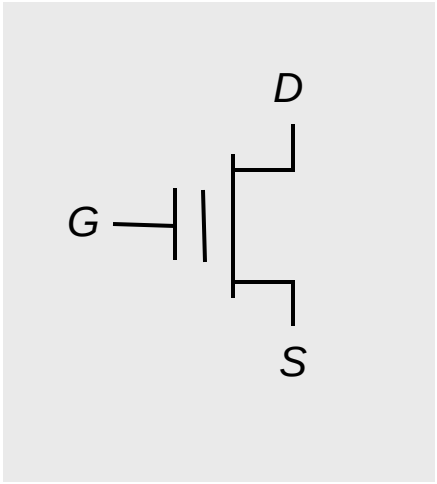


Stacked-capacitor Cell

Non-Volatile Memories
The Floating-gate transistor (FAMOS)

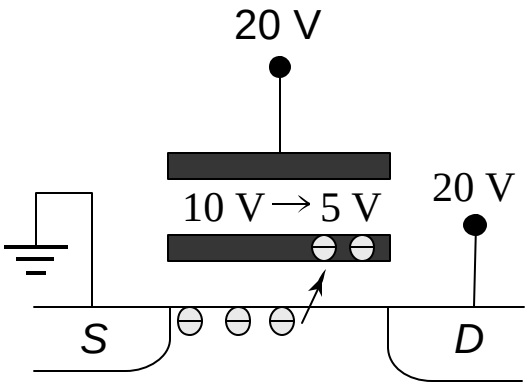


Device cross-section

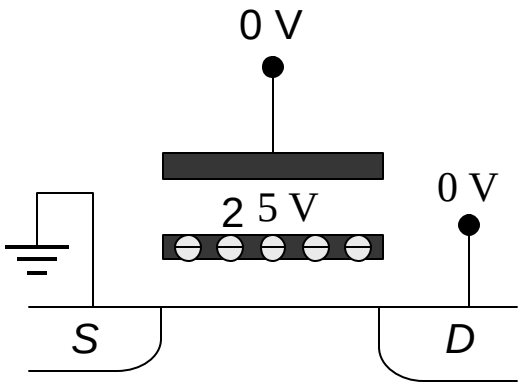


Schematic symbol

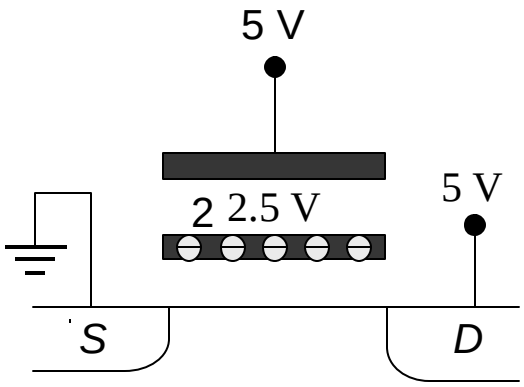
Floating-Gate Transistor Programming



Avalanche injection

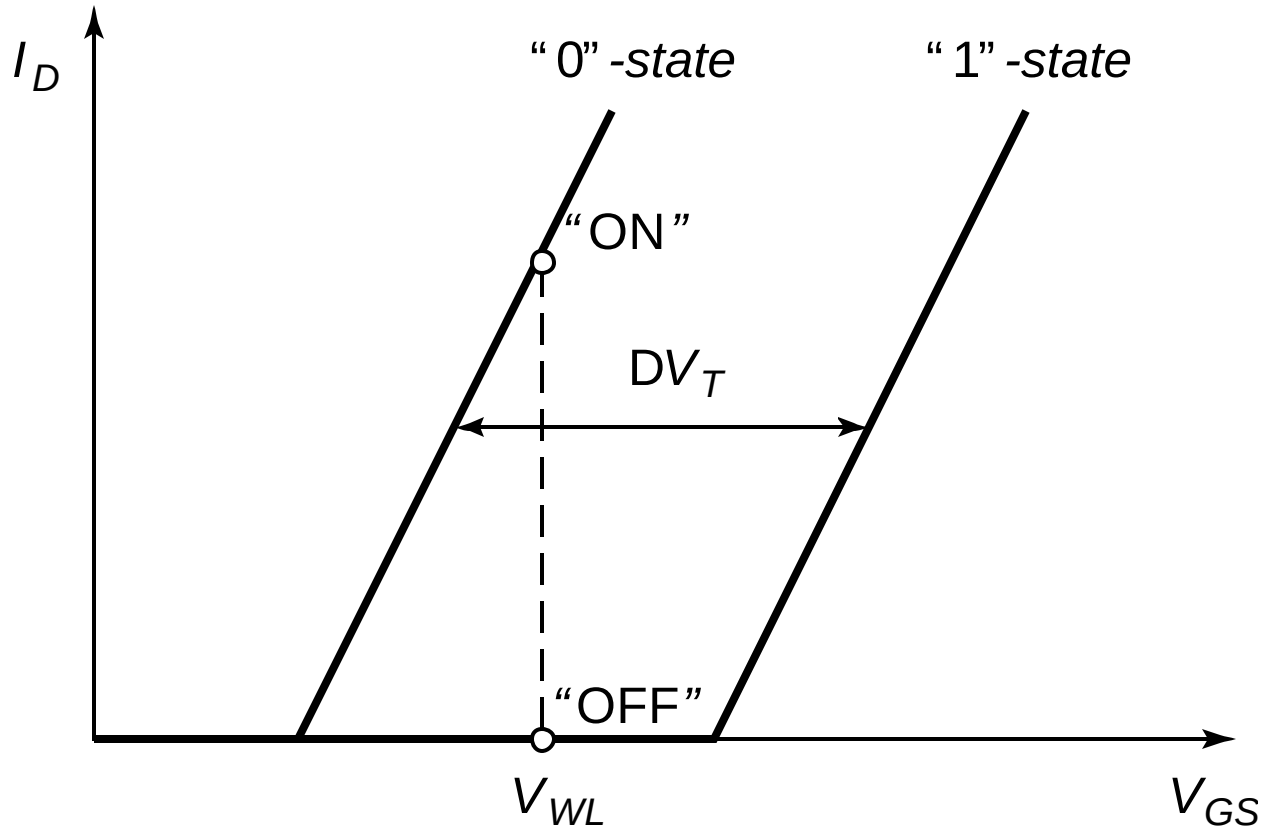


Removing programming voltage leaves charge trapped

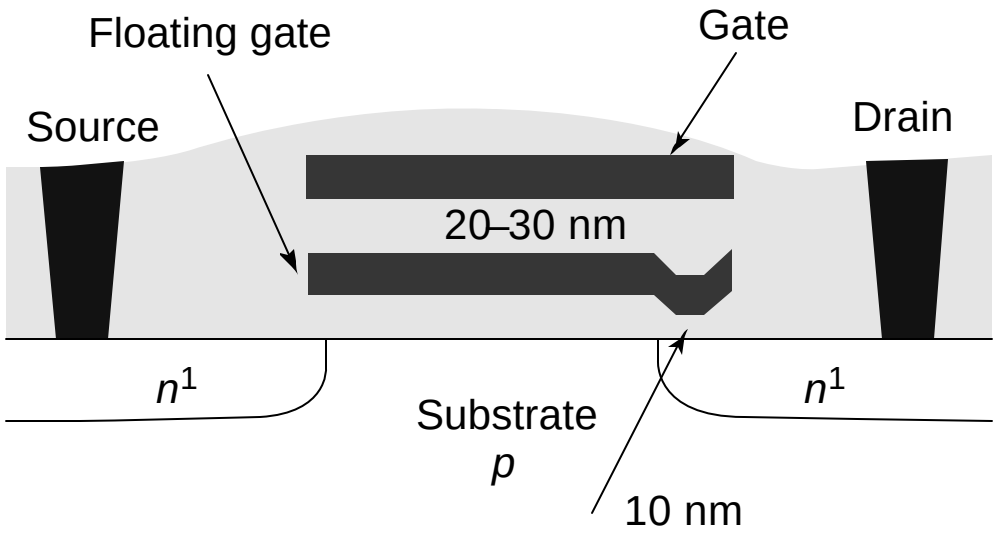


Programming results in higher V_T.

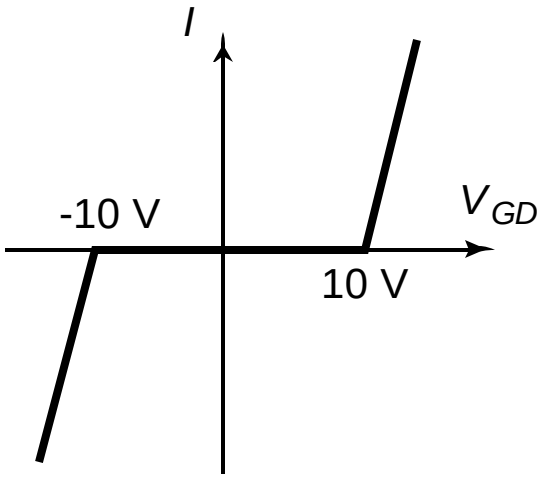
A "Programmable-Threshold" Transistor



FLOTOX EEPROM

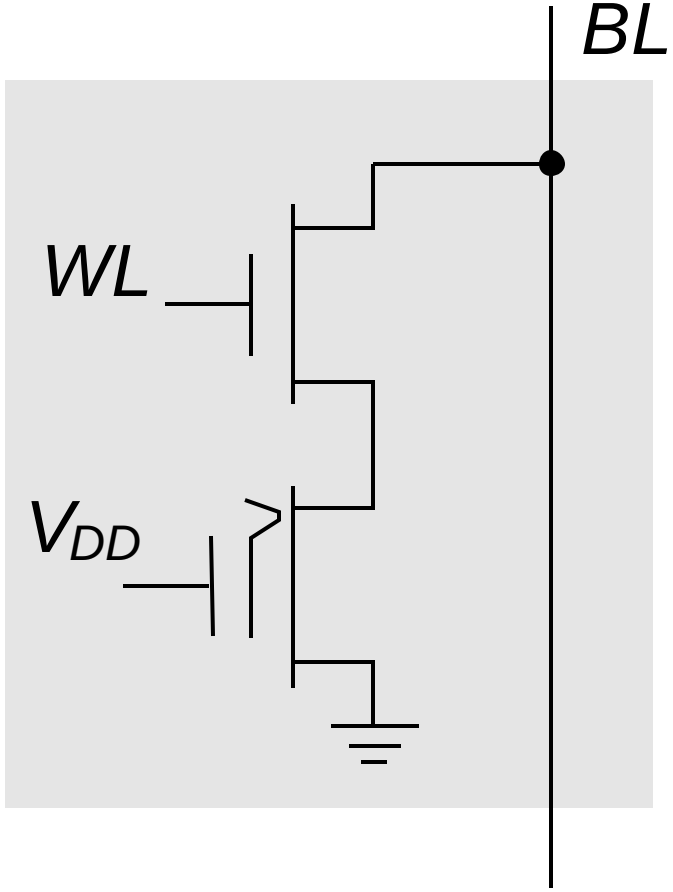


FLOTOX transistor



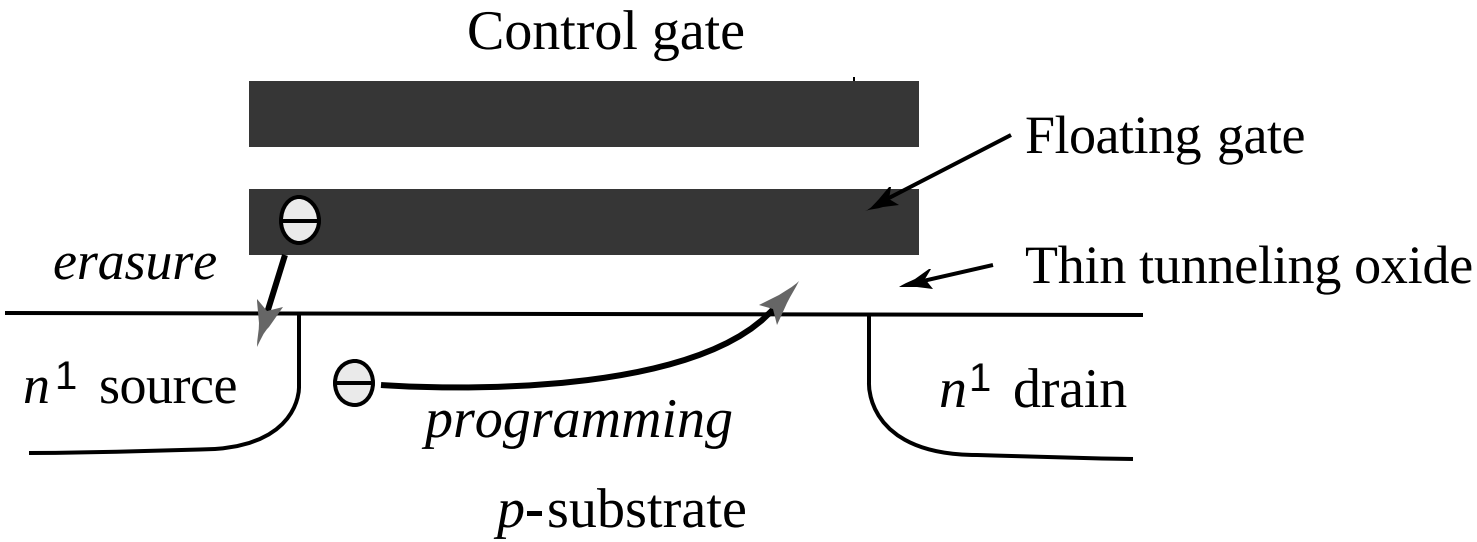
Fowler-Nordheim
I-V characteristic

EEPROM Cell



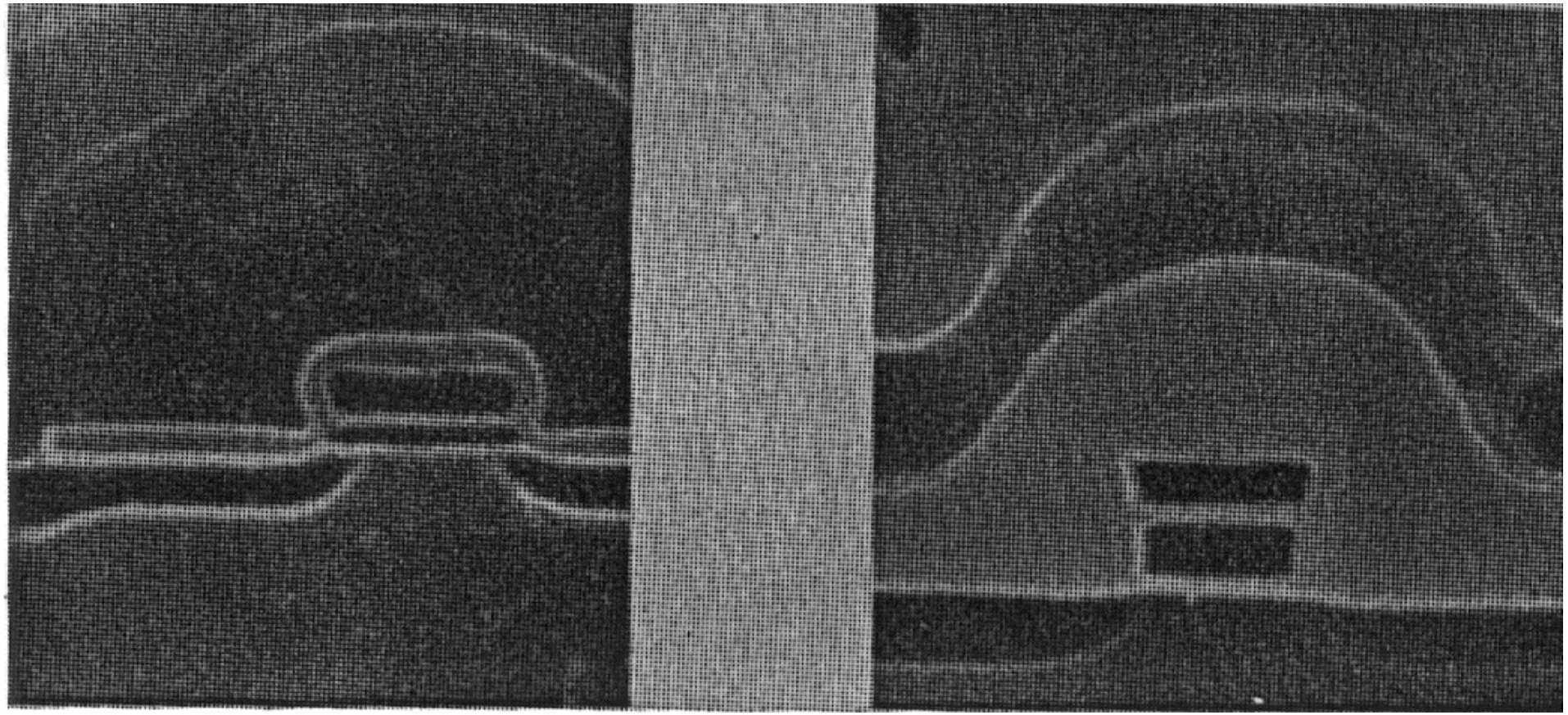
Absolute threshold control is hard
Unprogrammed transistor might be depletion
⇨ 2 transistor cell

Flash EEPROM



Many other options …

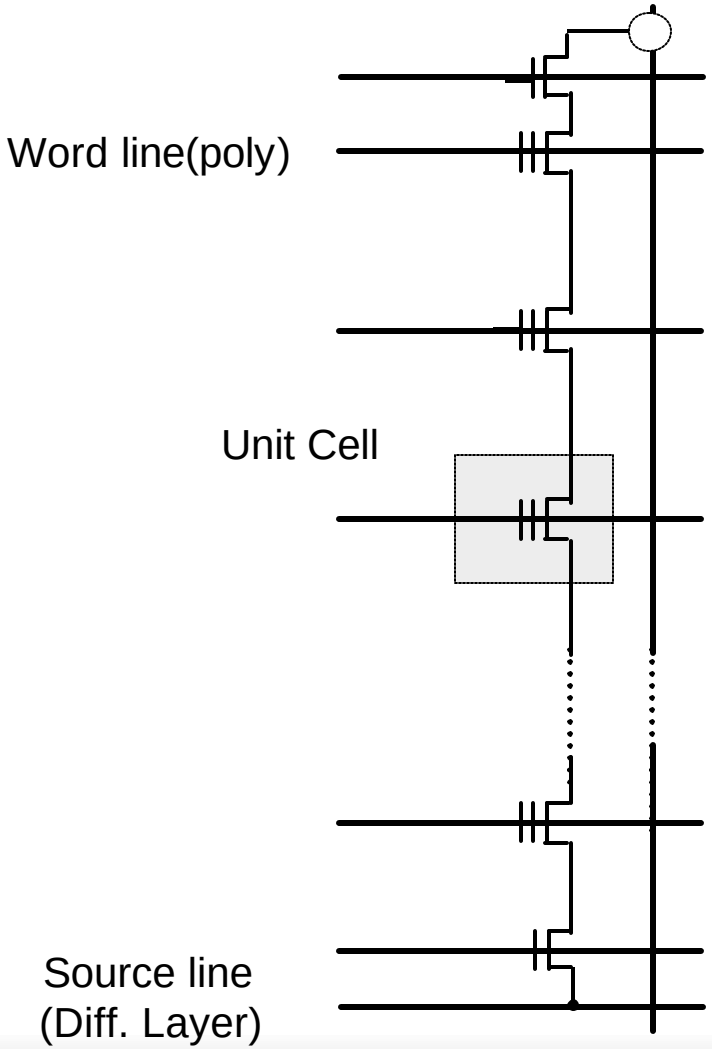
Cross-sections of NVM cells

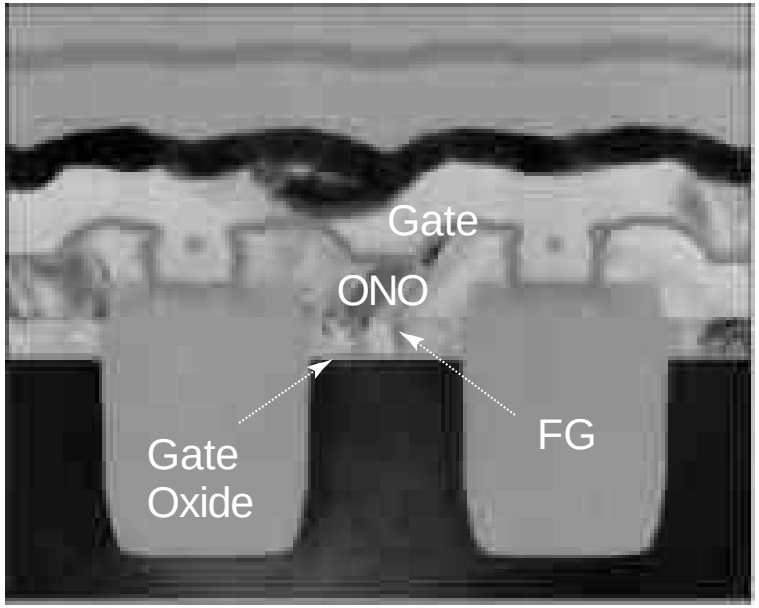


Flash EPROM

Courtesy Intel

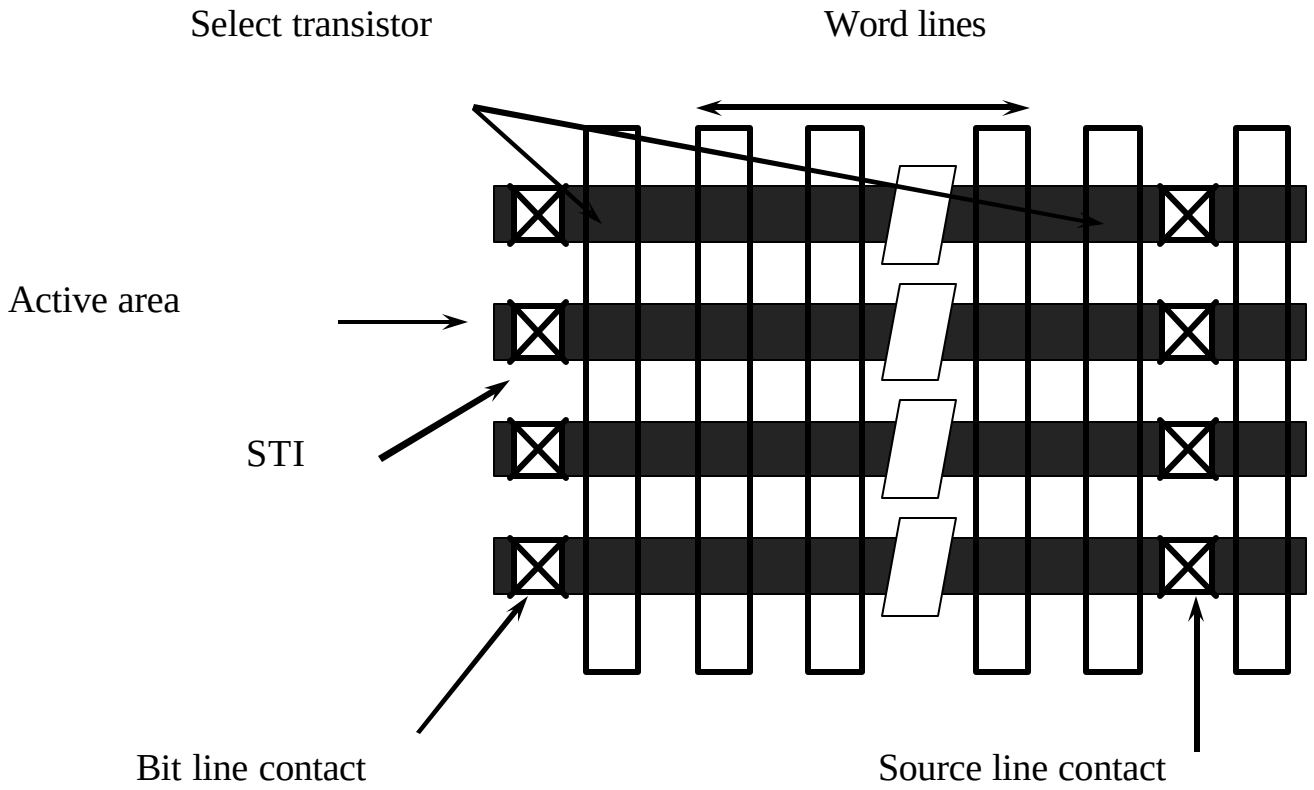
NAND Flash Memory





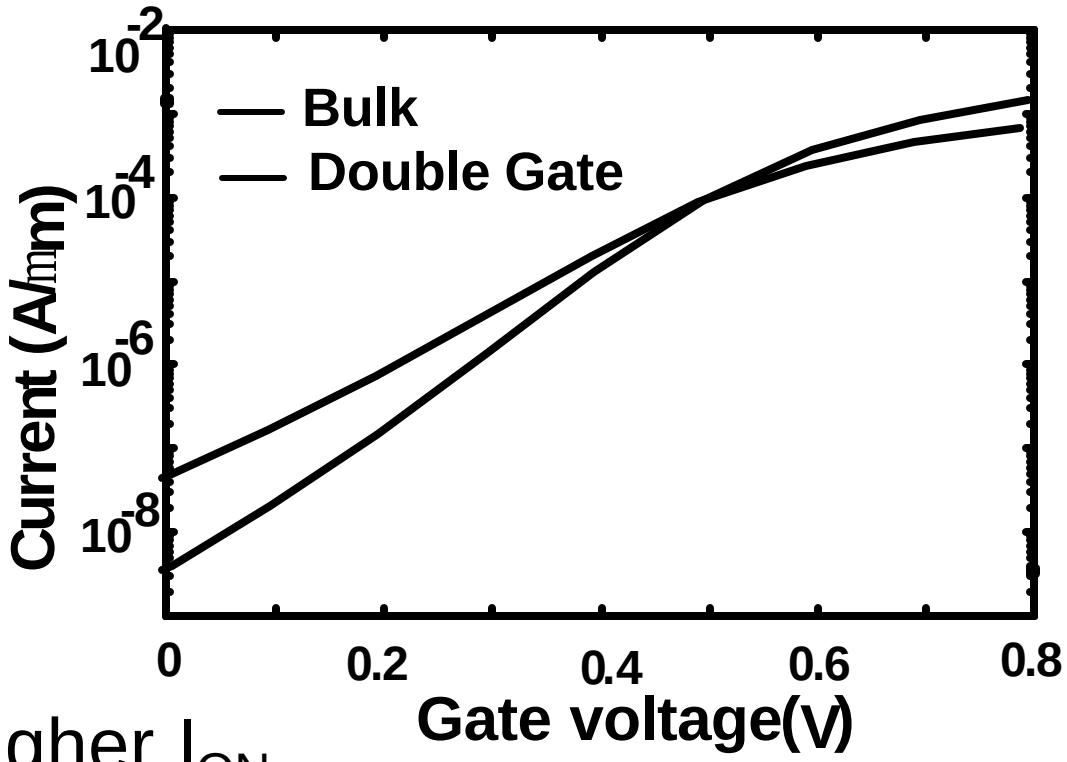
Courtesy Toshiba

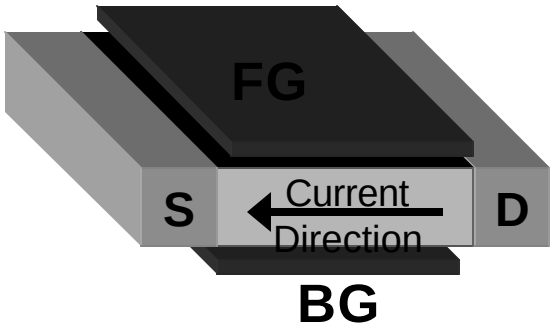
NAND Flash Memory



Courtesy Toshiba

FinFET Device Characteristics



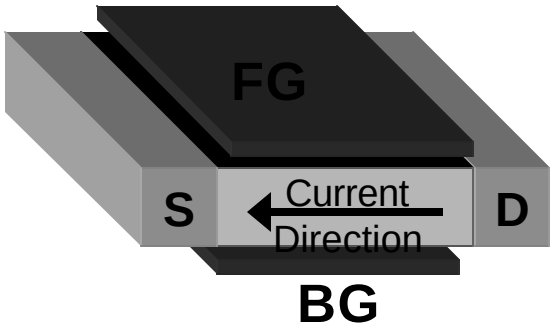


- Higher I_{ON}
- Lower leakage
- Near ideal (60 mV/decade) sub-threshold swing

Capacitorless Double-Gate DRAM

- Changing the V_T of the device by trapping the charge in thin body
- Using impact ionization

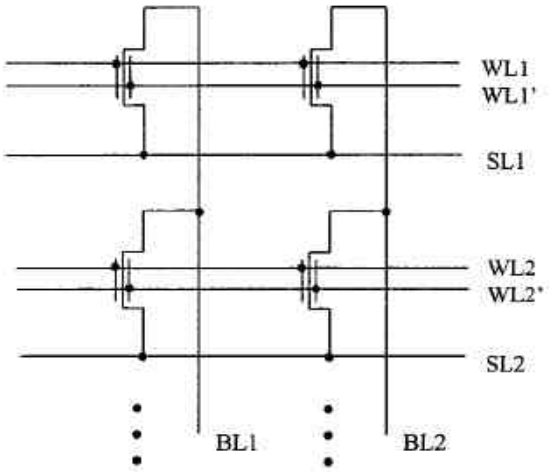
- Negative voltage is applied to body during programming



Capacitorless Double-Gate DRAM

- Large body coefficient

$$\frac{dV_T}{dV_{BS}} = \frac{dV_T}{dV_G} \times \frac{dV_G}{dQ_{inv}} \times \frac{dQ_{inv}}{dV_{BS}} = -\frac{C_{Si}}{C_{ox}} = -\frac{3T_{ox}}{T_{Si}}$$



	PGM (0/1)	HOLD	READ	PURGE
WL1	1.5V	-0.5V	1.5V	1.5V
WL1'	-1.5V	-0.5V	-1.5V	-0.5V
BL1	0.5V/1.5V	0.5V	0.5V	0.5V
SL1	0V	0.5V	0V	0V
WL2	-0.5V	-0.5V	-0.5V	-0.5V
WL2'	-0.5V	-0.5V	-0.5V	-0.5V
BL2	0.5V/1.5V	0.5V	0.5V	0.5V
SL2	0.5V	0.5V	0.5V	0.5V

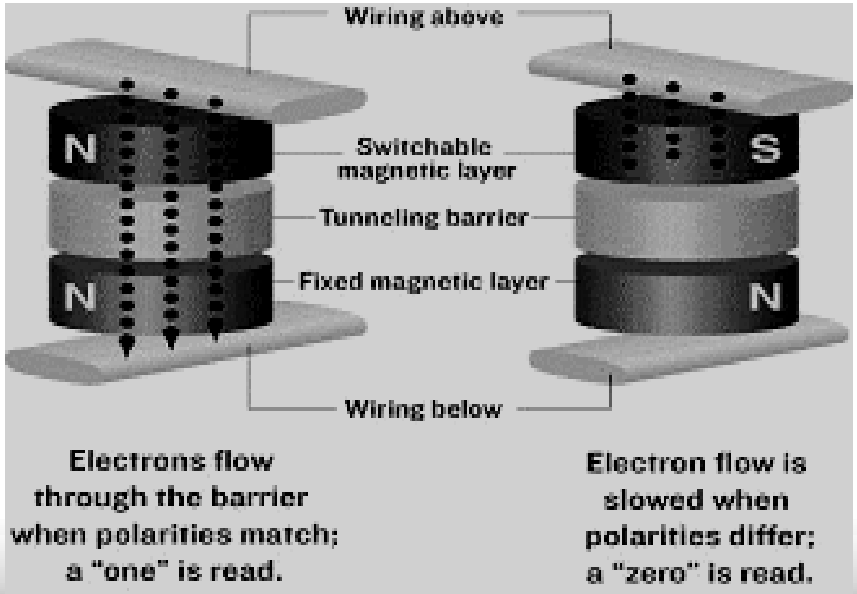
Cell Parameters:

$N_{body} = 10^{16}$ cm^{-3} (p-type)	$N_{S/D} = 10^{20}$ cm^{-3} (n-type)
$T_{ox} = 50$Å	$T_{body} = 100$Å
$L_{gate} = 50$nm	$\phi_{gate} = 4.4$eV
$\tau_{electron} = 1\mu s$	$\tau_{hole} = 1\mu s$

Capacitorless DRAM Array Structure

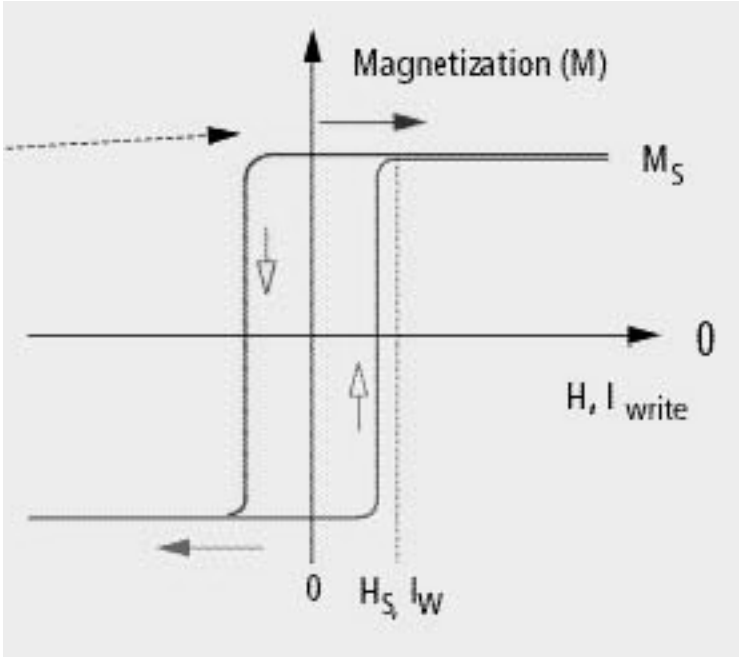
Magnetic RAM

- **Power efficiency**
  - MRAM can be the most efficient memory device in power consumption
- **Ferro-magnet**
  - Ferro-magnet is the type of material used to create a MTJ to develop MRAM



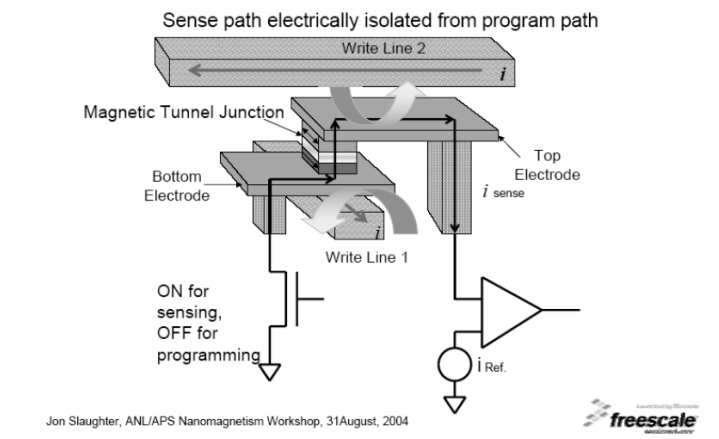
Basic Principles

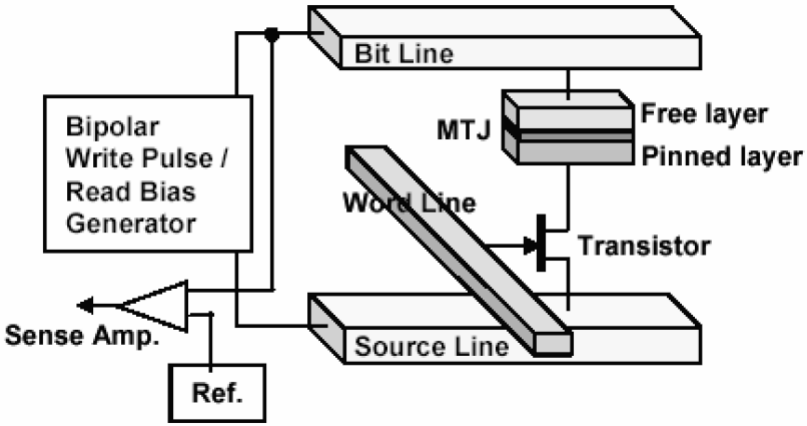
- The 2 Possible Magnetization States of a Ferromagnetic Element can be Described by a Hysteresis Loop
- Magnetization of Film vs. Magnetic Field



- *A magnetic field, with magnitude greater than the switching field, sets magnetization in direction of applied field*

Conventional MRAM (toggle) and Spin Torque MRAM





H *field produces torque to reverse free layer.*

- *Need* $I_{sw} \sim$ *40 mA/bit for 0.4 um x 1.0 um.*
- I_{sw} *constant for smaller bits.*

Spin polarized current produces torque to reverse free layer.

- I_{sw} *< 1 mA/bit for 0.06* ㎜ *x 0.12* ㎜ *bit.*
- I_{sw} *reduces as bit scales smaller.*

Summary

- Importance
  - Potentially Substantial Impact on Society
  - Potentially Central to Computers and Electronics that Engineers are Designing
- The Future of MRAM
  - Expected to Replace SRAM, DRAM, & FLASH
  - Predicted to be the Memory Standard in both Computers & Consumer Electronics
- Indicators of a Breakthrough
  - Price of MRAM is Equivalent to or Only Slightly More than DRAM & FLASH
  - MRAM is More Common in New PCs than DRAM & More Common in New Electronics than FLASH

Summary

- Researchers' Predictions
  - MRAMs Influence Will Not Occur Overnight
  - Production of MRAM will Gradually Increase Until Production is Large Enough that the Price is Equivalent to DRAM & FLASH
  - MRAM will Impact both the Computer Market & the Electronics Market
  - MRAM will be a Well-Known Product in 2 - 3 Years and the Memory Standard in Computers & Consumer Electronics in 3 - 4 Years