ECE 225
High-Speed Digital IC Design

Lecture 8

Review of Basic Circuit Styles-3
Dynamic CMOS
Variation Tolerant Keeper Design

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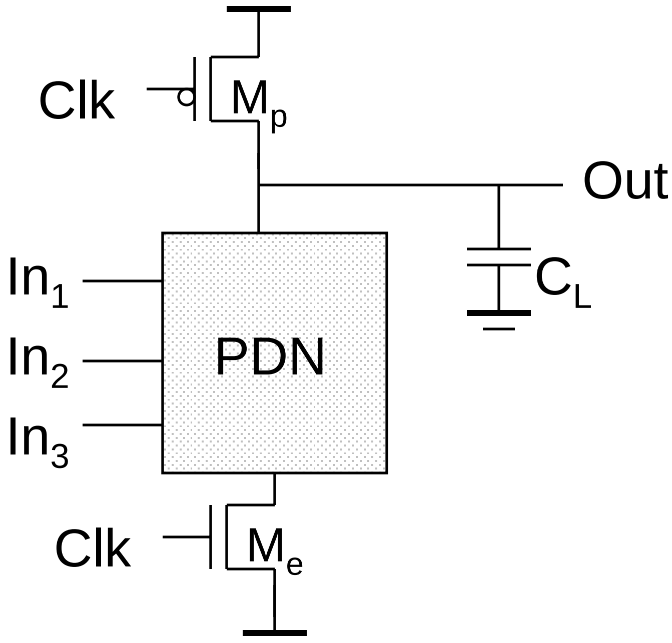
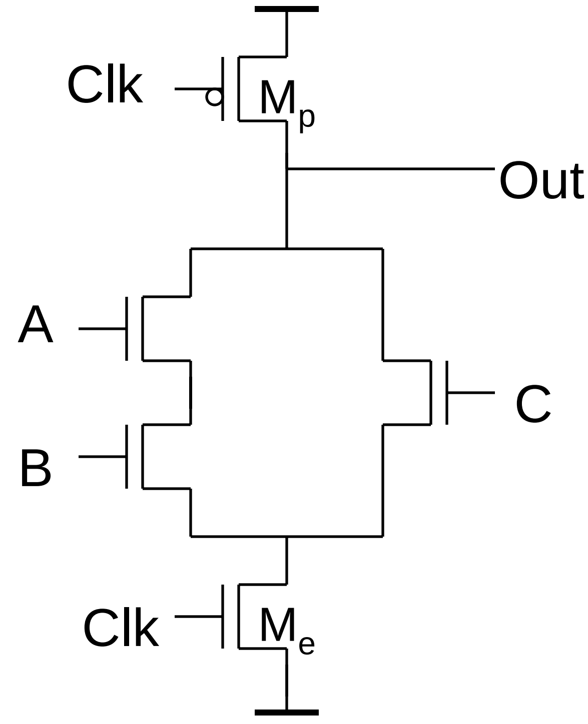
Dynamic CMOS

- In static circuits at every point in time (except when switching) the output is connected to either GND or V_{DD} via a low resistance path.
  - fan-in of *n* requires 2*n* (*n* N-type + *n* P-type) devices
- Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance nodes.
  - requires only *n* + 2 (*n*+1 N-type and 1 P-type) transistors

Dynamic Gate



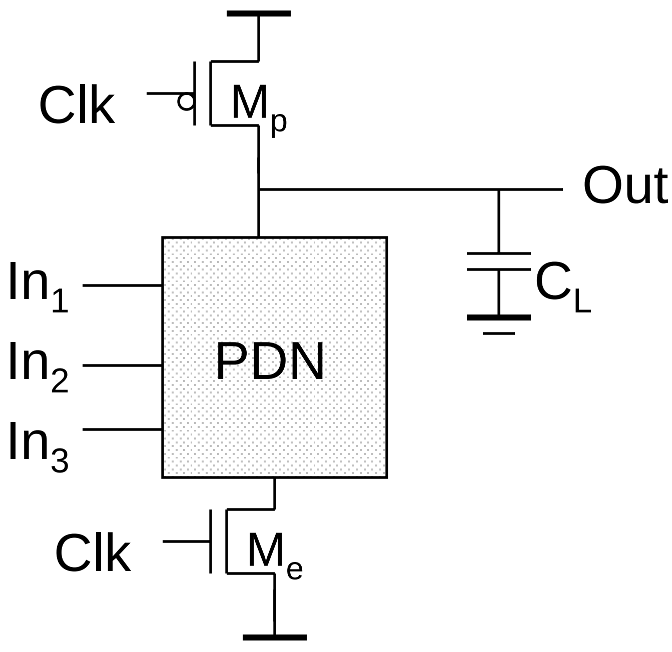


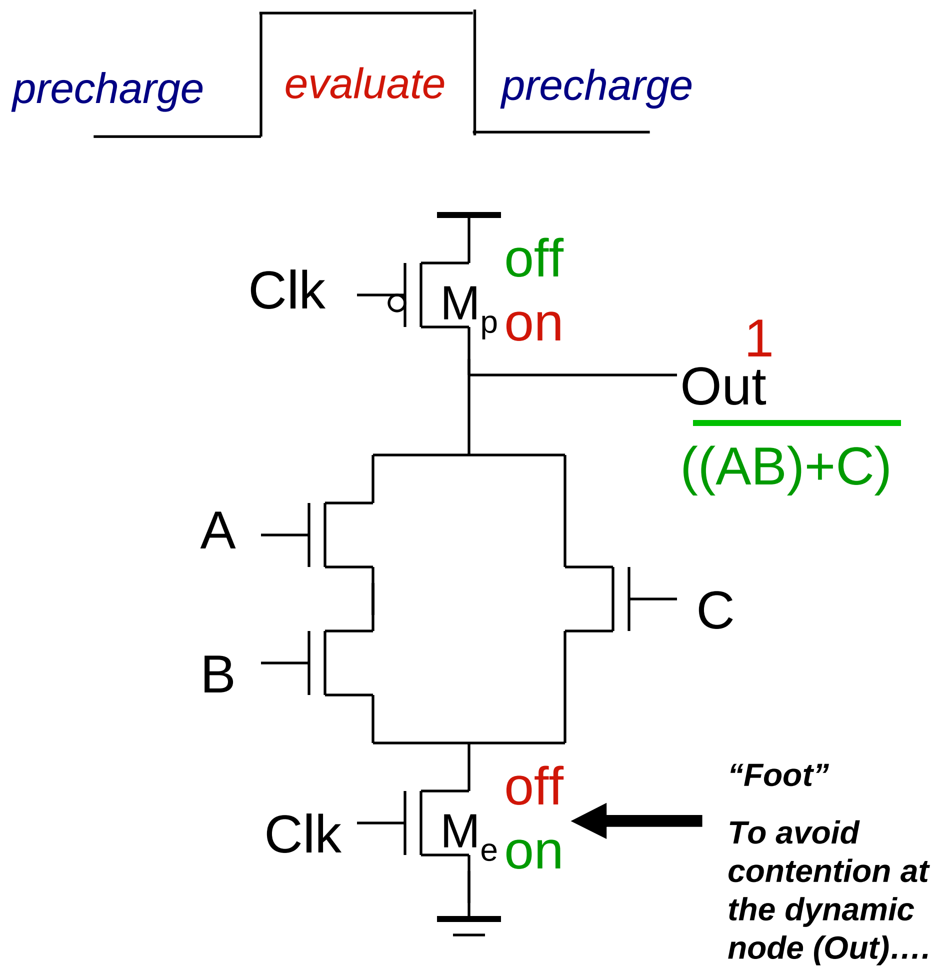
Two phase operation

Precharge (CLK = 0)

Evaluate (CLK = 1)

Dynamic Gate





Two phase operation

Precharge (Clk = 0)

Evaluate (Clk = 1)

$$Out = \overline{CLK} + \overline{(AB)+C} \cdot CLK$$

Conditions on Output

- During evaluation phase, the only possible path between output node and supply rail is to ground. Hence, once the output of a dynamic gate is discharged, it cannot be charged again until the next precharge operation.
- Inputs to the gate can make at most one transition during evaluation.
- Output can be in the high-impedance state during and after evaluation (if PDN is off), state is stored on C_L

Properties of Dynamic Gates

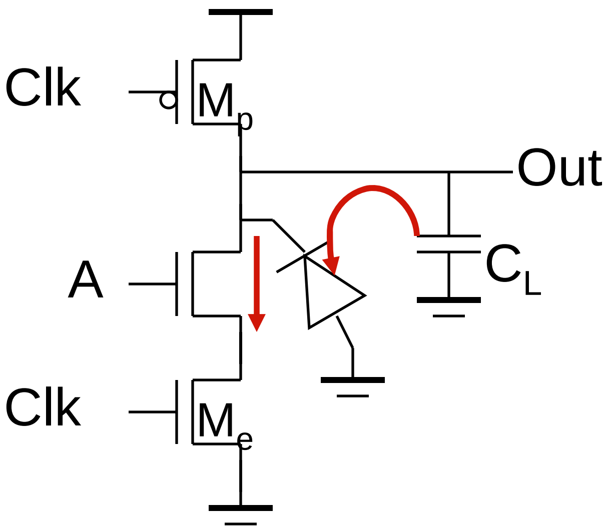
- Logic function is implemented by the PDN only
  - number of transistors is N + 2 (versus 2N for static complementary CMOS)
- Full swing outputs (V_{OL} = GND and $V_{OH} = V_{DD}$)
- Non-ratioed - sizing of the devices does not affect the logic levels
- PDN starts to work as soon as the input signals exceed V_{Tn}, so V_M, V_{IH} and V_{IL} equal to V_{Tn}
- Low noise margin (NM_L)
- Needs a precharge/evaluate clock
- Faster switching speeds
  - reduced load capacitance due to lower input capacitance (C_{in}) due to lower number of transistors per gate and single transistor load per fan-in (reduced logical effort, 2/3 for a 2-input dynamic NOR)
  - no I_{sc}, so all the current provided by PDN goes into discharging C_L

Properties of Dynamic Gates

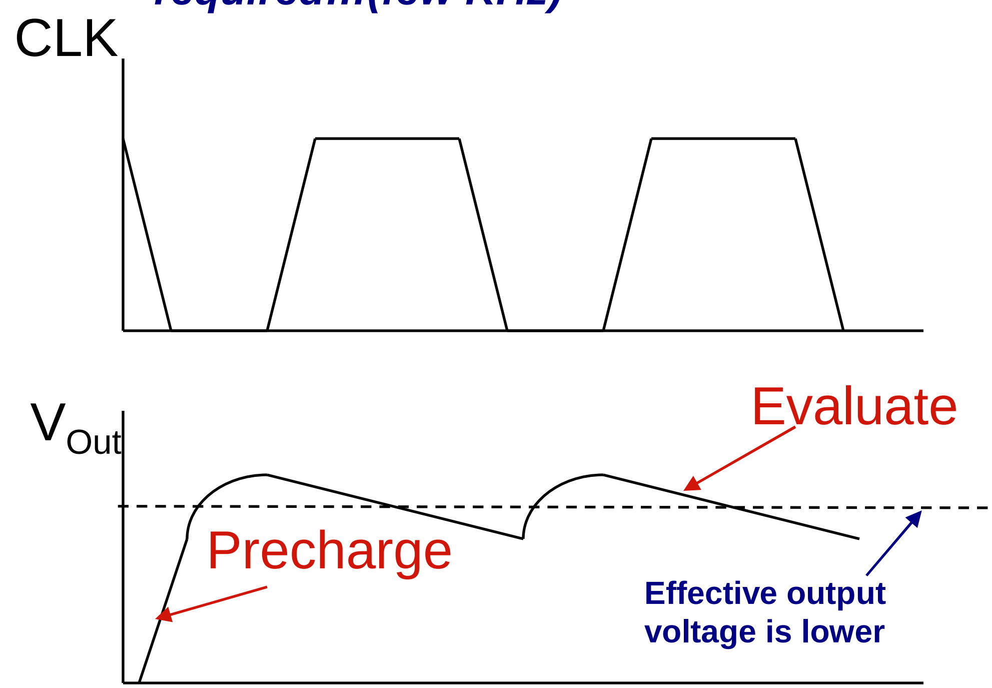
- Advantages:
  - Lower physical capacitance: uses fewer transistors
  - No glitching (dynamic gates can have at most one transition per CLK cycle)
  - Only consumes dynamic power…..no static current path ever exists between V_{DD} and GND (including P_{sc})
- In spite of the above…..overall power dissipation usually higher than static CMOS
  - CLK power can be significant: extra load on Clk + transition every CLK cycle
  - Number of transistors is more than the minimal set required for implementing logic
  - Higher switching activity due to higher transition probabilities

Issues in Dynamic Design 1: Charge Leakage

A dynamic inverter



Due to leakage, a minimal CLK rate required…(few KHz)



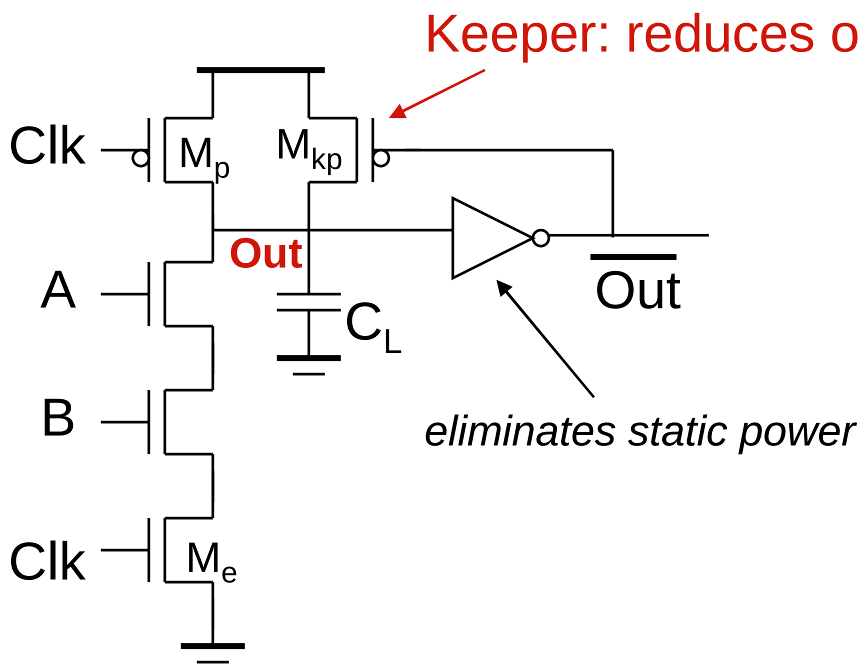
Leakage sources: reverse biased diode and subthreshold

Dominant component is subthreshold current

Note: leakage of precharge PMOS can partially compensate for the charge loss at the dynamic node

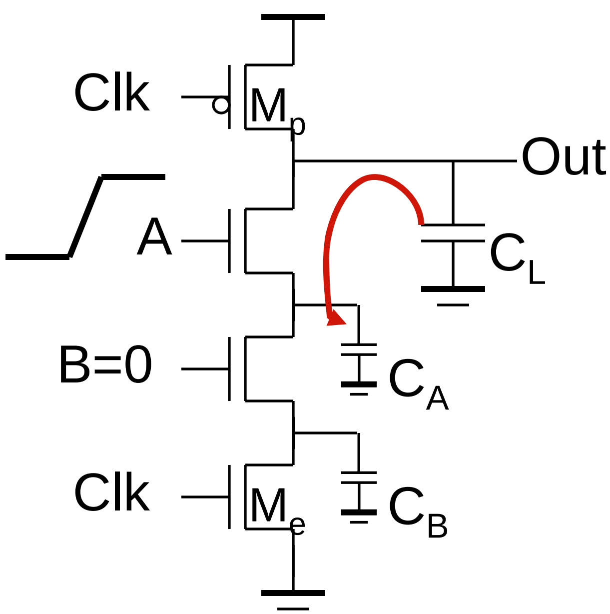
Solution to Charge Leakage

Same approach as level restorer for pass-transistor logic



Contention between keeper and PDN--- strength of keeper must be less than that of the PDN to lower the out node well below the switching threshold of the next gate. Hence keeper size should be small.

Issues in Dynamic Design 2: Charge Sharing



Charge stored originally on C_L is redistributed (shared) over C_L and C_A leading to reduced robustness

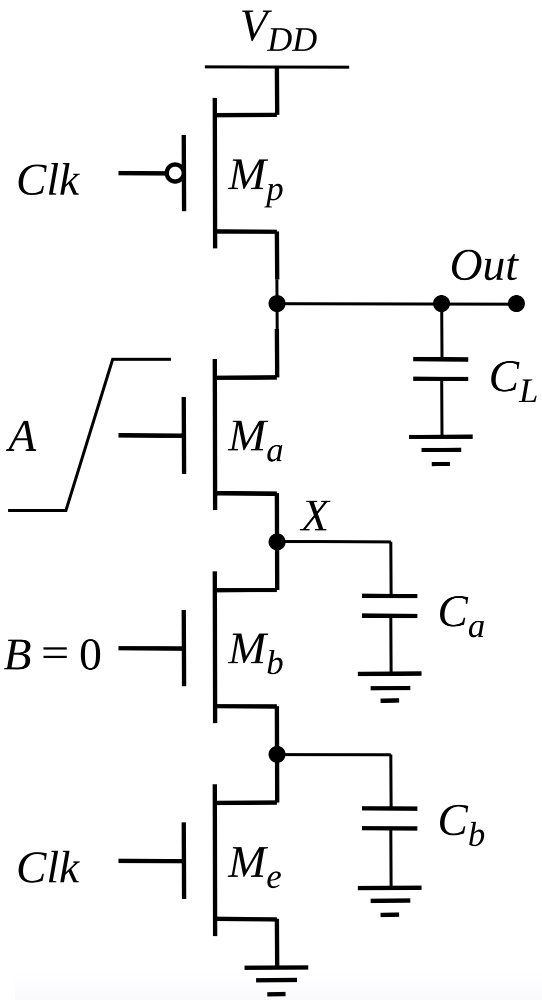
Output node voltage drops and cannot be recovered due to the dynamic nature of the circuit.

Charge Sharing

All inputs = 0 during pre-charge

Initial conditions: $V_{out}(t=0)=V_{DD}$ and $V_x(t=0)=0$

2 possible scenarios:



case 1) if $\Delta V_{out} < V_{Tn}$

Final value of V_X

$$C_L V_{DD} = C_L V_{out}(t) + C_a(V_{DD} - V_{Tn}(V_X))$$

or

$$\Delta V_{out} = V_{out}(t) - V_{DD} = -\frac{C_a}{C_L}(V_{DD} - V_{Tn}(V_X))$$

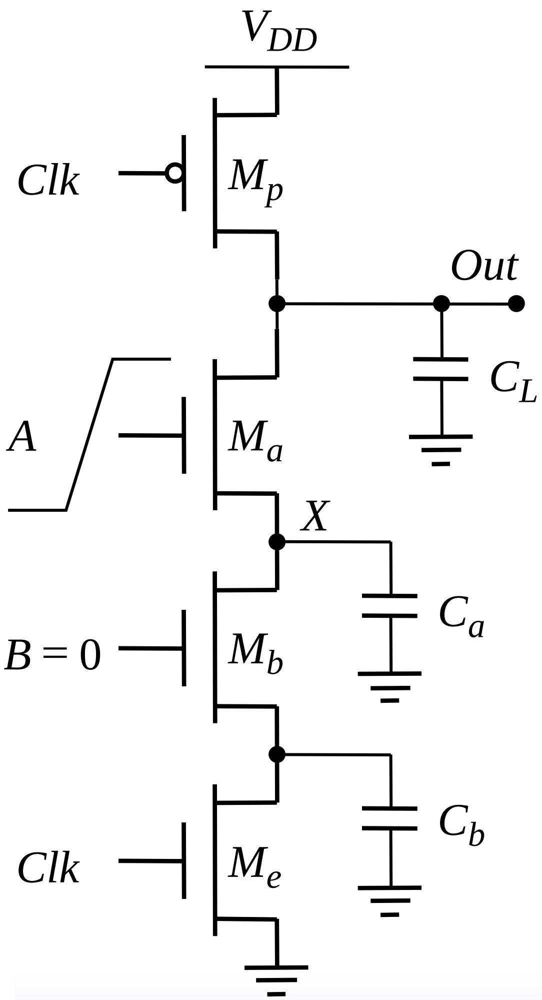
case 2) if $\Delta V_{out} > V_{Tn}$

V_{OUT} and V_X then reach the same value…..

$$\Delta V_{out} = -V_{DD}\left(\frac{C_a}{C_a + C_L}\right)$$

Which of these scenarios is valid?

Charge Sharing



Initial conditions: V_{out} (t=0)=V_{DD} and V_x(t=0)=0

2 possible scenarios:

$\Delta V_{out} < V_{Tn}$ ….case I

$\Delta V_{out} > V_{Tn}$ ….case II

Which of these scenarios is valid?

First find the capacitance ratio: C_a/C_L

The boundary condition between the two cases can be determined by setting $\Delta V_{out} = V_{Tn}$. Hence,

$$\frac{C_a}{C_L} = \frac{V_{Tn}}{V_{DD} - V_{Tn}}$$

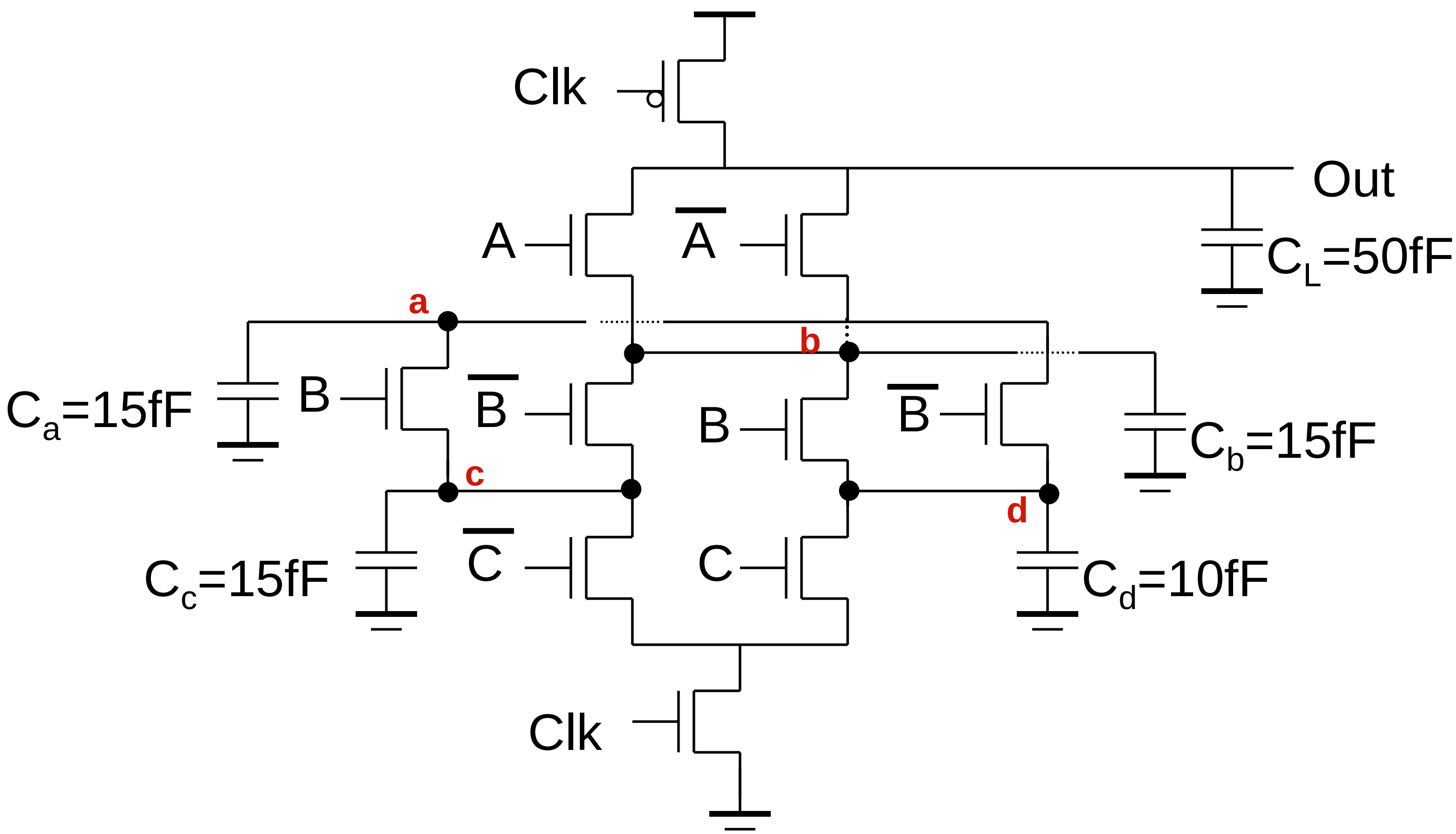
Case I holds when the C_a/C_L ratio is smaller than the value defined above, otherwise Case II holds.

Overall, it is desirable to keep $\Delta V_{out} < |V_{Tp}|$ ---since the output of dynamic gate might be connected to a static inverter---low level of V_{out} will cause static power consumption. Also, V_{out} must not go below V_M of the inverter.

Charge Sharing Example

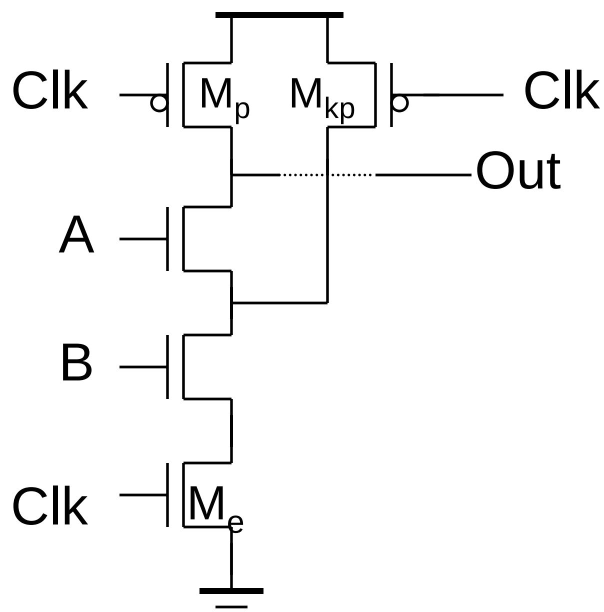
Dynamic 3-input EXOR gate

$$Out = A \oplus B \oplus C$$



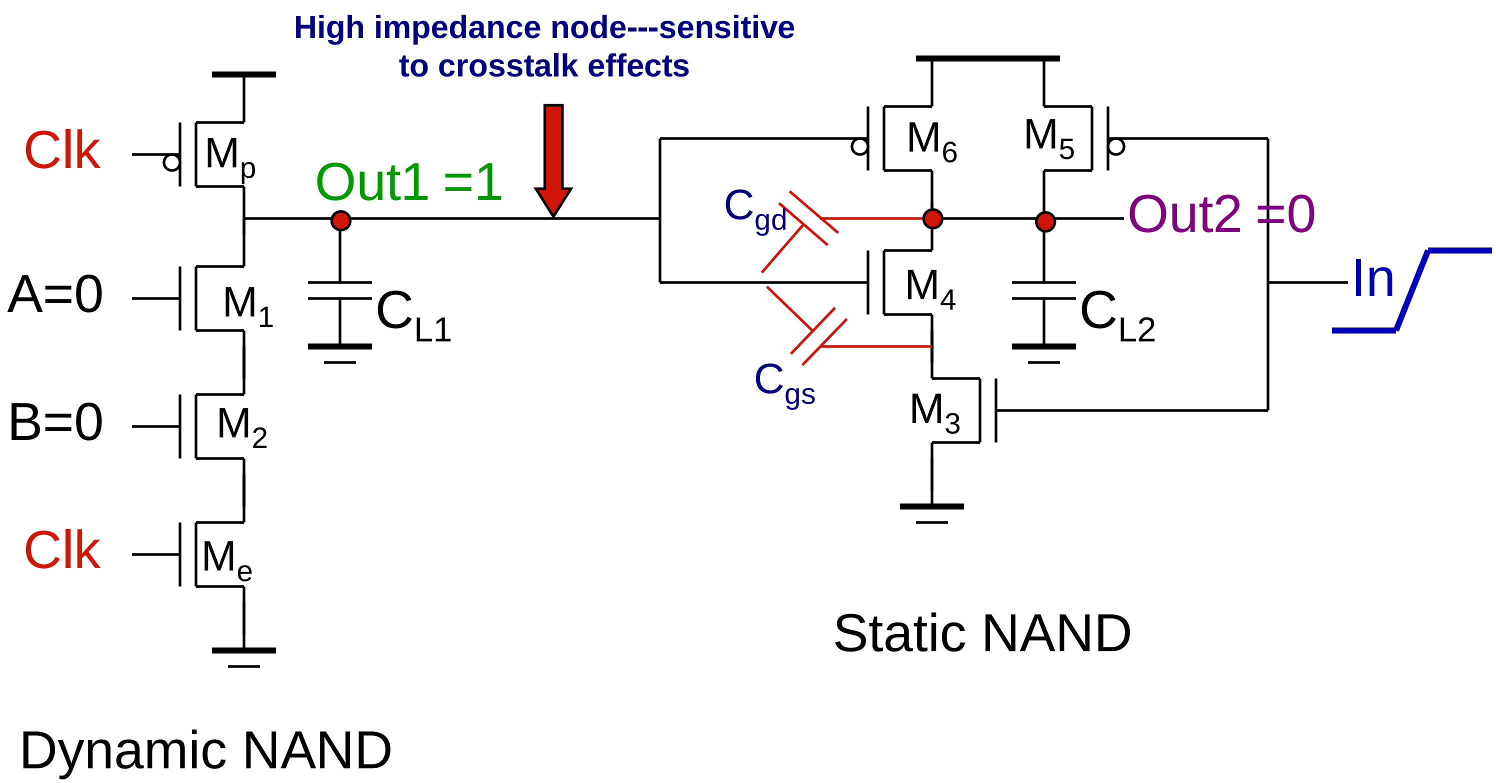
Worst case change in Output is obtained by exposing the maximum number of internal capacitances to the output: this happens for $\overline{A}BC$ or $A\overline{B}C$

Solution to Charge Redistribution



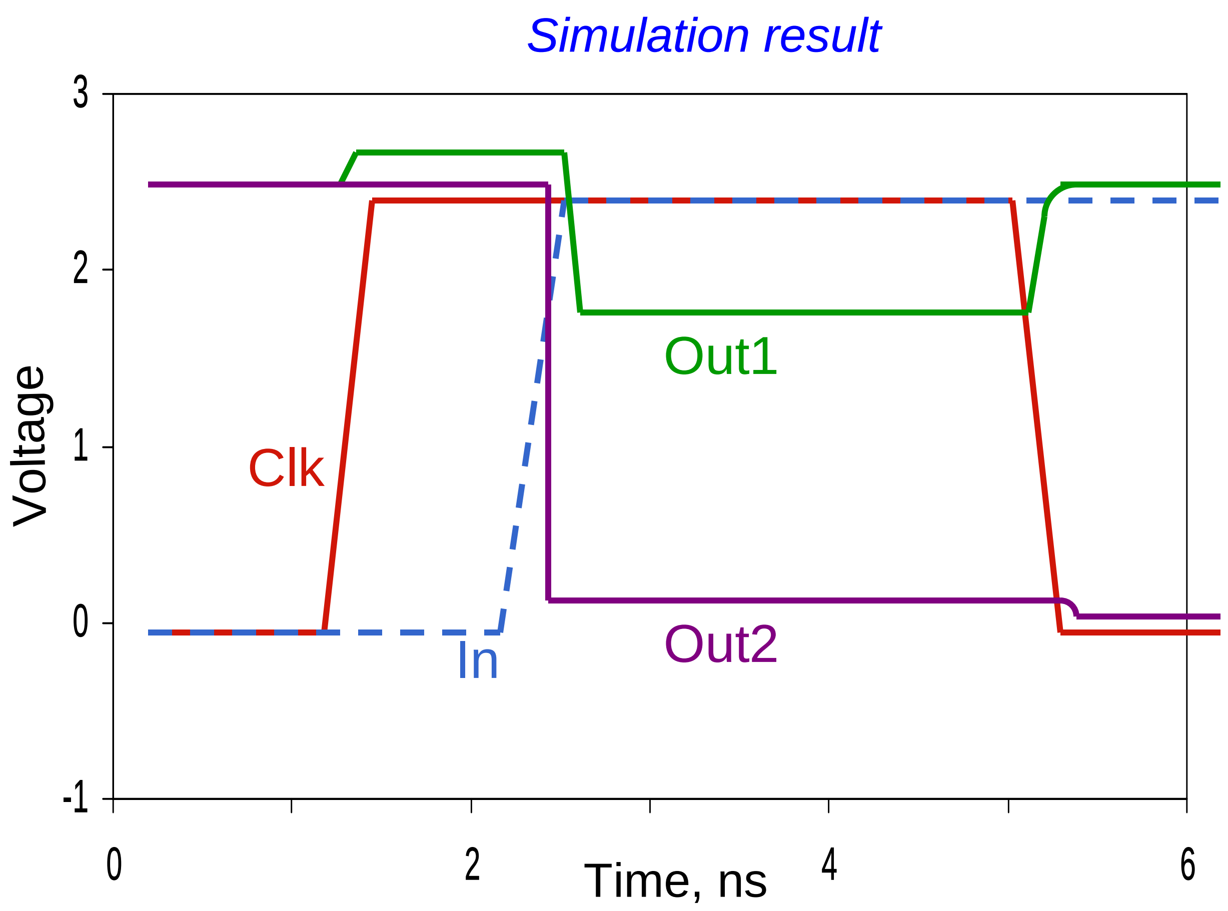
Precharge internal nodes (to V_{DD}) using a clock-driven transistor (at the cost of increased area and power)

Issues in Dynamic Design 3: Backgate Coupling



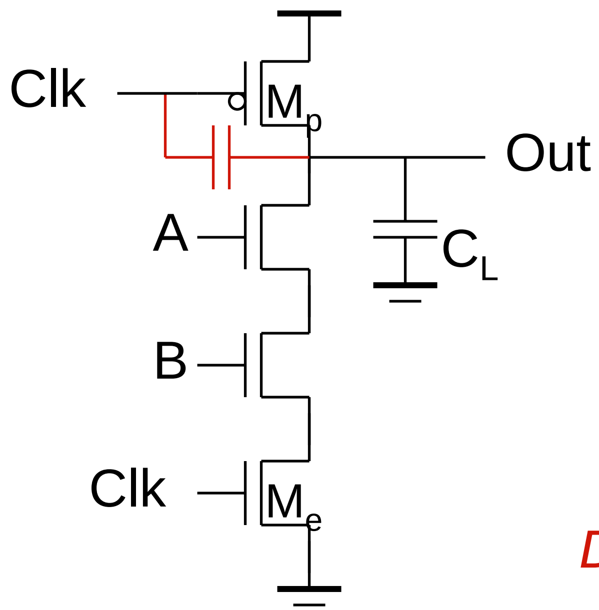
Capacitive coupling between dynamic node Out1 and H-L transition at Out2 through the gate-drain and gate-source capacitance of M4

Backgate Coupling Effect



Coupling causes dynamic node Out1 to drop significantly, which further prevents Out2 from dropping all the way to zero---static power dissipation.

Issues in Dynamic Design 4: Clock Feedthrough



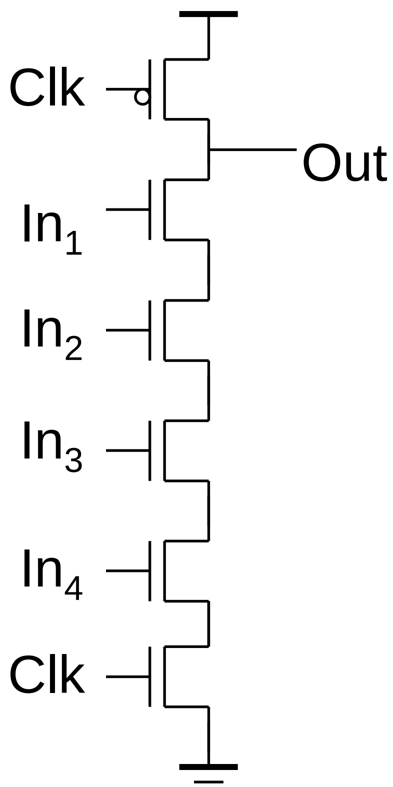
Coupling between Out and Clk input of the precharge device due to gate to drain capacitance (includes both overlap and channel).

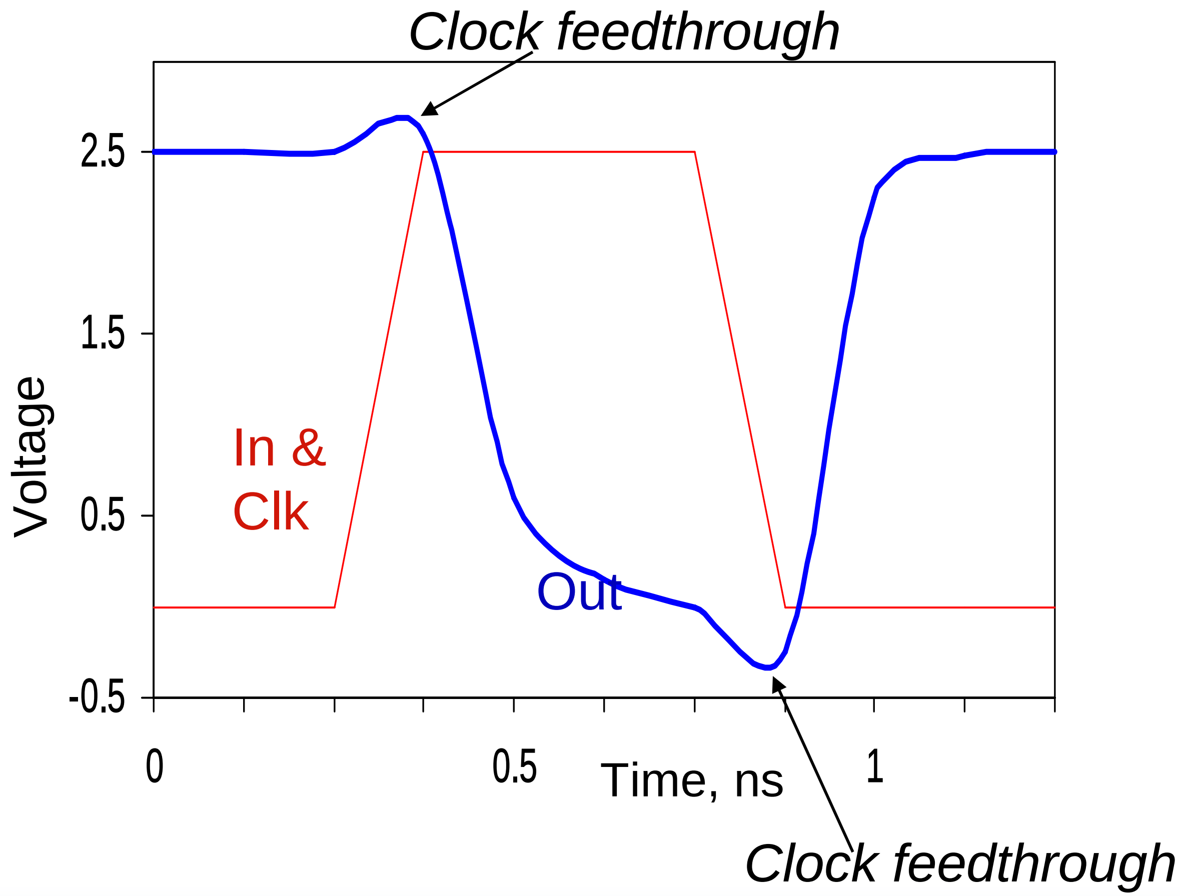
Hence, voltage of Out can rise above V_{DD} on the L-H Clk transition (assuming PDN is off). The fast rising (and falling edges) of the clock couple to Out.

Dynamic circuits need careful simulation!

Clk feedthrough can cause normally reverse biased junction diodes of the precharge transistor to become forward biased---causing electron injection into the substrate that can be collected by a nearby high-impedance node in the 1 state, eventually resulting in faulty operation.

Clock Feedthrough



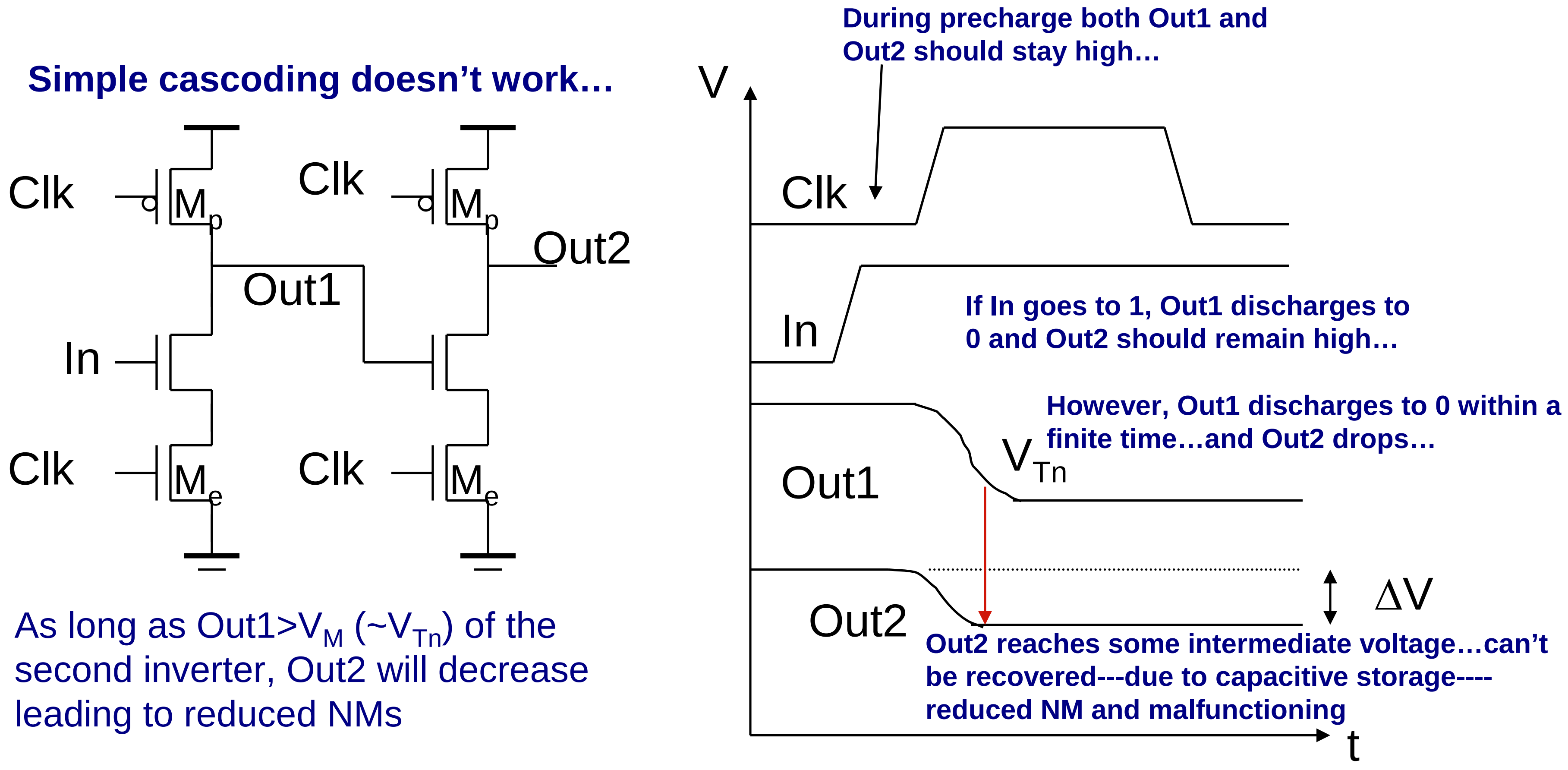


Other Effects

- Capacitive coupling
- Substrate coupling
- Minority charge injection
- Supply noise (ground bounce)

Cascading Dynamic Gates

Simple cascoding doesn't work…



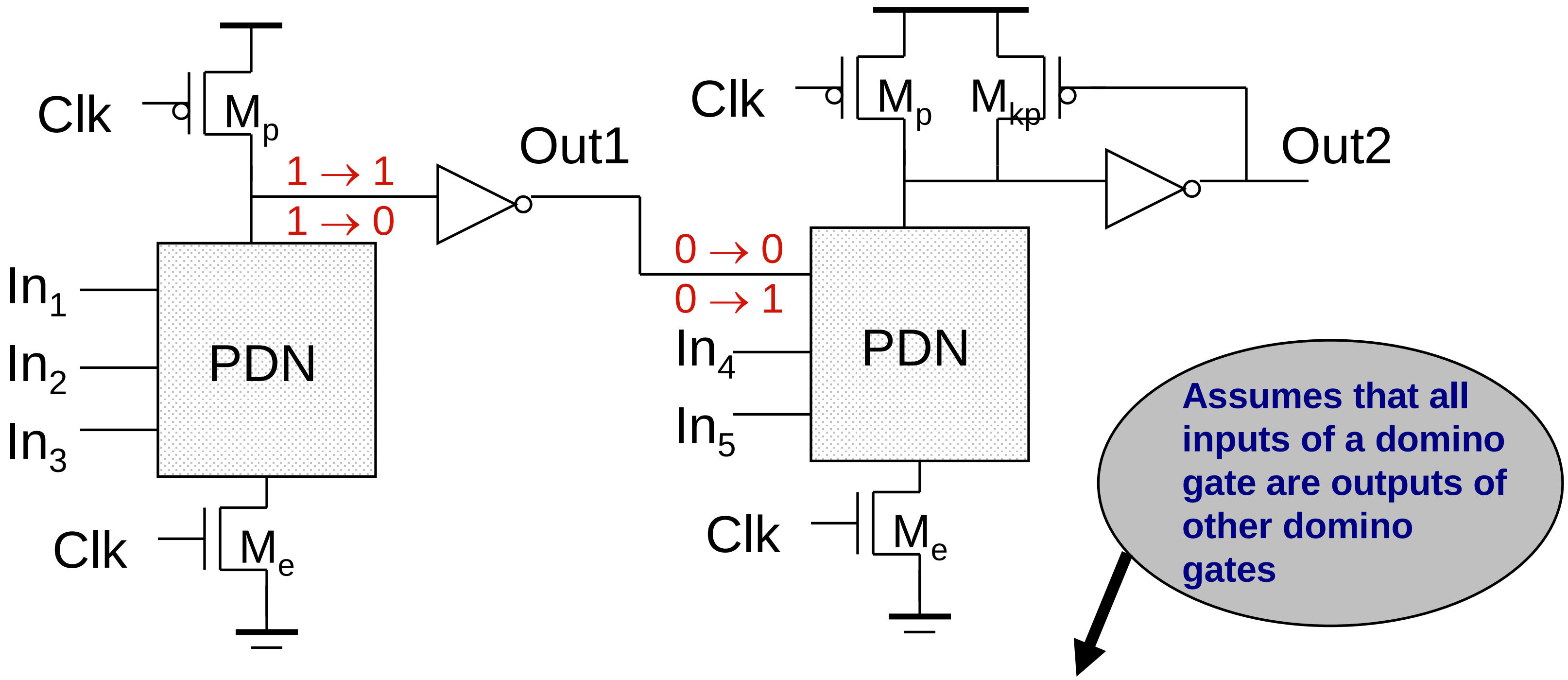
As long as Out1>V_M (~V_{Tn}) of the second inverter, Out2 will decrease leading to reduced NMs

Solution: Set all inputs to 0 during precharge

For correct operation only 0 $\rightarrow$ 1 transitions should be allowed at inputs!

Domino Logic

An n-type dynamic logic followed by a static inverter…

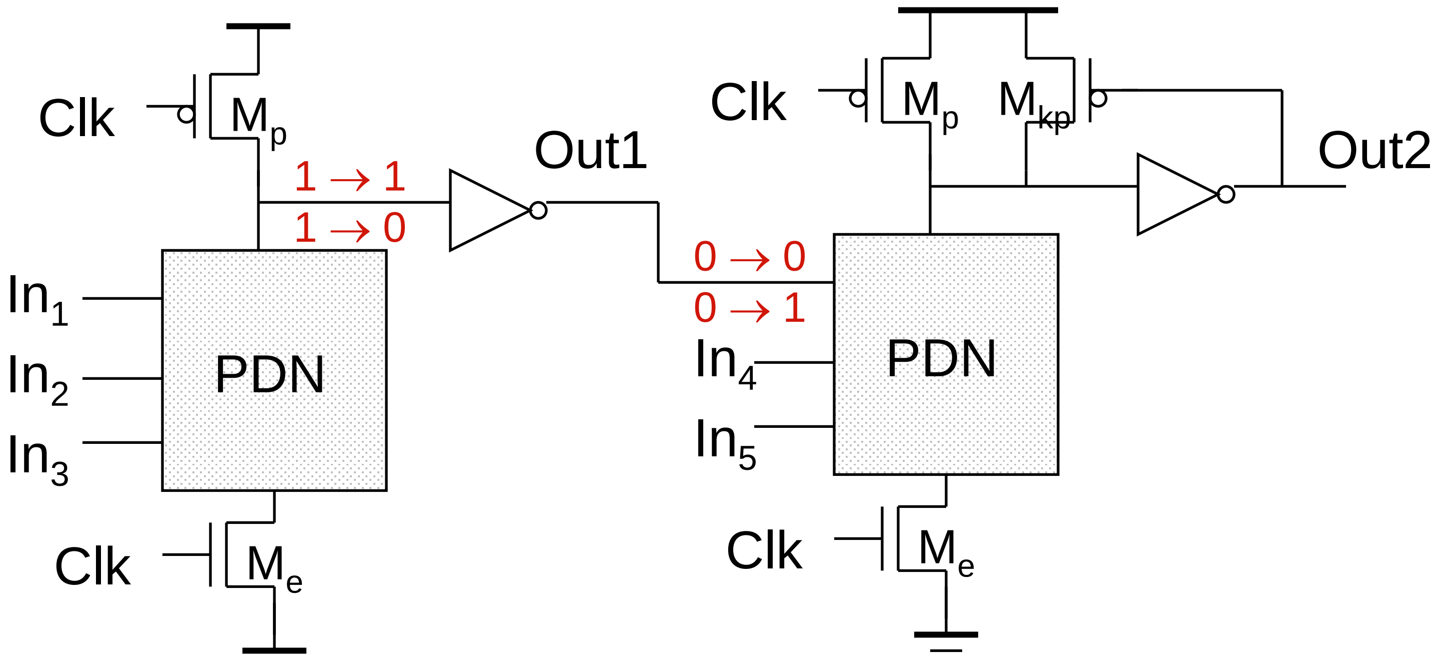


All inputs (are outputs of other Domino gates) are set to 0 at the end of precharge phase

Only 0 to 1 transition at the inputs during evaluation phase:
during evaluation, dynamic gate conditionally discharges and the output of the inverter makes a conditional transition from 0 to 1.

Domino Logic

An n-type dynamic logic followed by a static inverter…

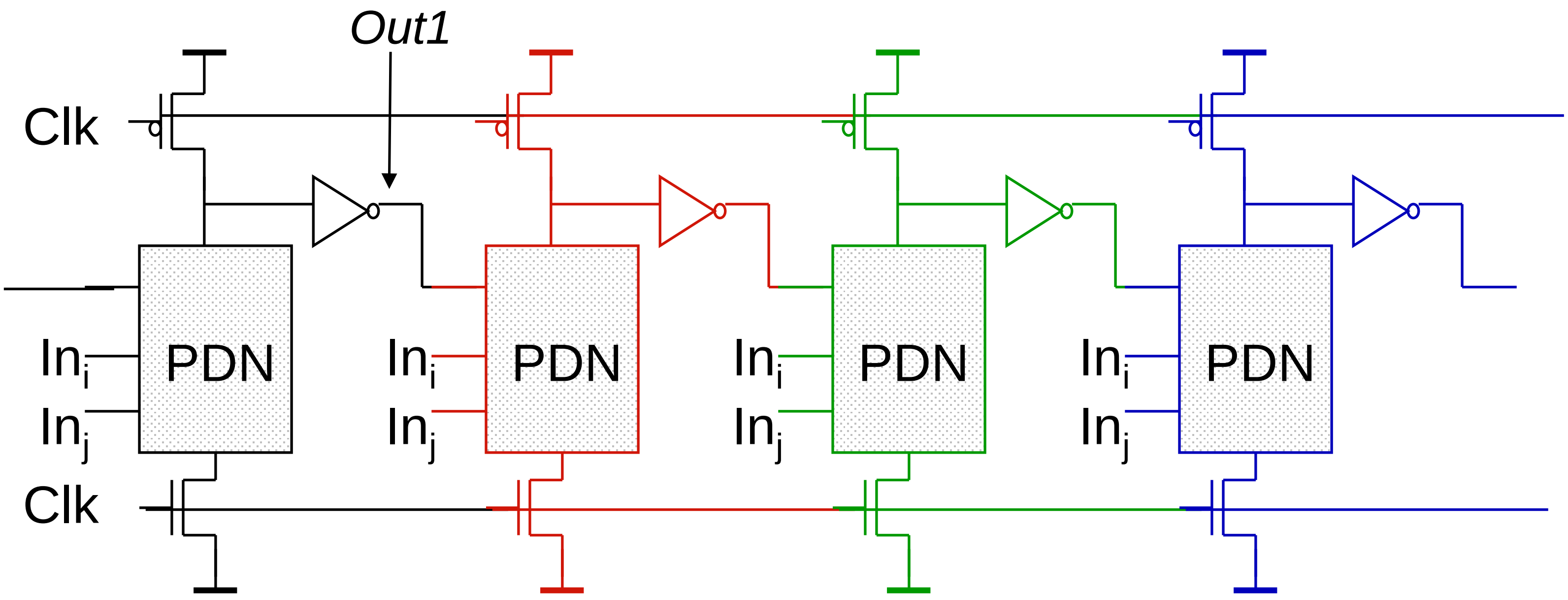


The static inverter reduces the capacitance of the dynamic output node by separating internal and load capacitances…..it also increases the NM (due to the low-impedance output)

The inverter can also be used to drive a keeper device to combat leakage and charge redistribution.

Why Domino?

A Domino chain



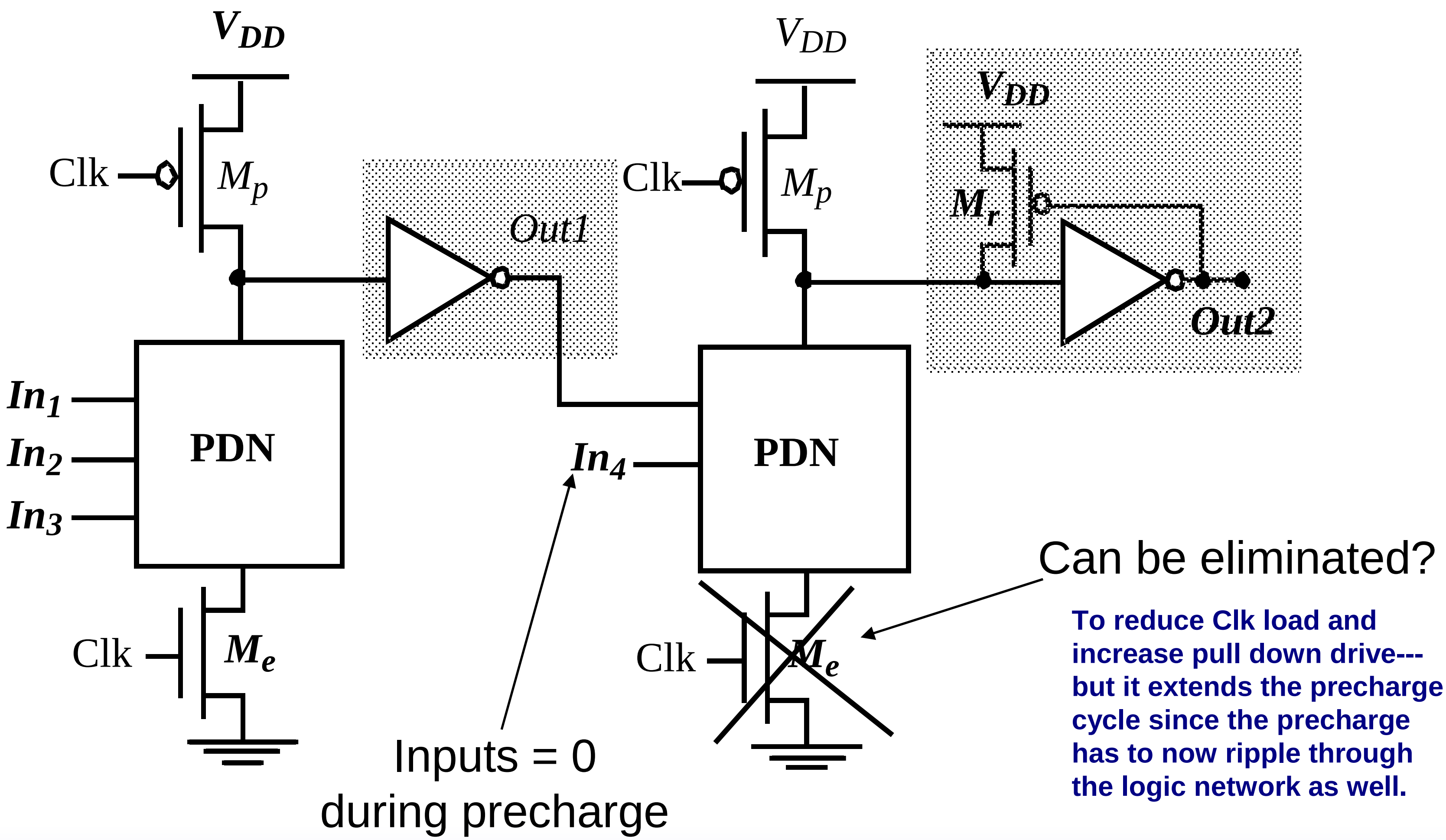
Precharge: all inputs=0

Evaluation: Output of domino1 either stays at 0 or makes a transition from 0 to 1, affecting the second gate. This effect might ripple through the whole chain…***like a line of falling dominos!***

Properties of Domino CMOS Logic

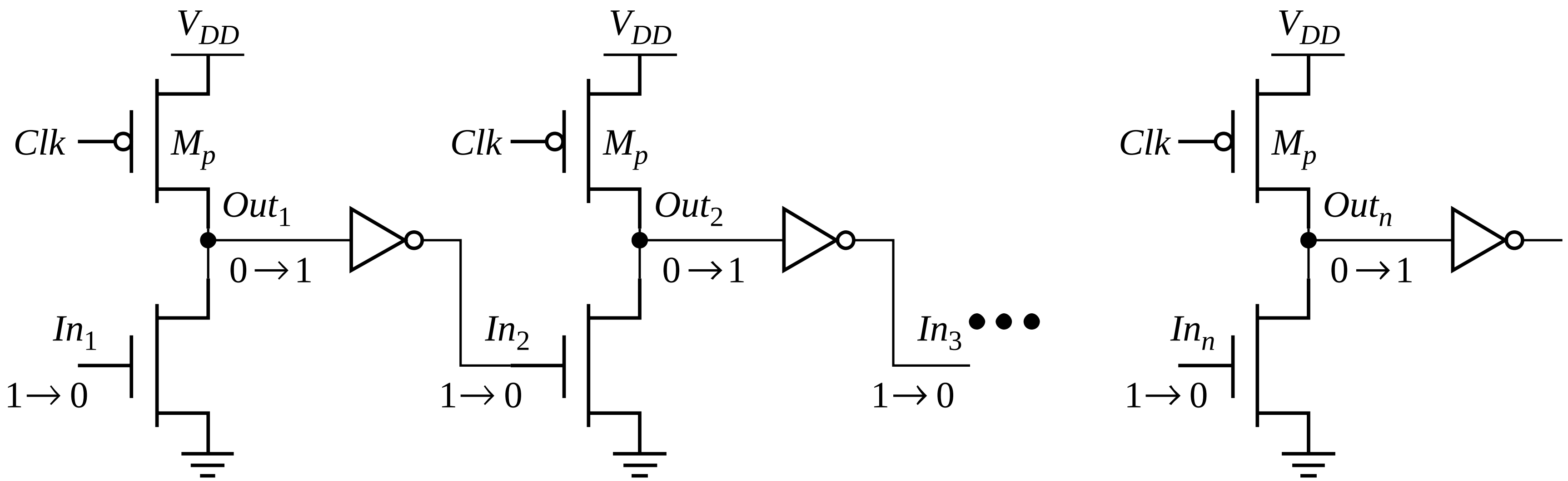
- Only non-inverting logic can be implemented (due to the static inverter)
  - Major limitation
  - Can be overcome using dual-rail domino (an expensive solution)
- Very high speed
  - Only rising edge delays, and $t_{pHL}=0$
  - static inverter can be skewed to match the fanout, which is already much smaller than in the complimentary case, since only a single gate capacitance needs to be accounted for per fan-out gate.
  - Input capacitance reduced – smaller logical effort

Designing with Domino Logic



To reduce Clk load and increase pull down drive--- but it extends the precharge cycle since the precharge has to now ripple through the logic network as well.

Footless Domino



If In_1=1, out_1=0 and In_2=1

On the falling edge of CLK, let In_1 =0: but it takes two gate delays for In_2 to be 0, during which second gate cannot pre-charge its output (Out_2), since PDN is fighting the precharge-PMOS

Time taken to precharge equals the critical path delay!

Better to use the evaluation device….

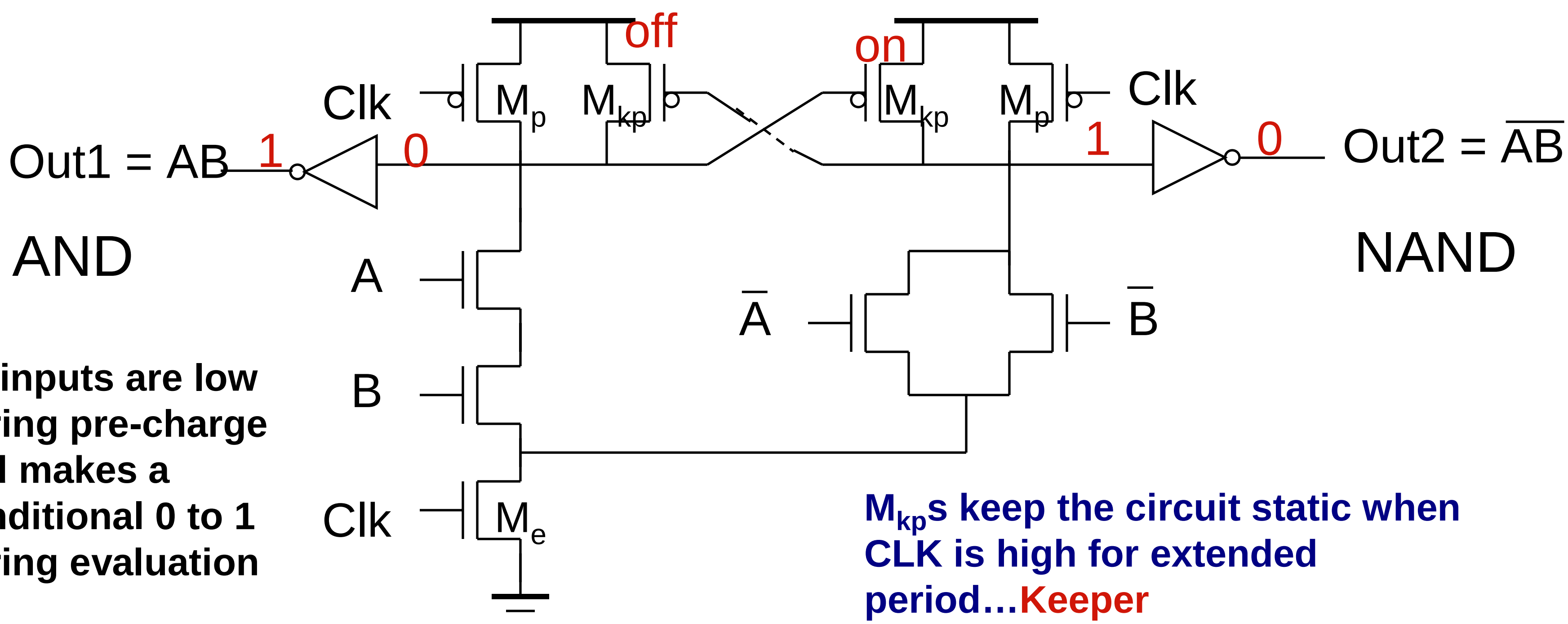
Pre-charge is rippling – short-circuit current

A solution is to delay the clock for each stage

Differential (Dual Rail) Domino

Overcomes the non-inverting property of Domino Logic: used commercially in several microprocessors

Uses a pre-charged load….



All inputs are low during pre-charge and makes a conditional 0 to 1 during evaluation

M_{kp}s keep the circuit static when CLK is high for extended period…Keeper

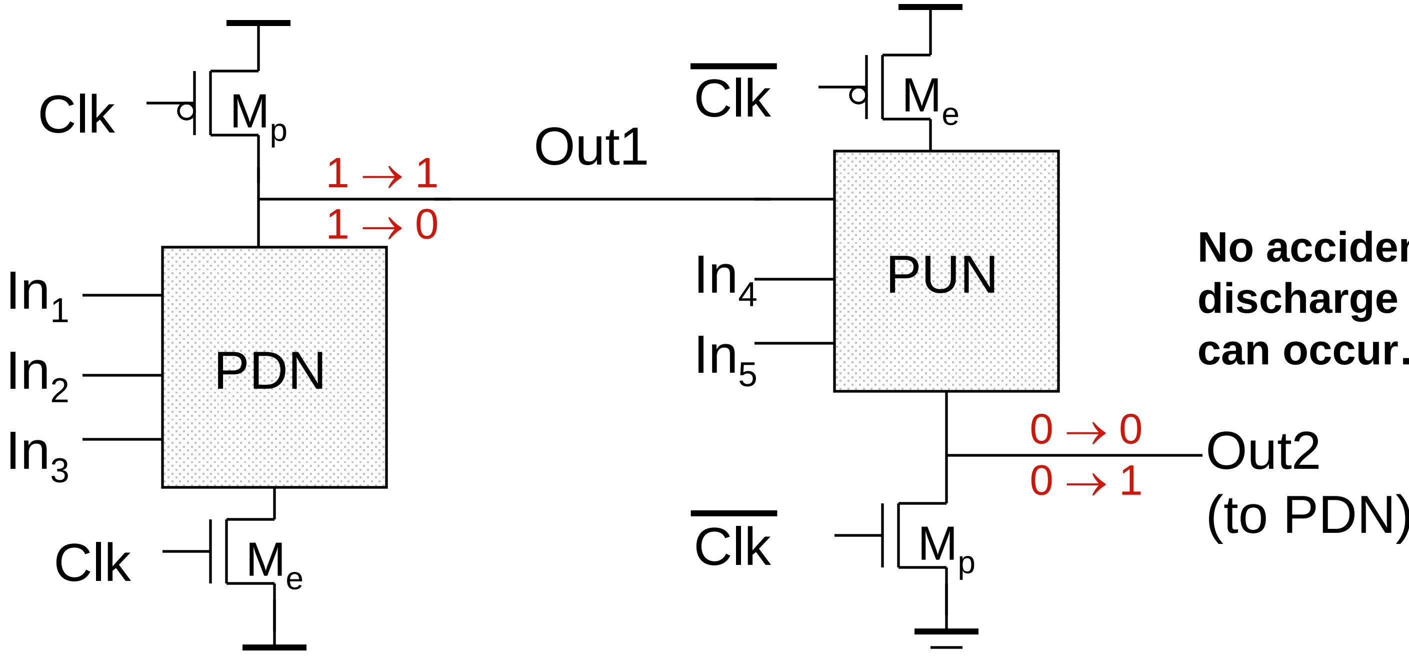
Possible to implement any arbitrary function….but comes at the expense of increased power since a transition is guaranteed every CLK cycle irrespective of the input values….either Out1 or Out2 must make a 0 to 1 transition.

np-CMOS

Alternative to cascading dynamic gates….uses n-type and p-type dynamic logic

Exploits duality between n-tree and p-tree logic gates to eliminate cascading problem

No extra inverter at the outputs….unless output of n-tree (p-tree) needs to be connected to another n-tree (p-tree) gates



No accidental discharge of Out2 can occur….

Only 0 → 1 transitions allowed at inputs of PDN
Only 1 → 0 transitions allowed at inputs of PUN

Drawback: p-tree gates are slower than the n-tree gates…needs proper skewing of PMOS….area penalty

No buffers---so dynamic nodes need to be routed between gates

A Novel Variation-Tolerant Keeper Architecture for High-Performance Low-Power Wide Fan-in Dynamic OR Gates

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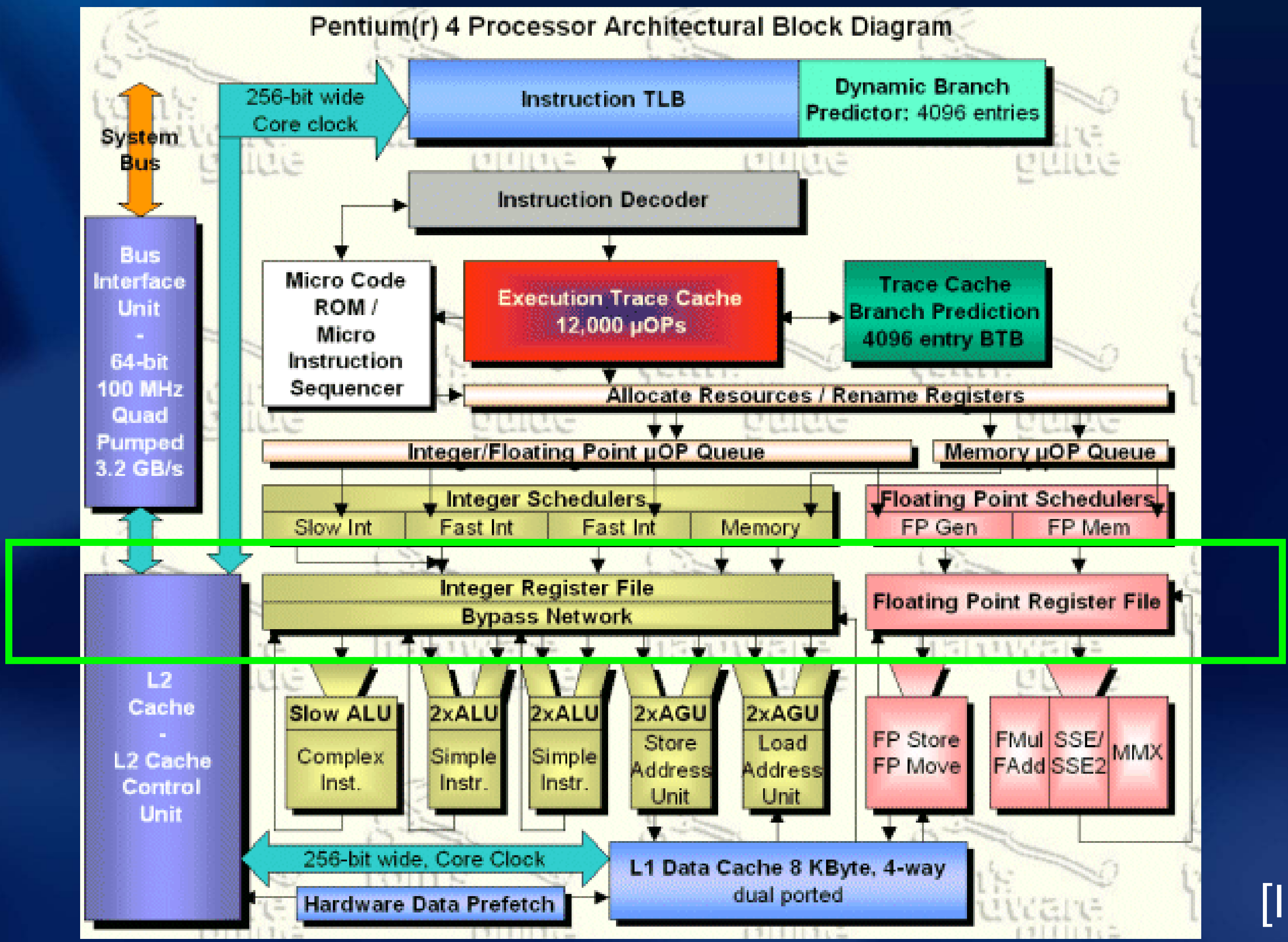
Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106

IEEE Transactions on VLSI, 2009 (to appear)

Preliminary Version Published in DAC 2006.

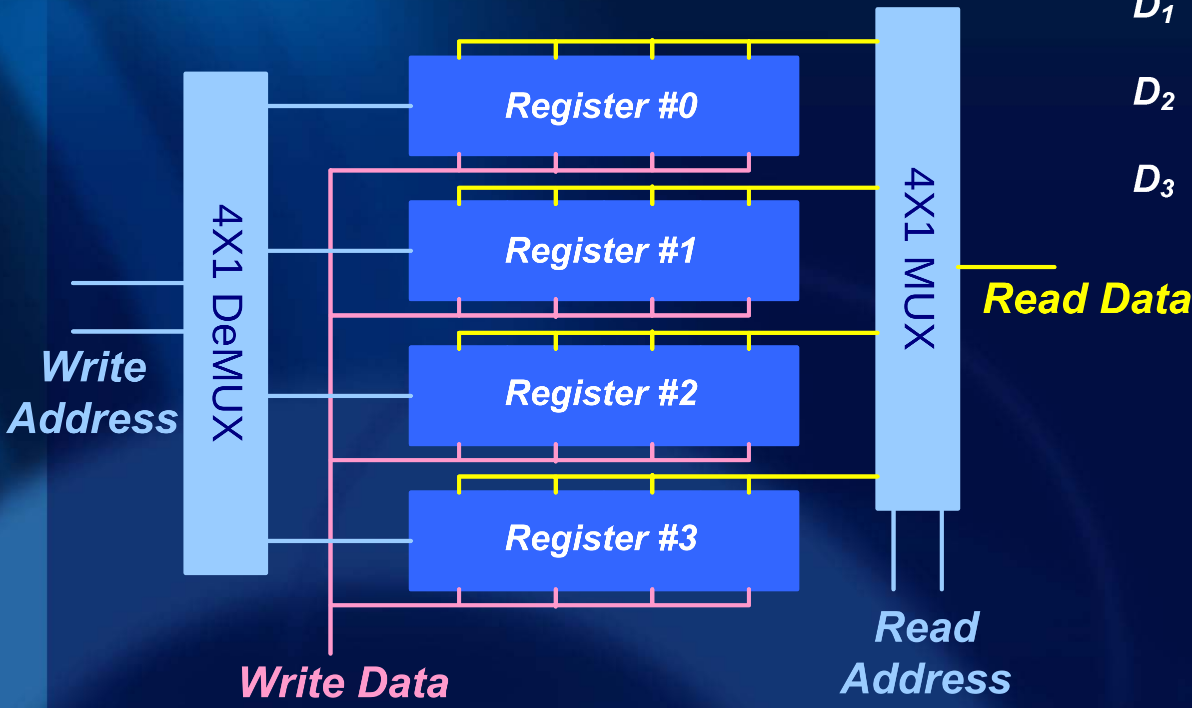
Motivation



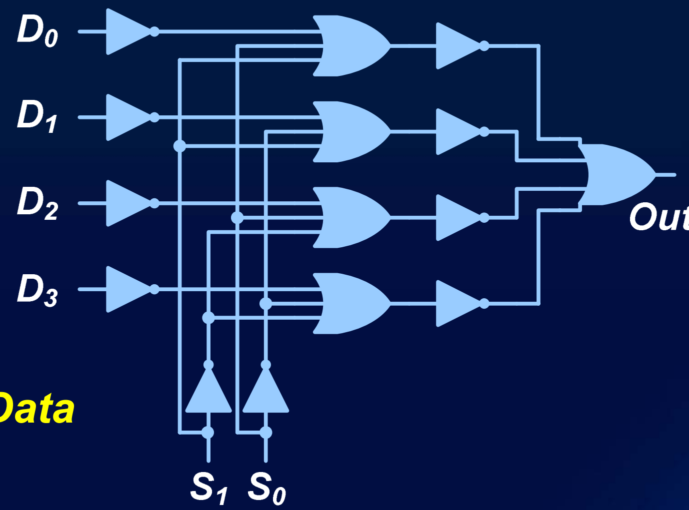
[Intel Inc.]

- **Register files are critical modules in computer architecture**

Motivation



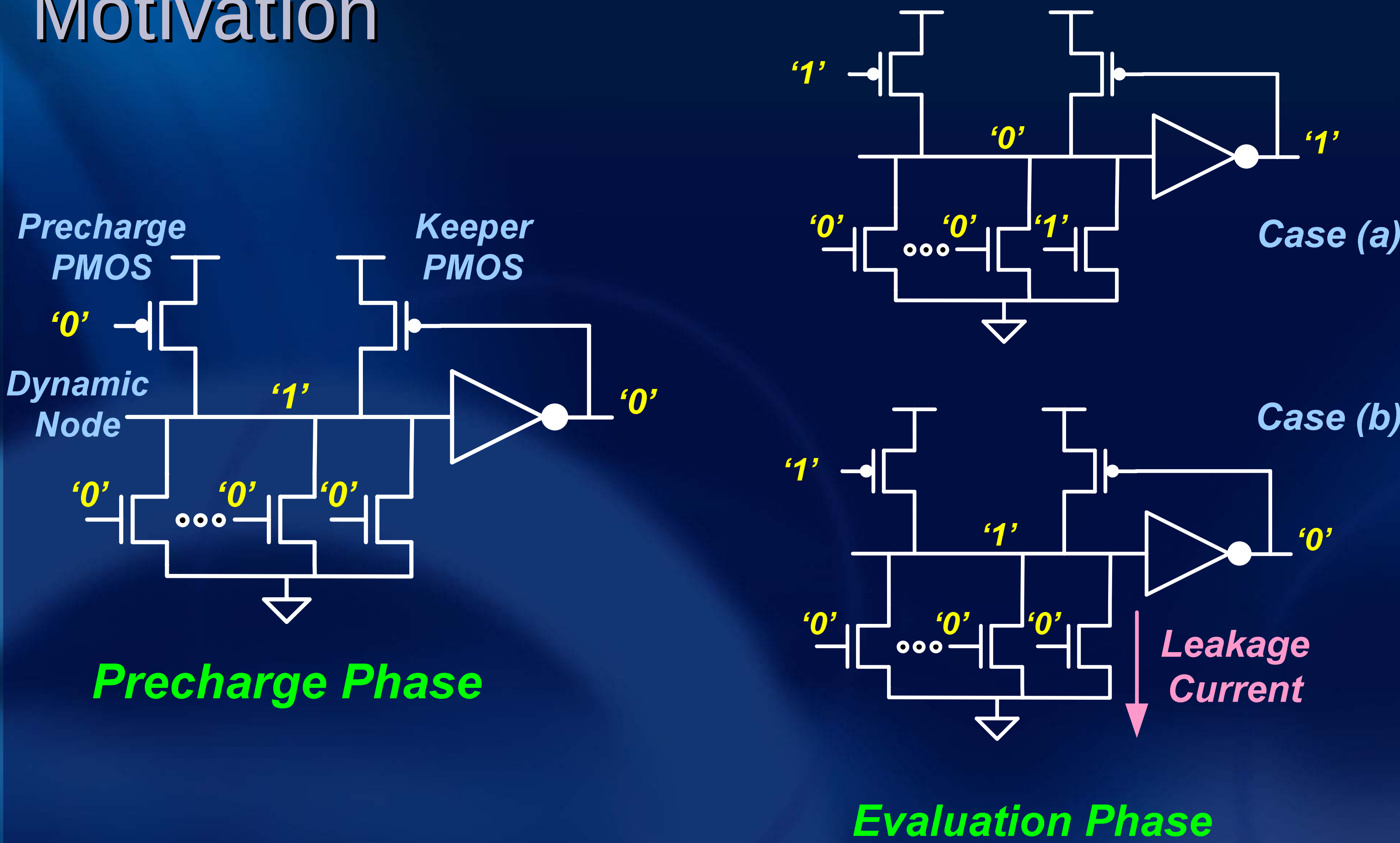
A Simple register File



4X1 MUX

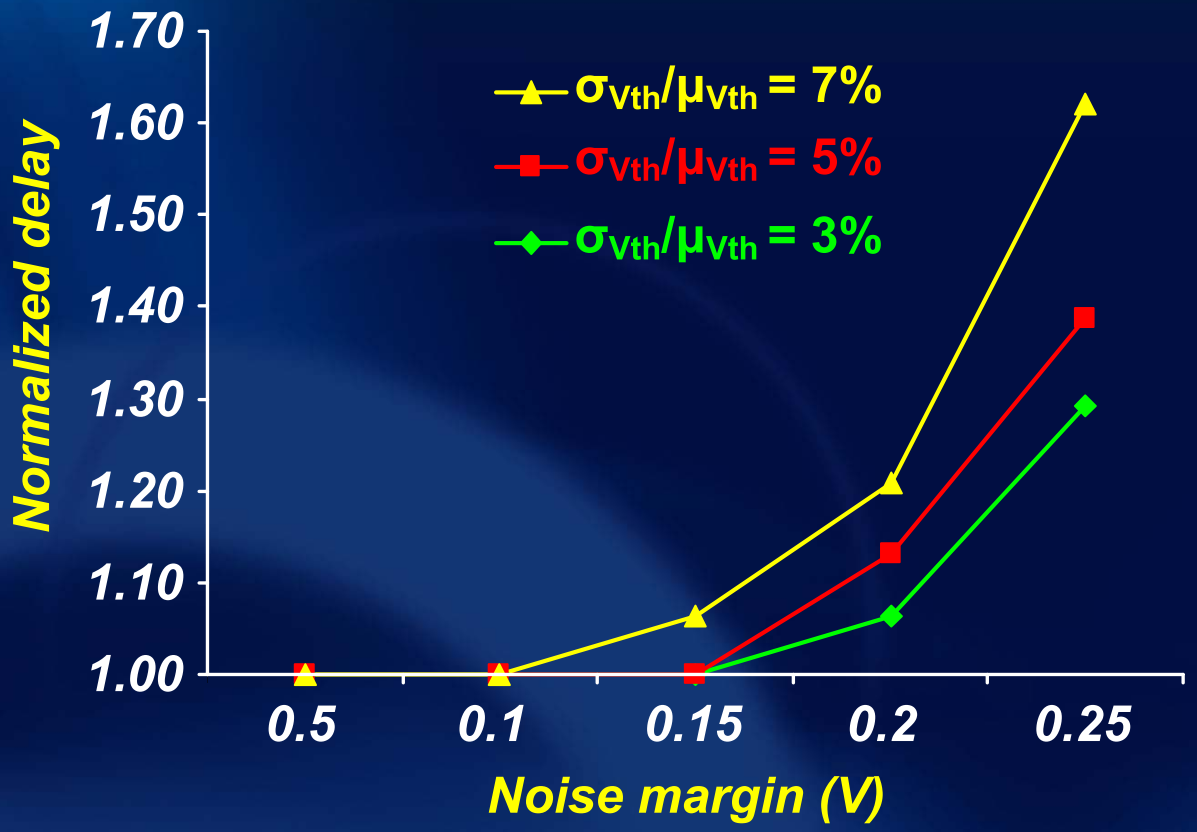
- **Dynamic gates are preferred gate style in high-performance designs.**
- **Address decoder and multiplexers are realized using dynamic OR gates.**

Motivation



- **Pre-charge and evaluation phases for dynamic gates**

Motivation

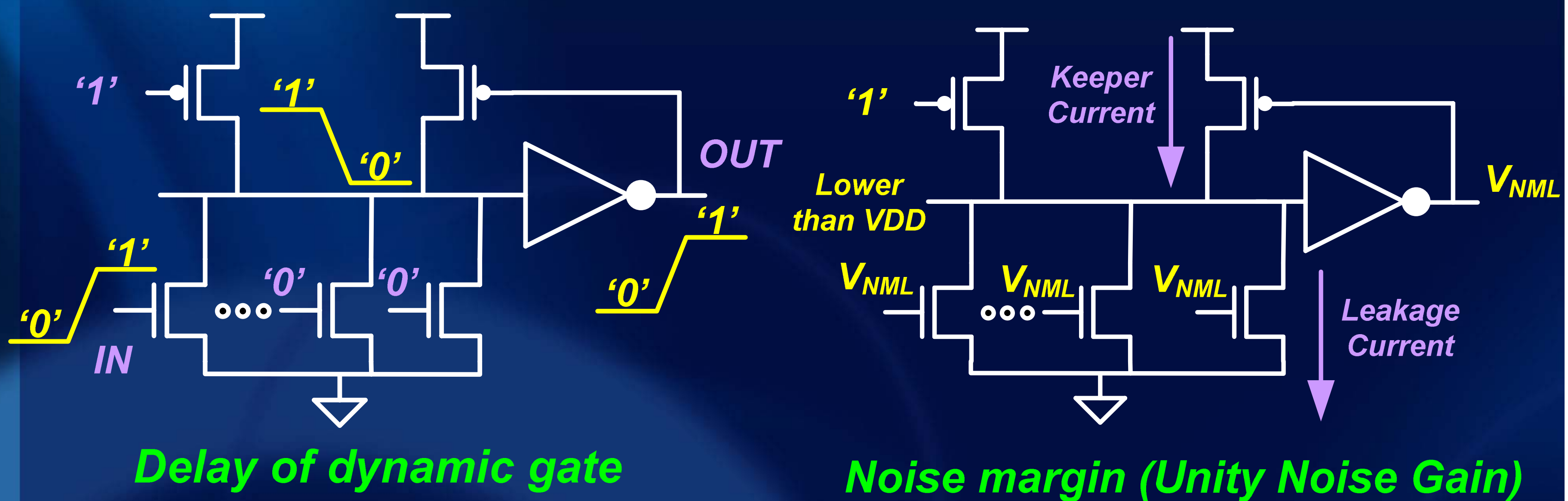


- **Trade-off between performance and robustness for traditional keeper.**

Outline

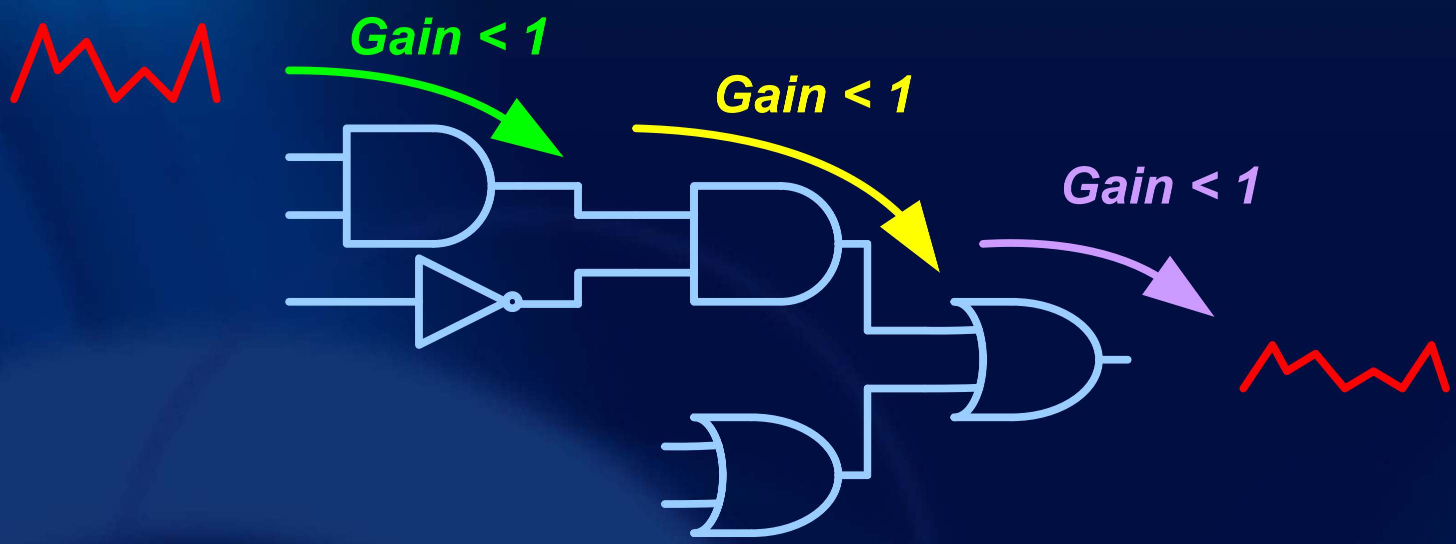
- **Introduction**
- **Keeper Sizing**
- **Proposed Keeper**
- **Simulation Results**
- **Conclusions**

Introduction



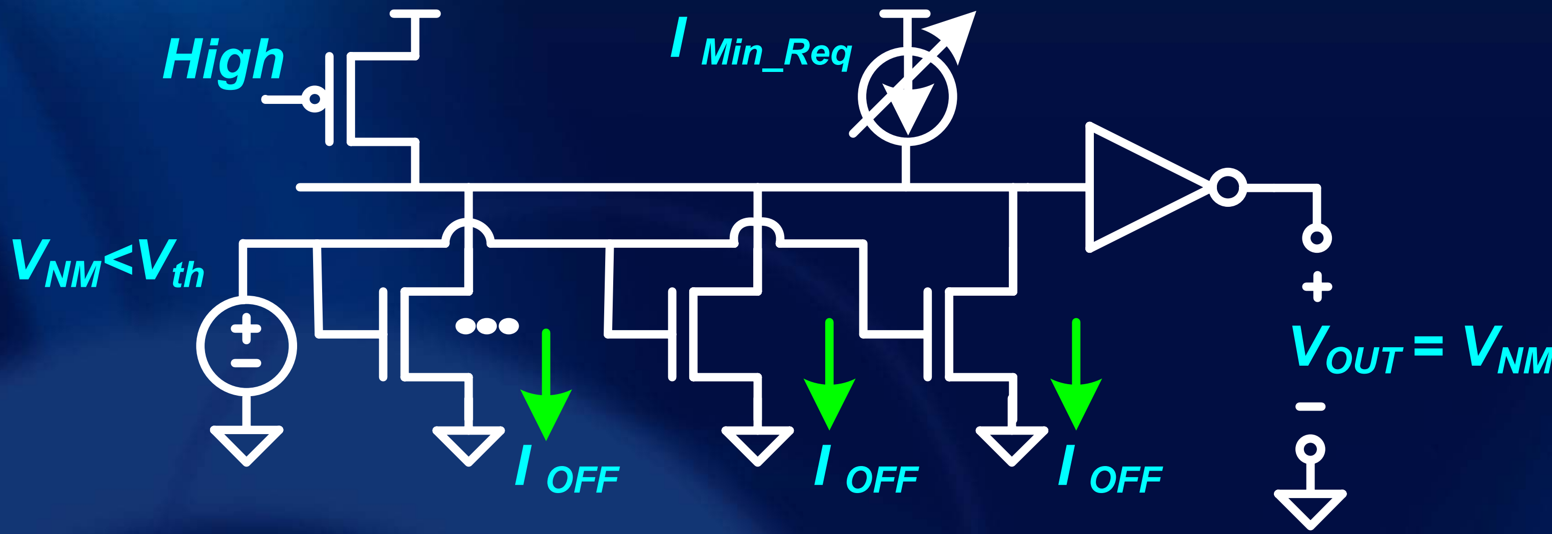
- **Worst case delay occurs when only one input switches**
- **Unity Noise Gain (UNG) is the voltage level that when applied to all inputs, results in same output voltage.**
- **Trade-off between performance and robustness.**

Introduction



- Noise margin definition is based on the fact that noise signal must not be amplified in a chain of logic gates.
- In this work we focus on correlated variation of threshold voltage.
- Impact of random variation can be considered by targeting a slightly higher noise margin.

Keeper Sizing

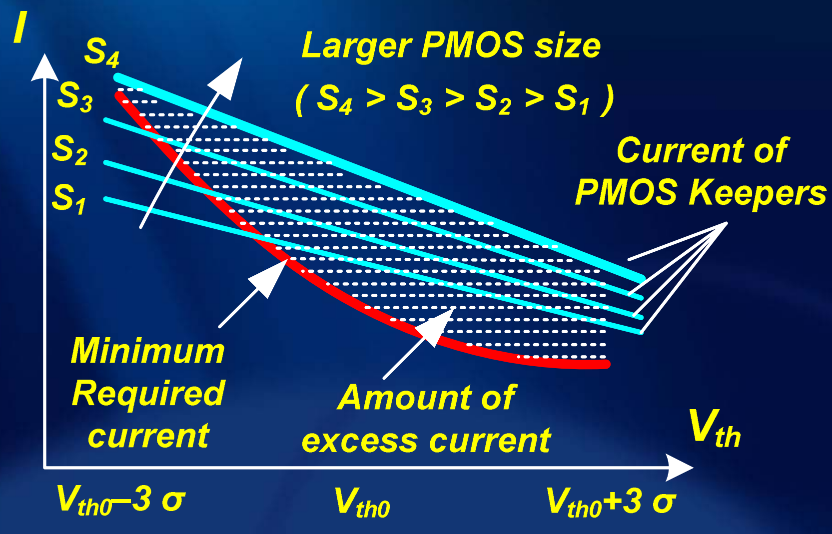


- ***Minimum required current (*** **ideal keeper):**

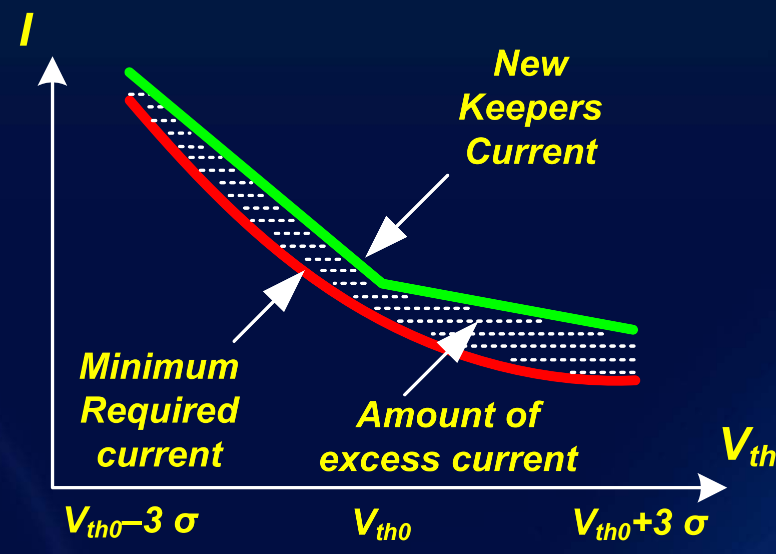
  smallest amount of current that must be injected to dynamic node to guarantee a particular level of UNG.

- **Minimum required current is a strong function of V_{th} variation of pull down network transistors.**

Keeper Sizing



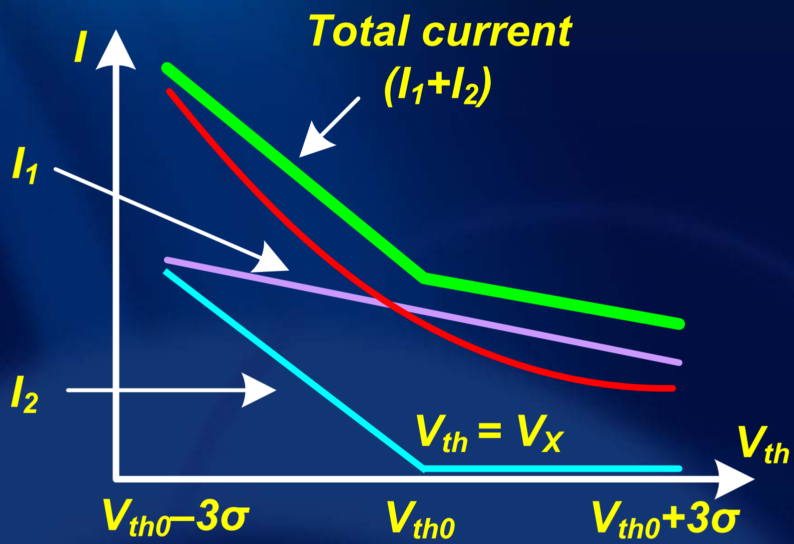
(a) Traditional keeper's behavior

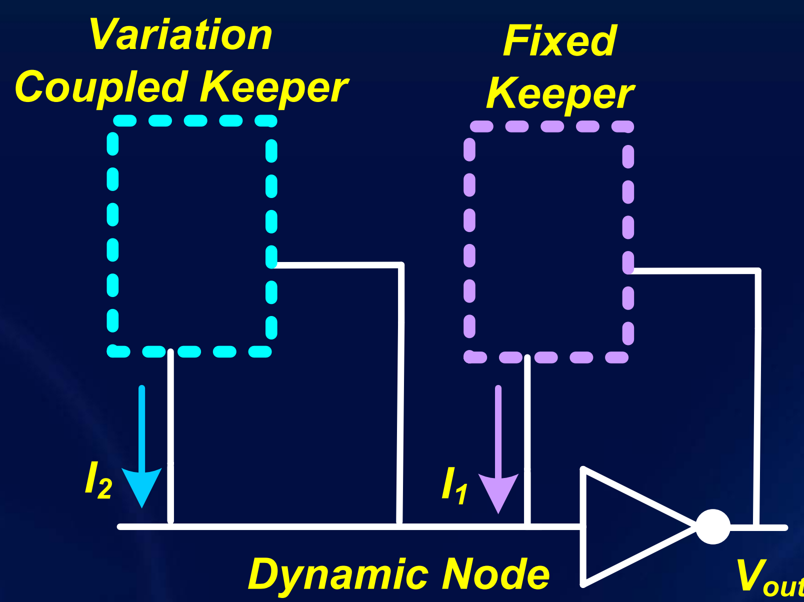


(b) Proposed keeper's behavior

- To maintain the minimum required current level over entire variation range, traditional PMOS keeper must be resized.
- At lower threshold voltage, top line (S_4) supplies enough current; however, at higher threshold voltage huge amount of excess current is injected to node.

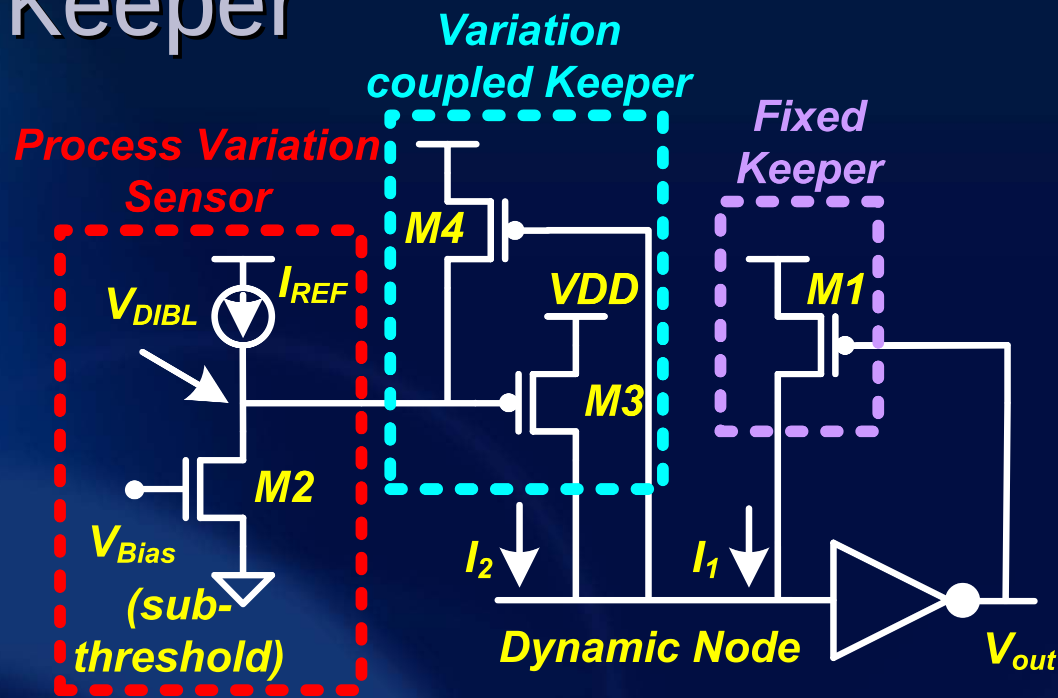
Proposed Keeper





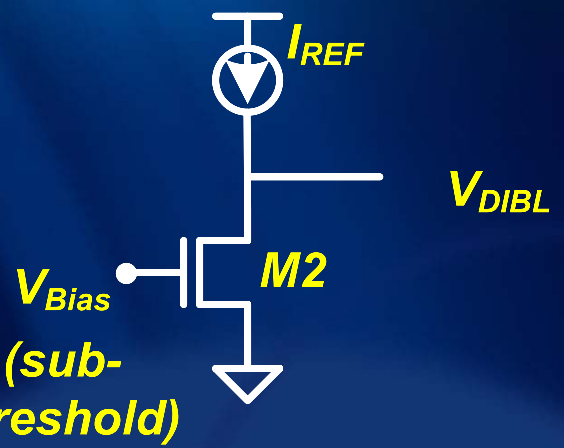
- New keeper is composed of two circuits.
- First one is a small fixed-size PMOS keeper.
- Second one is a variation-coupled keeper.
- Total current shows much better behavior compared to traditional PMOS keepers.

Proposed Keeper



- Beside two keepers, there is a process variation sensor.
- On lower V_{th} side, variation sensor provides higher V_{DIBL} voltage and hence, M_3 supplies less current. On higher V_{th} side vice versa.
- M4 is used to turn off M3 keeper when dynamic node needs to be pulled down.

Proposed Keeper



Process Variation Sensor
(Kuroda et al. ISSCC 1996)

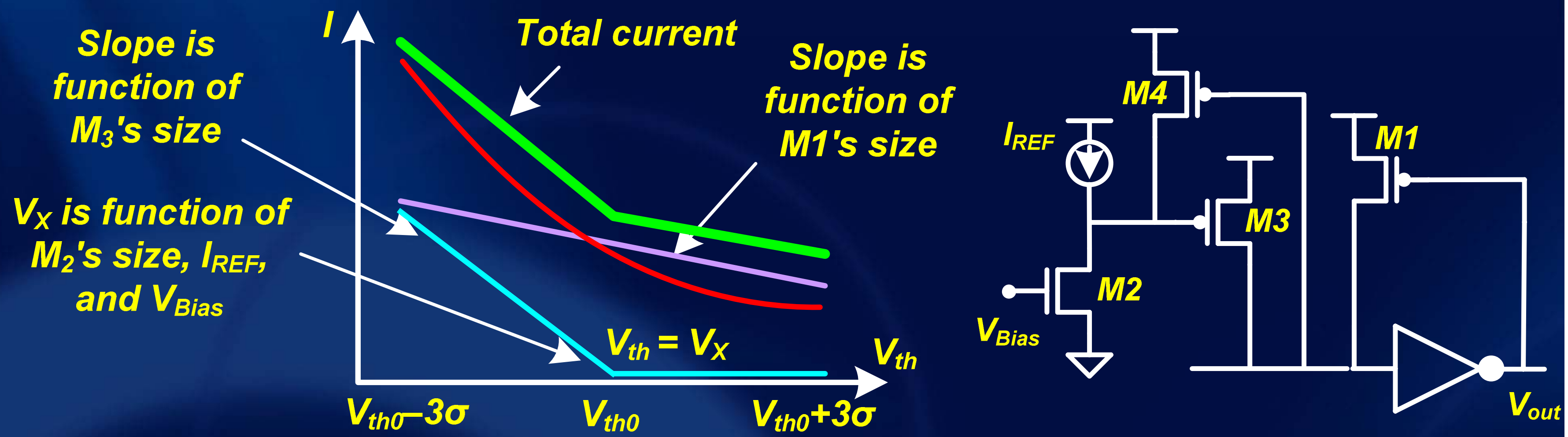
(a) $$I_{REF} = \mu_n C_{ox} \frac{W}{L} V_T^{\,2}\, e^{\frac{V_{Bias} - (V_{th} - \eta V_{DIBL})}{n V_T}}$$

(b) I_{REF} and V_{Bias} are function of nV_T.

(c) $$V_{th} - \eta V_{DIBL} = cons.$$

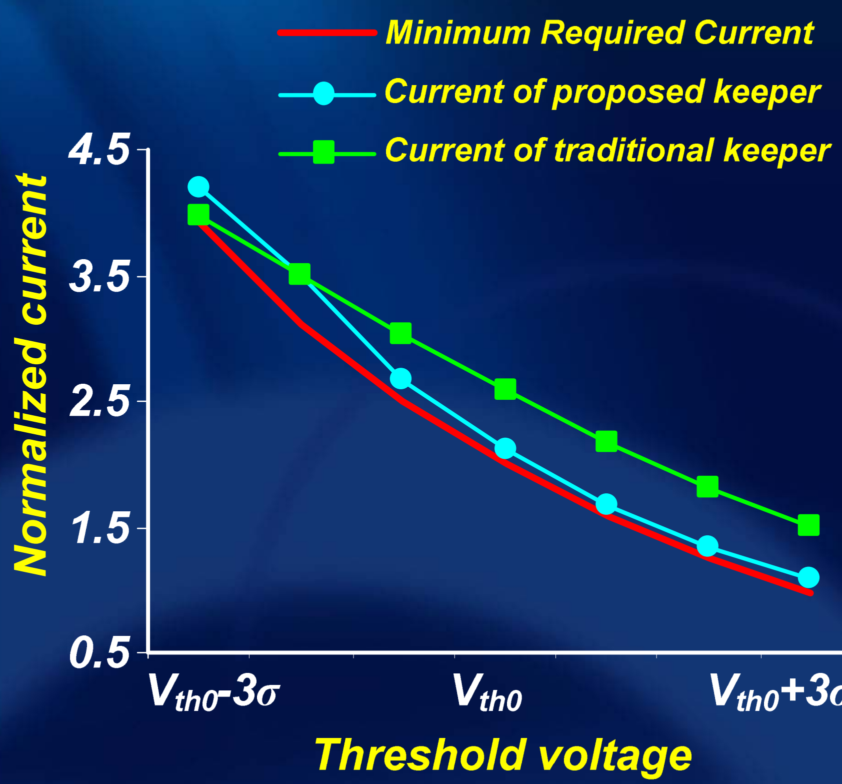
- I_{REF} and V_{Bias} are designed to be independent of V_{th} and it's variations.
- M_2 is biased to operate in sub-threshold region.
- Small variation in V_{th} of M_2 causes η time wider fluctuation on V_{DIBL}. (η is DIBL constant).

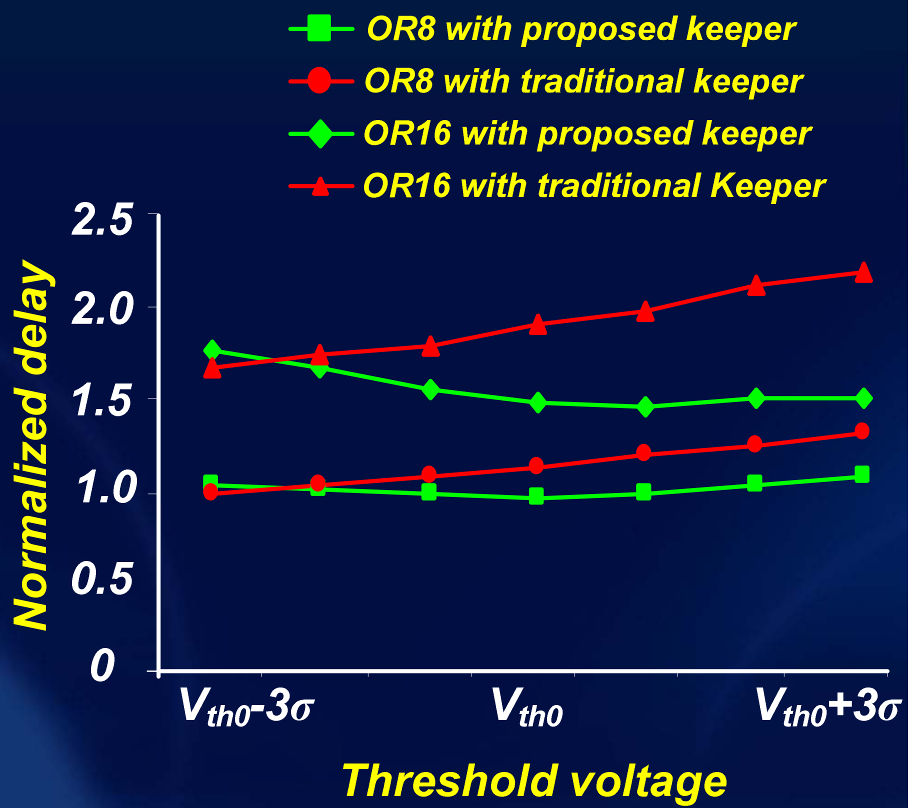
Proposed Keeper



- **Through analytical equations, circuit parameter affecting keeper current curves have been studied.**
- **It is shown that each circuit parameter affects a separate part of curves which gives more flexibility in adjusting current curves to get best possible results.**

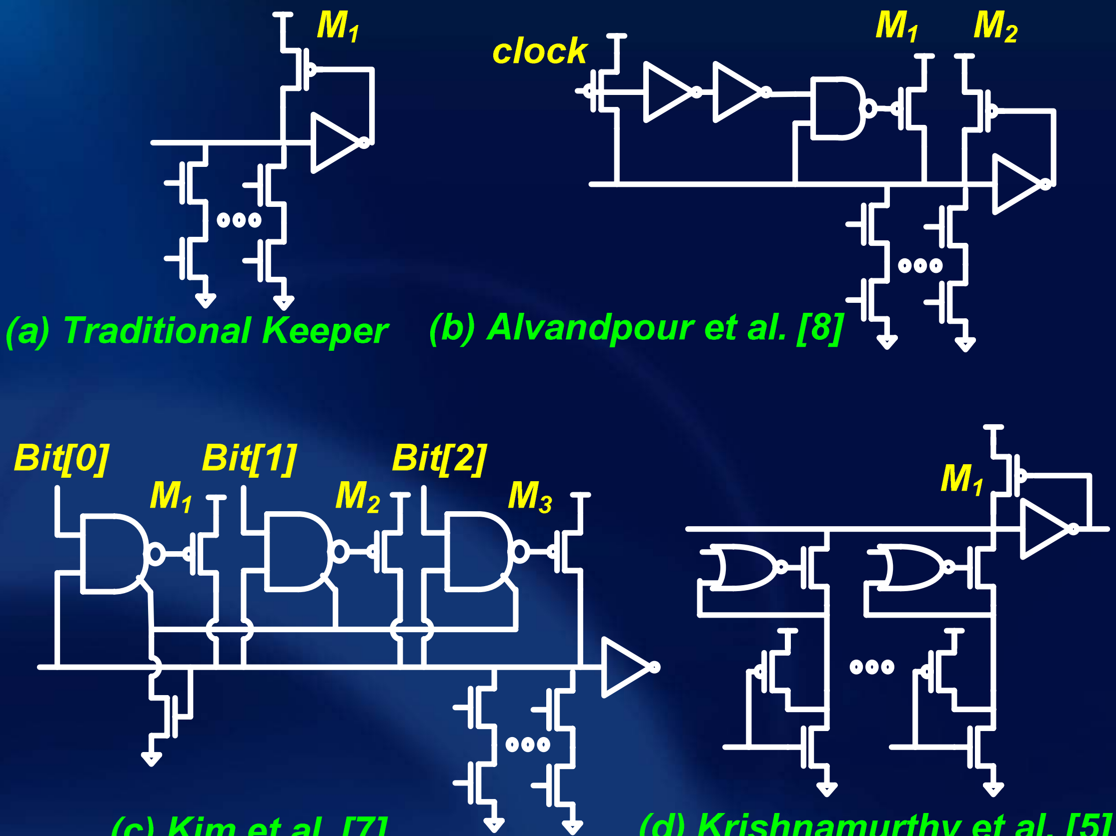
Simulation Results





- Normalized current supplied by traditional and proposed keeper vs minimum required current. (left)
- Normalized delay of 8- and 16-input OR gates with traditional and proposed keeper. (right)

Simulation Results

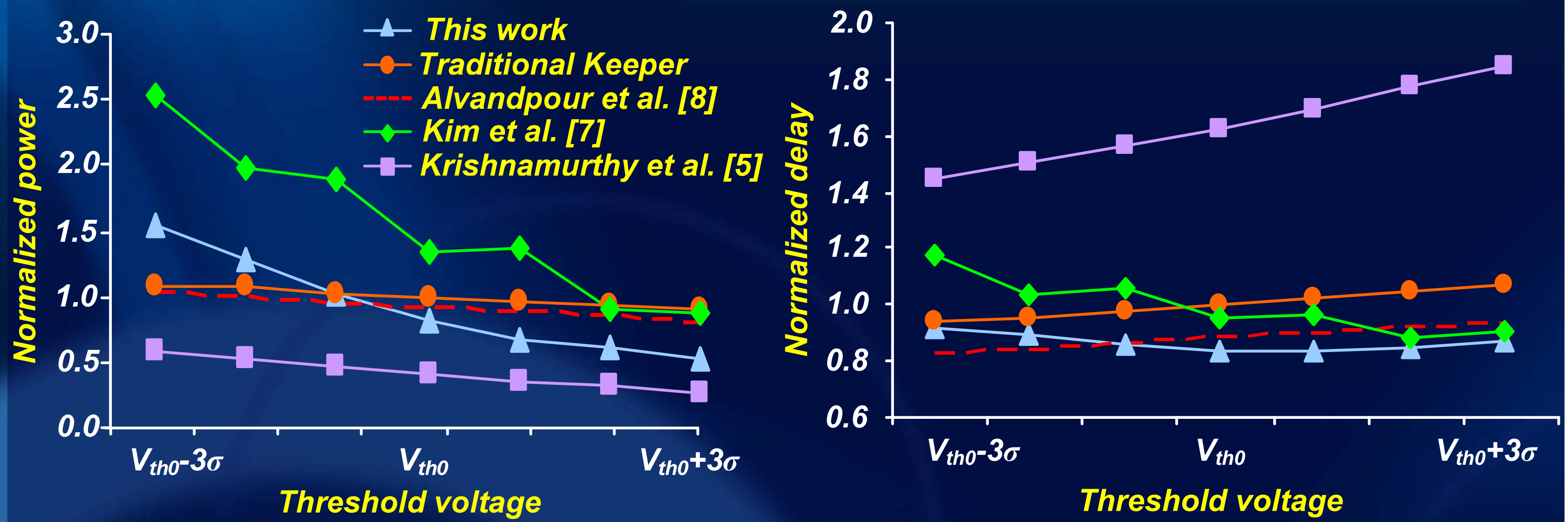


(a) Traditional Keeper (b) Alvandpour et al. [8]

(c) Kim et al. [7] (d) Krishnamurthy et al. [5]

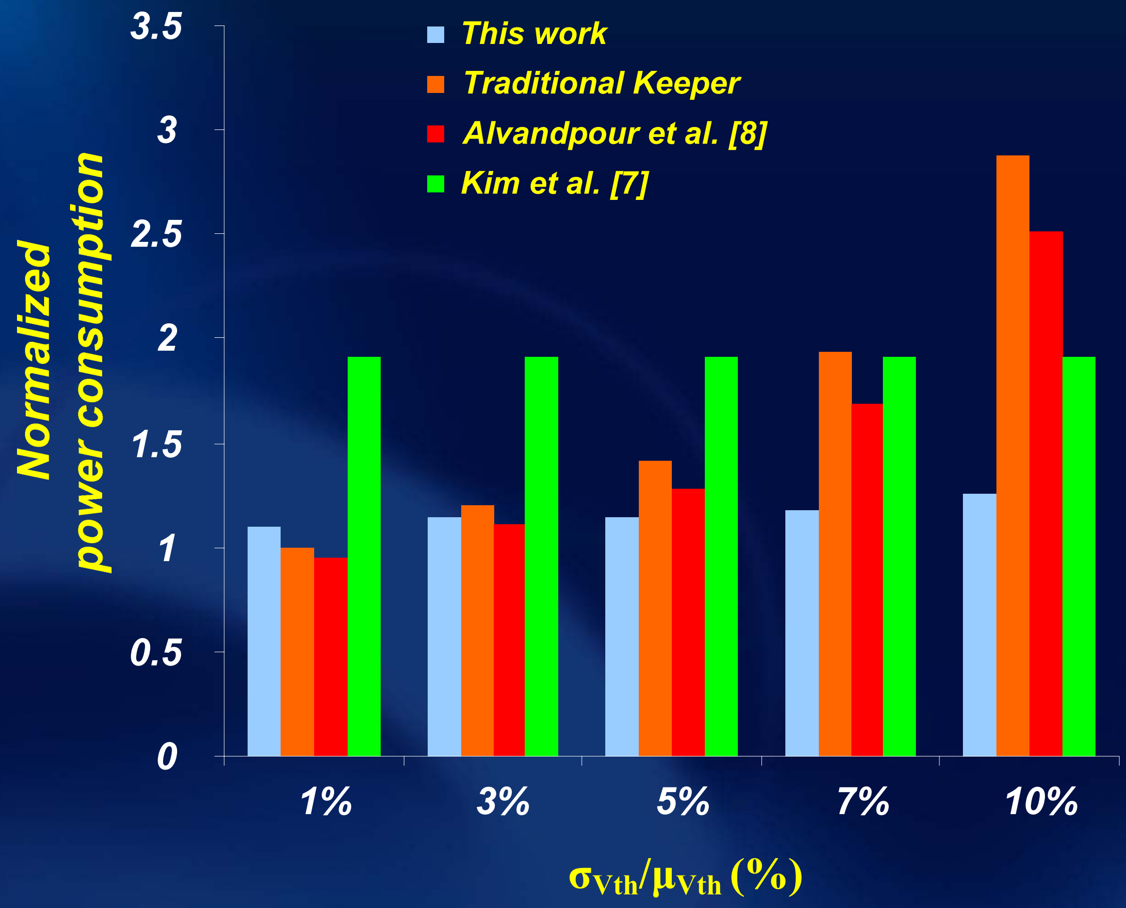
- **Proposed keeper has been compared to previous work.**
- **Mean delay value, power consumption and standard deviation of delay are used as metrics.**

Simulation Results



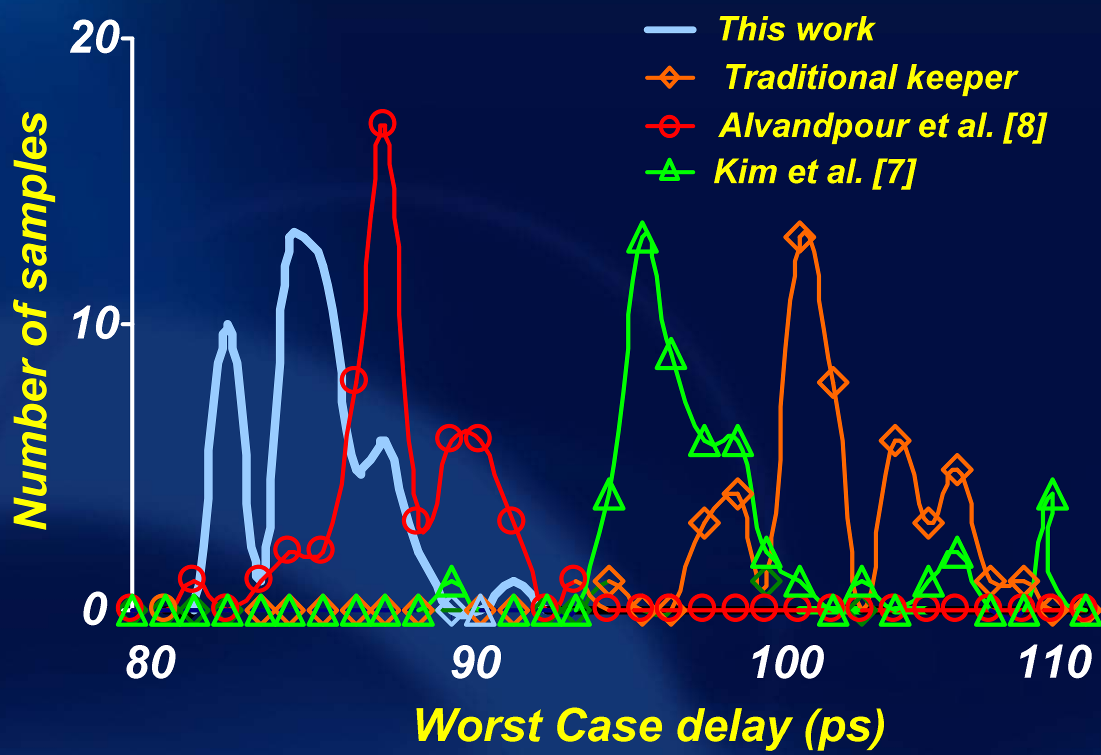
- **Comparison between normalized mean delay (left) and power consumption (right) of OR gates realized by different keepers.**
- **Proposed keeper shows low delay and power consumption.**

Simulation Results



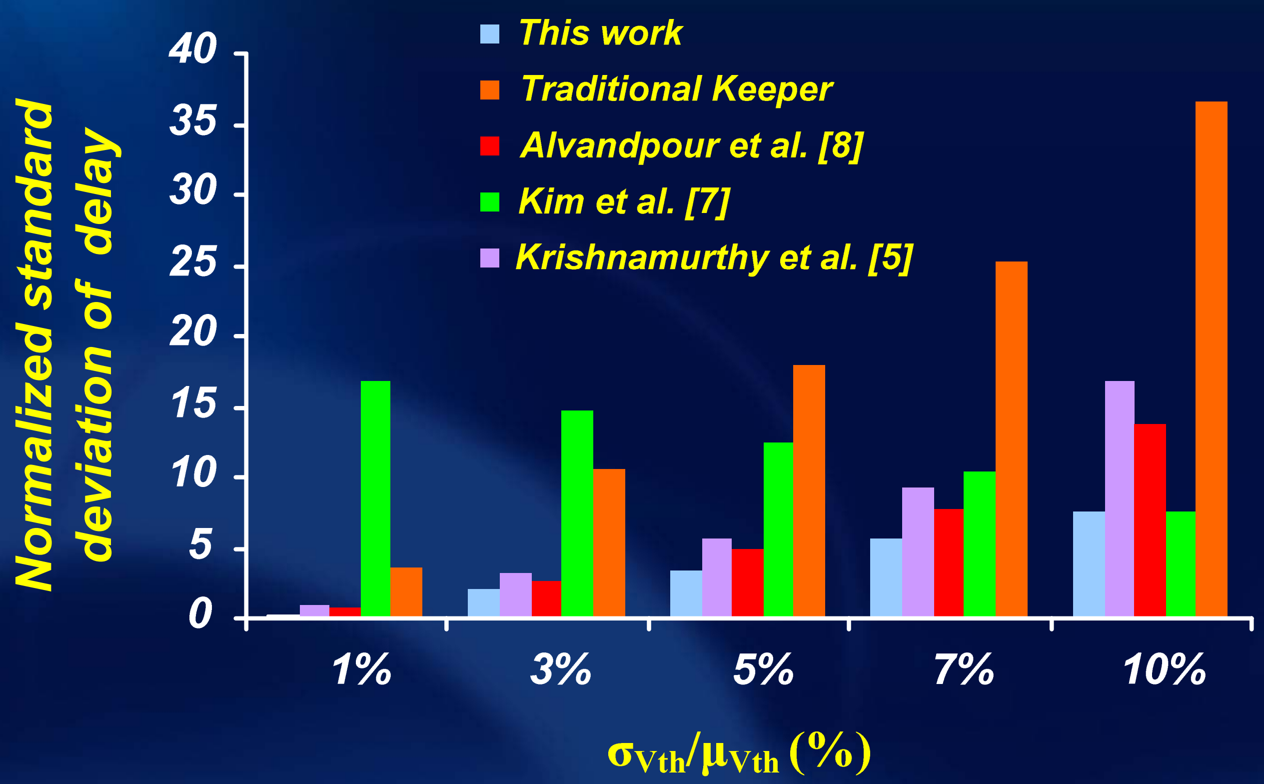
- Normalized power consumption for different keepers at different levels of process variation (σ_{Vth}/μ_{Vth}).

Simulation Results



- Delay distribution of dynamic OR gates with different keeper circuits obtained for 100 samples.
- Distribution corresponded to proposed keeper shows lower mean and narrower spread.

Simulation Results



- **Normalized STD of delay for different keepers at different levels of process variation (σ_{Vth}/μ_{Vth}).**
- **Proposed keeper shows superior behavior in terms of robustness to increasing level of variation.**

Conclusions

- A novel approach for designing low-power variation-aware keeper circuits of wide fan-in dynamic gates has been presented.
- HSPICE simulation results show that the proposed architecture offers smallest delay deviation for entire *Vth* range compared to all existing works in the literature.
- The proposed keeper architecture could be very effective in increasing the robustness of dynamic gates to process variation.