A Transmission Line Model for Silicided Diffusions: Impact on the Performance of VLSI Circuits

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Abstract—In scaled technologies, performance improvements become increasingly limited by interconnect parasitics. The increased emphasis in the literature on low-resistance replacements for, or supplements to, polysilicon-gate technologies verifies the importance of parasitic limitations. Further, the role of the series source and drain resistance as well as contact resistance in limiting device performance has also been addressed by several authors. This role is further enhanced by the actual much more rapid increase in sheet resistivity with decreasing junction depth than previously assumed by other workers. In fact, it can be anticipated that metallurgical advances, such as silicides, will be required to compensate for the increased sheet resistance of source and drain diffusions.

In the present work, a theoretical development of a transmission line model for a totally silicided diffusion is presented. Both the silicide and the diffusion sheet resistivities ρ_S and ρ_D, and the specific contact resistivity ρ_C, are incorporated, unlike earlier models for contact holes only in which $\rho_S = 0$. This model is applied to specific typical MOS structures, including single-section and three-section structures, to calculate the contact resistance contribution to total resistance. These results are used in conjunction with device equations addressing the device and circuit performance of small-geometry MOSFET's. Both n- and p-channel devices are considered as well as various scaling scenarios (constant field, constant voltage, etc.). These results show that for n-channel devices with a gate length of 1 μm, a-factor-of-two increase in circuit performance can be expected when using silicides. However, for p-channel devices, the expected performance gain as a result of using silicides is a factor of ten.

I. Introduction

THE ROLE of parasitic interconnect resistance in integrated circuit MOS technology has received increasing emphasis in the literature, as the performance improvements in scaled technologies become increasingly limited by interconnect parasitics. The profusion of literature in recent years on low-resistance replacements for, or supplements to, polysilicon-gate technologies, including "polycides" [1], [3], refractory metals [2], and silicides [4] verifies the importance of this limitation. Recently, the role of series source/drain and contact resistance in limiting device performance has also received attention [5]-[7]. This limitation is further aggravated by the much stronger dependence of diffused junction sheet resistance on junction depth (as discussed later) than assumed in classical scaling [8]. Besides self-aligned shallow/deep junction techniques [9]-[11], it can be anticipated that metallurgical advances, such as silicides, will be required to overcome the limitations of scaled, implanted, and diffused source-drain junctions.

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While the behavior of silicided conductors has received considerable experimental attention, both from a materials science and a technology point of view in recent literature, no theoretical modeling of such structures has appeared. Using extensions of transmission line models, which have been applied previously to metal or metal-silicide contacts only [12]-[14], the electrical behavior of totally silicided conductors is developed in this paper. While illustrative examples are given for silicided diffusions, the theoretical development is general, and is applicable to silicided, doped polysilicon as well.

The general transmission line model for silicided conductors is developed in Section II, followed by applications to specific typical structures in Section III. Section IV utilizes these results to examine the consequences of silicided diffusion in scaled MOS technologies.

II. Derivation of Transmission Line Model

The diffusion and silicide layer shown in Fig. 1(a), are approximated by the transmission line model illustrated in Fig. 1(b). Although a similar treatment has been previously reported [12], [14], the structures considered in the present work require an analysis of a more general nature. As stated by Berger [14], the use of a transmission line model requires the following assumptions:

1) the current through the interface between the two layers is vertical,
2) the thickness of the silicide and diffusion layers are both infinitesimally small,
3) the contact is ohmic.

Unlike the previous work [12]-[14] in which the metal in the contact hole shorts out one side of the transmission line, the order-of-magnitude larger resistivity of silicides requires that the sheet resistance of the silicide be included as part of the overall resistance of the various structures considered.

The current in the diffusion shown in Fig. 1 can be expressed as

$$I_D = -\frac{W}{\rho_D}\frac{dV_D}{dx} \tag{1}$$

where $\rho_D[\Omega/\square]$ is the sheet resistivity of the diffusion and W [μm] is the diffusion width. Similarly, the current in the silicide is given as

$$I_S = -\frac{W}{\rho_S}\frac{dV_S}{dx}. \tag{2}$$

Further, the current through an element $W\,dx$ of the silicide-

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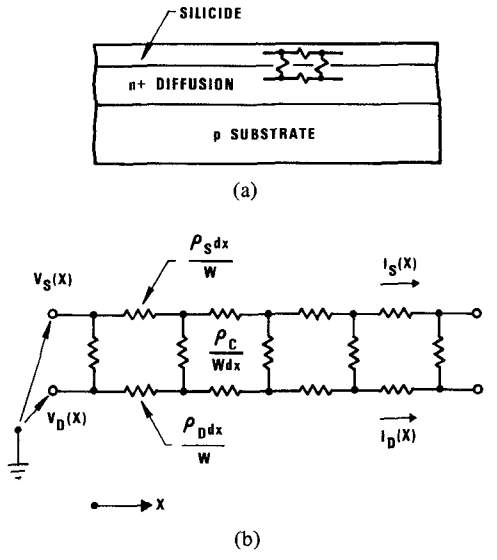

Fig. 1. Illustration showing (a) a cross section of a silicided n^+ diffusion; and (b) the transmission line model for a silicided n^+ diffusion.

diffusion interface (upwards in Fig. 1(b)) is given by Kirchoff's Law as

$$dI_S = \frac{W\,dx}{\rho_c}(V_D - V_S) \tag{3}$$

where $\rho_c[\Omega \cdot \mu m^2]$ is the specific contact resistivity between the two layers. Using (3) the relation between the currents in the two layers is given as

$$\frac{dI_D}{dx} = -\frac{dI_S}{dx} = -\frac{W}{\rho_c}(V_D - V_S). \tag{4}$$

From (1), (2), and (4), the potential distribution within the two resistive layers can be described by the following pair of coupled differential equations:

$$\frac{d^2V_D}{dx^2} - \frac{\rho_D}{\rho_c}(V_D - V_S) = 0 \tag{5a}$$

$$\frac{d^2V_S}{dx^2} + \frac{\rho_S}{\rho_c}(V_D - V_S) = 0. \tag{5b}$$

The solution of this pair of differential equations is given by

$$V_D(x) = \frac{\rho_D}{\rho_D + \rho_S}[Ae^{\beta x} + Be^{-\beta x}] + Dx + C \tag{6a}$$

$$V_S(x) = \frac{-\rho_S}{\rho_D + \rho_S}[Ae^{\beta x} + Be^{-\beta x}] + Dx + C \tag{6b}$$

where $\beta = ((\rho_D + \rho_S)/\rho_c)^{1/2}$. The associated current equations are

$$I_D(x) = -\frac{W}{\rho_D}\left[\frac{\beta\rho_D}{\rho_D + \rho_S}(Ae^{\beta x} - Be^{-\beta x}) + D\right] \tag{6c}$$

$$I_S(x) = -\frac{W}{\rho_S}\left[-\frac{\beta\rho_S}{\rho_D + \rho_S}(Ae^{\beta x} - Be^{-\beta x}) + D\right]. \tag{6d}$$

The constants A, B, C, and D are determined by the boundary conditions appropriate for the particular geometry considered.

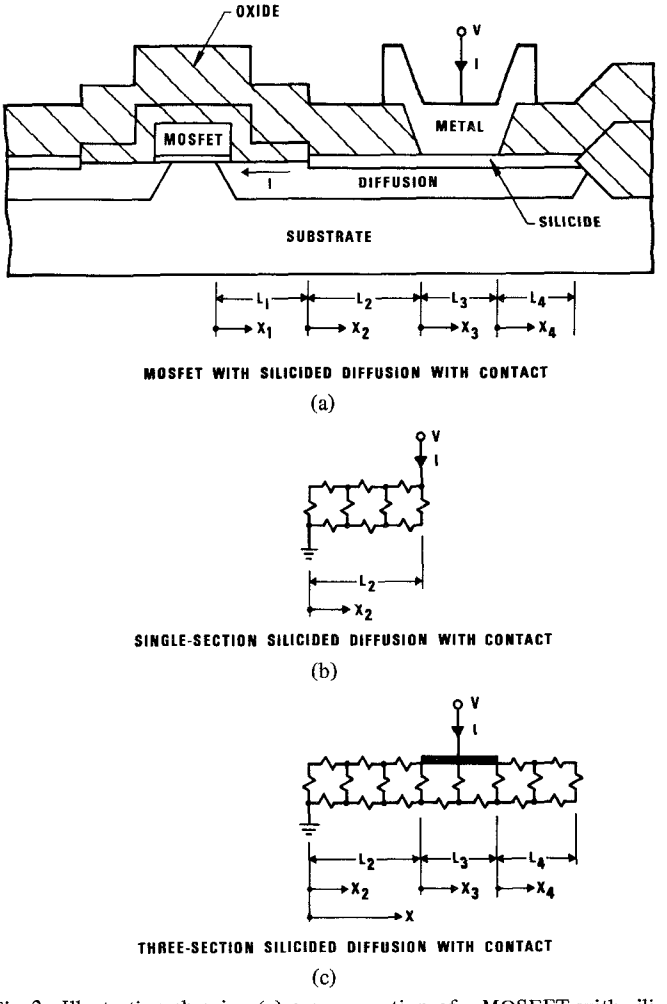

Fig. 2. Illustration showing (a) a cross section of a MOSFET with silicided diffusion interconnect and contact hole; (b) a simplified model of regions 2, 3, and 4 in which the impedance of sections 3 and 4 is assumed large; and (c) a rigorous coupled transmission line treatment of sections 2, 3, and 4.

In the limit that ρ_S goes to zero, e.g., when the silicide is shorted by metal in a contact hole, (6a) and (6b) reduce to the degenerate case analyzed previously [12], [14]. The voltage as a function of position in this case is now given by

$$V_D(x) = Ae^{\alpha x} + Be^{-\alpha x} + V_S \tag{7a}$$

where V_S is the constant voltage on the metal-shorted silicide, and the associated current is given by

$$I_D(x) = -\frac{\alpha W}{\rho_D}[Ae^{\alpha x} - Be^{-\alpha x}] \tag{7b}$$

where $\alpha = (\rho_D/\rho_c)^{1/2}$.

III. Application to Specific Structures

A. Analysis of a Single-Section Silicided Diffusion with Contact

The use of a silicide over a diffused junction to decrease the series resistance to a transistor is shown in Fig. 2. As shown, the series resistance components can be divided into four regions. However, in this particular section, the discussion has been limited to a simple analysis, and thus the model indicated by Fig. 2(b) will be considered first. The following analysis,

therefore, is considered in the limit that

$$L_2 \gg L_3 \quad \text{and} \quad L_2 \gg L_4. \tag{8}$$

The four required boundary conditions to determine the current-voltage relations are given as

1) At $x_2 = 0$, $V_D(0) = 0$.
2) At $x_2 = L_2$, $V_S(L_2) = V$, where the contact is made.
3) At $x_2 = 0$, the current in the silicide is zero and thus

$$\left.\frac{dV_S}{dx}\right|_{x_2=0} = 0.$$

4) At $x_2 = L_2$, the current in the diffusion is zero and thus

$$\left.\frac{dV_D}{dx}\right|_{x_2=L_2} = 0.$$

The application of the above listed boundary conditions yields the following solution for $V_S(x)$ and $V_D(x)$:

$$V_S(x_2) = \frac{V}{F_1}[\rho_S^2 \cosh \beta x_2 + \rho_S\rho_D \cdot \cosh \beta(L_2 - x_2) + \rho_S\rho_D\, \beta x_2 \sinh \beta L_2] + \frac{V}{F_1}[\rho_S\rho_D + \rho_D^2 \cosh \beta L_2] \tag{9}$$

and

$$V_D(x_2) = -\frac{V}{F_1}[\rho_S\rho_D \cosh \beta x_2 + \rho_D^2 \cdot \cosh \beta(L_2 - x_2) - \rho_S\rho_D\, \beta x_2 \sinh \beta L_2] + \frac{V}{F_1}[\rho_S\rho_D + \rho_D^2) \cosh \beta L_2] \tag{10}$$

where

$$F_1 = 2\rho_S\rho_D + (\rho_D^2 + \rho_S^2) \cosh \beta L_2 + \rho_S\rho_D\, \beta L_2 \sinh \beta L_2.$$

The total current through the structure of Fig. 2(b) is given by the sum of the currents in the two layers. Thus

$$I = I_S + I_D = -\frac{W}{\rho_D}\frac{dV_D}{dx_2} - \frac{W}{\rho_S}\frac{dV_S}{dx_2} \tag{11}$$

where W is the diffusion width. Using (9)-(11), the total resistance of the structure defined by Fig. 2(b) is given as

$$R_T = \frac{L_2}{W}\frac{\rho_D\rho_S}{\rho_D + \rho_S} + \frac{2\rho_S\rho_D + (\rho_S^2 + \rho_D^2)\cosh \beta L_2}{W\beta(\rho_S + \rho_D)\sinh \beta L_2} \tag{12}$$

where the first term is identified as the geometrical line resistance, and the second term is identified as the contact resistance R_C.

In Fig. 3, the resistance of the structure of Fig. 2(b) has been calculated as a function of L_2 using various values of ρ_c, the specific contact resistivity. Values of $\rho_D = 100\ \Omega/\square$ and $\rho_S = 10\ \Omega/\square$ were used for the respective sheet resistances. As can be seen by observing Fig. 3, the resistance of the structure increases abruptly as L_2 becomes small. In general, the value of L_2 at which the resistance increases abruptly is given by

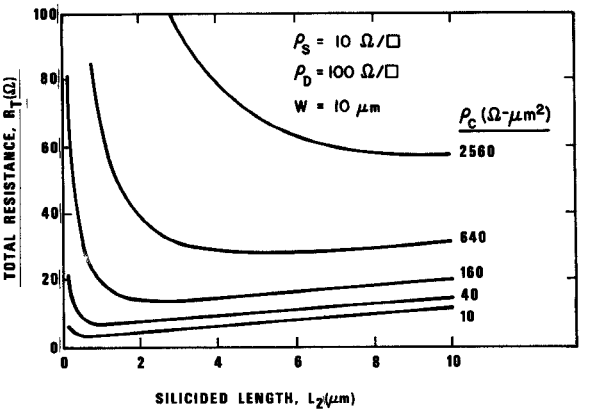

Fig. 3. Total resistance of the single-section silicide diffusion with contact of Fig. 2(b) versus silicided length L_2 for different specific contact resistivities ρ_c.

$$L_C = \frac{1}{\beta} = \left(\frac{\rho_c}{\rho_D + \rho_S}\right)^{1/2}. \tag{13}$$

In Fig. 3, this value of L_C varies from 0.3 to 4.8 μm as ρ_c varies from 10 to 2560 $\Omega \cdot \mu m^2$.

Equation (13) can be used to define the two limiting cases of resistance. For $L_2 \ll L_C$, (12) reduces to

$$R_T\Big|_{L_2 \ll L_C} = \frac{\rho_c}{L_2 W} + \frac{L_2}{W}\frac{\rho_D\rho_S}{\rho_D + \rho_S}. \tag{14}$$

In this limit, the contact resistance is area dependent, and the resistance of the structure increases as L_2 decreases. In the other limit that $L_2 \gg L_C$, (12) reduces to

$$R_T\Big|_{L_2 \gg L_C} = \frac{1}{W}\frac{(\rho_S^2 + \rho_D^2)}{(\rho_S + \rho_D)^{3/2}}\rho_c^{1/2} + \frac{L_2}{W}\frac{\rho_D\rho_S}{\rho_D + \rho_S}. \tag{15}$$

For this limit, the resistance is given by the sum of a width-dependent contact resistance and a geometrical resistance. Understanding of the regions of validity of these two extremes is necessary in that either extreme used outside its region of validity will underestimate the overall resistance.

The width-dependent contact resistance is of interest in that the contact resistance is in part determined by the sheet resistance of the diffusion beneath the silicide. Physically, the dependence of the contact resistance on the diffusion sheet resistivity is due to current crowding. Current crowding can best be illustrated by considering the current in the silicide as a function of position for the structure of Fig. 2(b). The fraction of current in the silicide as a function of position can be written as

$$\frac{I_S(x_2)}{I} = \frac{\rho_S \sinh \beta x_2 - \rho_D \sinh \beta(L_2 - x_2) + \rho_D \sinh \beta L_2}{(\rho_D + \rho_S)\sinh \beta L_2}. \tag{16}$$

An illustration of current crowding is shown in Fig. 4. Using (16), the fraction of current in the silicide is plotted as a function of position for various values of specific contact resistivity ρ_c. As the current approaches the unsilicided part of the diffusion, it is forced from the silicide. The value of specific

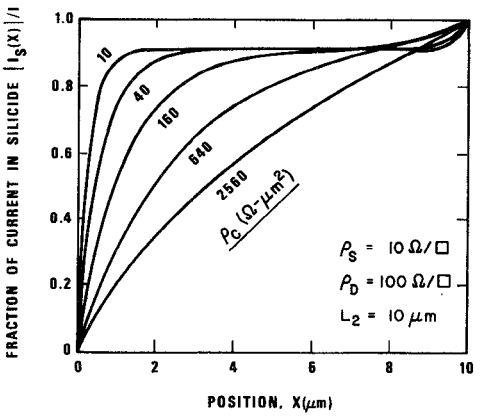

Fig. 4. The fraction of current in the silicide as a function of position, for different specific contact activities ρ_C.

contact resistivity determines the degree to which current crowding can occur. For small values of ρ_c, the current crowds into a relatively small region when going across the interface. For larger values of contact resistivity, much of the current is forced to go a considerable distance through the diffusion before reaching $x_2 = 0$. Hence the dependence of the width-related contact resistance on the diffusion sheet resistance.

B. Analysis of Three-Section Silicided Diffusion with Metal Contact

In Fig. 2(c), the full three-section coupled transmission line for the structure in Fig. 2(a) is shown. Sections 2 and 4 are composed of three-element transmission lines, while the two-element transmission line of section 3 is equivalent to assuming $\rho_S = 0$. This is justified because 1) the sheet resistance of the metal interconnect is typically at least a factor of 10 less than the silicide, and 2) the specific contact resistivity between a metal and silicide (which is nearly metallic in conductivity) should be much less than that arising from the metal-semiconductor Schottky-diode behavior of silicided diffusions.

In applying the theoretical equations in Section II to this case, it is convenient to subscript the variables x, $V_D(x)$, etc., and the coefficients A, B, etc., with a subscript denoting the section. The appropriate boundary and continuity conditions to determine the current-voltage relations are given as follows:

1) In section 4, $I_{S4}(x_4) = -I_{D4}(x_4)$.
2) At $x_4 = L_4$, $I_{S4}(L_4) = I_{D4}(L_4) = 0$.
3) At $x_4 = 0$, $V_{S4}(0) = V$, the applied voltage.
4) Between sections 3 and 4, at $x_3 = L_3$ and $x_4 = 0$, $V_{D3}(L_3) = V_{D4}(0)$.
5) At $x_3 = L_3$ and $x_4 = 0$, $I_{D3}(L_3) = I_{D4}(0)$.
6) Between sections 2 and 3, at $x_2 = L_2$ and $x_3 = 0$, $V_{D2}(L_2) = V_{D3}(0)$.
7) At $x_2 = L_2$ and $x_3 = 0$, $I_{D2}(L_2) = I_{D3}(0)$.
8) In section 2, $I_{S2}(x_2) + I_{D2}(x_2) = -I$.
9) At $x_2 = 0$, $I_{S2}(0) = 0$.
10) At $x_2 = L_2$, $V_{S2}(L_2) = V$, the applied voltage.

The derivation of contact resistance and the coefficients for each section proceeds by applying the boundary conditions above, first in section 4 and then in section 3. At this point, it is possible to define an effective resistance R'_C of sections 3 and 4 which shunts section 2 at $x_2 = L_2$. Using the remaining boundary conditions, the total resistance R_T is calculated, and the contact resistance R_C is identified.

Boundary conditions in section 4 result in

$$D_4 = 0 \tag{17a}$$

$$B_4 = A_4 e^{2\beta L_4} \tag{17b}$$

$$C_4 = V + \frac{\rho_S}{\rho_S + \rho_D}(A_4 + B_4). \tag{17c}$$

Using the continuity of diffusion region voltage and current between section 3 and 4, it can be shown that

$$A_3 e^{\alpha L_3} + B_3 e^{-\alpha L_3} = A_4(e^{2\beta L_4} + 1) \tag{18a}$$

$$A_3 e^{\alpha L_3} - B_3 e^{-\alpha L_3} = -A_4(e^{2\beta L_4} - 1)\frac{\rho_D}{\rho_S + \rho_D}\frac{\beta}{\alpha} \tag{18b}$$

with

$$\alpha = (\rho_c/\rho_D)^{1/2}$$

which can be solved for A_3 and B_3 in terms of A_4

$$A_3 = -\frac{1}{2}A_4 e^{-\alpha L_3}\left[(e^{2\beta L_4} - 1)\frac{\rho_D}{\rho_S + \rho_D}\frac{\beta}{\alpha} - (e^{2\beta L_4} + 1)\right] \tag{19a}$$

$$B_3 = +\frac{1}{2}A_4 e^{\alpha L_3}\left[(e^{2\beta L_4} - 1)\frac{\rho_D}{\rho_S + \rho_D}\frac{\beta}{\alpha} + (e^{2\beta L_4} + 1)\right]. \tag{19b}$$

It is convenient to define R'_C, the equivalent resistance shunting section 2, caused by sections 3 and 4 of the coupled transmission lines

$$R'_C \equiv \frac{V_{S3}(0) - V_{D3}(0)}{-I_{D3}(0)} = -\frac{\rho_D}{\alpha W}\frac{(A_3 + B_3)}{(A_3 - B_3)}. \tag{20}$$

After algebraic manipulation, it can be shown that

$$R'_C = \frac{\rho_D}{\alpha W}\frac{\cosh \alpha L_3 + \dfrac{\rho_D}{\rho_S + \rho_D}\dfrac{\beta}{\alpha}\tanh \beta L_4 \sinh \alpha L_3}{\sinh \alpha L_3 + \dfrac{\rho_D}{\rho_S + \rho_D}\dfrac{\beta}{\alpha}\tanh \beta L_4 \cosh \alpha L_3}. \tag{21}$$

When $L_4 = 0$, R'_C reduces to the resistance of a silicided contact hole [12], [14]. Digressing momentarily, it is useful to consider several limiting forms of R'_C. It can be seen that

$$R'_C\big|_{L_3 \to \infty} = R'_C\big|_{\substack{L_4 \to \infty \\ \rho_S << \rho_D}} = \frac{\rho_D}{\alpha W}. \tag{22}$$

Boundary conditions in section 2 result in

$$D_2 = \frac{\rho_S \rho_D}{\rho_S + \rho_D}\frac{I}{W} \tag{23a}$$

$$B_2 = A_2 - \frac{\rho_S + \rho_D}{\rho_S}\frac{D_2}{\beta} \tag{23b}$$

and

$$C_2 = V + \frac{\rho_S}{\rho_S + \rho_D}(A_2 e^{\beta L_2} + B_2 e^{-\beta L_2}) - D_2 L_2 \tag{23c}$$

while continuity of diffusion region voltage and current between sections 2 and 3 results in

$$A_2 e^{\beta L_2} + B_2 e^{-\beta L_2} = A_3 + B_3 \tag{24a}$$

and

$$-\frac{\beta W}{\rho_S + \rho_D}(A_2 e^{\beta L_2} - B_2 e^{-\beta L_2}) - \frac{D_2 W}{\rho_D} = -\frac{\alpha W}{\rho_D}(A_3 - B_3). \tag{24b}$$

Dividing these two equations, and using previous results for B_2 and the definition of R'_C, one can solve for A_2

$$A_2 = -\frac{\rho_D I\left[\frac{R'_C}{\rho_D} + \frac{R'_C}{\rho_S} e^{-\beta L_2} - \frac{\rho_S + \rho_D}{\rho_S}\frac{1}{\beta W} e^{-\beta L_2}\right]}{\frac{R'_C}{\rho_S}\beta W(e^{\beta L_2} - e^{-\beta L_2}) + \frac{\rho_S + \rho_D}{\rho_S}(e^{\beta L_2} + e^{-\beta L_2})}. \tag{25}$$

Using (23b), it can be shown that

$$B_2 = -\frac{\rho_D I\left[\frac{R'_C}{\rho_D} + \frac{R'_C}{\rho_S} e^{\beta L_2} + \frac{\rho_S + \rho_D}{\rho_S}\frac{1}{\beta W} e^{\beta L_2}\right]}{\frac{R'_C}{\rho_S}\beta W(e^{\beta L_2} - e^{-\beta L_2}) + \frac{\rho_S + \rho_D}{\rho_S}(e^{\beta L_2} + e^{-\beta L_2})}. \tag{26}$$

Using A_2 and B_2 in (24a) and (24b), and solving for A_3 and B_3 results in

$$A_3 = \frac{I\rho_D\left(\frac{1}{\alpha W} - \frac{R'_C}{\rho_D}\right)\left[\cosh \beta L_2 + \frac{\rho_D}{\rho_S}\right]}{\frac{R'_C}{\rho_S}\beta W(e^{\beta L_2} - e^{-\beta L_2}) + \frac{\rho_S + \rho_D}{\rho_S}(e^{\beta L_2} + e^{-\beta L_2})} \tag{27}$$

$$B_3 = -\frac{I\rho_D\left(\frac{1}{\alpha W} + \frac{R'_C}{\rho_D}\right)\left[\cosh \beta L_2 + \frac{\rho_D}{\rho_S}\right]}{\frac{R'_C}{\rho_S}\beta W(e^{\beta L_2} - e^{-\beta L_2}) + \frac{\rho_S + \rho_D}{\rho_S}(e^{\beta L_2} + e^{-\beta L_2})}. \tag{28}$$

Given A_3 or B_3, A_4 can be obtained from either (19a) or (19b), while B_4, C_4, and D_4 are given by (17a, b, c).

The total resistance R_T of the structure in Fig. 2(c) is given by

$$R_T = \frac{V_{S2}(L_2) - V_{D2}(0)}{I} = \frac{D_2 L_2 + A_2\left(e^{\beta L_2} + \frac{\rho_D}{\rho_S}\right) + B_2\left(e^{-\beta L_2} + \frac{\rho_D}{\rho_S}\right)}{I} \tag{29}$$

which, after algebraic manipulation, results in an expression of the form

$$R_T = \frac{\rho_S \rho_D}{\rho_S + \rho_D}\frac{L_2}{W} + R_C \tag{30}$$

in which the first term is identified as the geometrical line resistance of section 2, from $x_2 = 0$ to $x_2 = L_2$ at the leading edge of the contact hole. The second term, R_C, is identified as the contact resistance and is given by

$$R_C = \frac{\frac{\rho_D^2}{\rho_S \beta W}\sinh \beta L_2 + \frac{R'_C \rho_D}{\rho_S + \rho_D}\left(2 + \frac{\rho_S^2 + \rho_D^2}{\rho_S \rho_D}\cosh \beta L_2\right)}{\frac{\rho_S + \rho_D}{\rho_S}\cosh \beta L_2 + \frac{R'_C}{\rho_S}\beta W \sinh \beta L_2}. \tag{31}$$

When $R'_C \to \infty$ (equivalent to L_3 and $L_4 \to 0$), this reduces to the simplified case shown in Fig. 2(b). Equation (31) describing the three-section model of Fig. 2(c) is compared to (12) describing the simplified single-section of Fig. 2(b) in Fig. 5. The single-section model has a contact resistance which increases indefinitely as the length L_2 decreases. In contrast, the three-section model has a finite contact resistance as a result of the termination of section 2 by sections 3 and 4. As L_2 becomes greater than the characteristic length β^{-1}, which for the example in Fig. 5 is 4.8 μm, the contribution of section 2 to the contact resistance begins to dominate, and the two curves asymptotically approach one another. The current distributions for $L_2 = 2$ μm and $L_2 = 10$ μm for the single- and three-section model cases are shown on Fig. 6. For $L_2 = 10$ μm, the contact resistances are nearly the same (as seen in Fig. 5), even though the current distribution of the single-section case with $L_3 = L_4 = 0$ in Fig. 6 is perceptibly altered by the termination sections present for the three-section case with

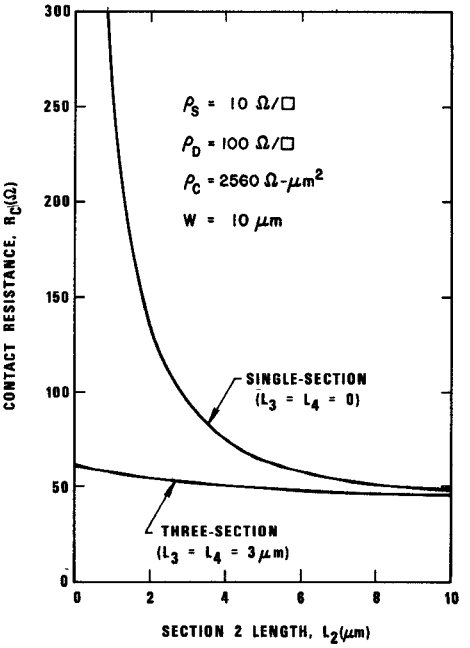

Fig. 5. Contact resistance R_C versus section 2 length L_2 for single-section and three-section models of Fig. 2.

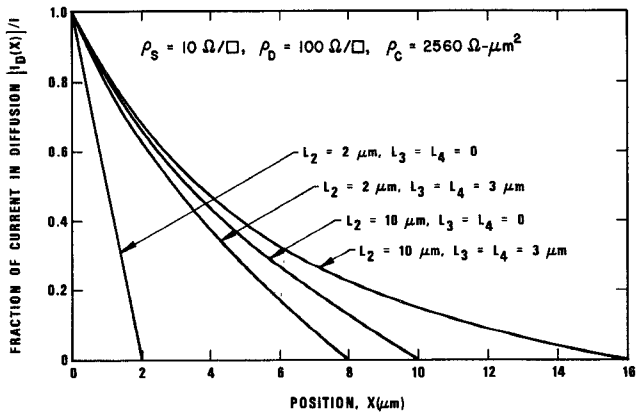

Fig. 6. Fraction of current in diffusion as a function of position for the single-section model ($L_3 = L_4 = 0$) and for the three-section model ($L_3 = L_4 = 3$ μm) of Fig. 2.

L_3, $L_4 \neq 0$. However, the gradient of the current, which determines the current-spreading contribution of ρ_c to the contact resistance, is not significantly altered. In contrast, for $L_2 = 2$ μm, for which the contact resistances differ by almost a factor of 2 (as seen in Fig. 5), the two cases have appreciably different gradients of the current.

It is useful to consider two limiting forms for R_C

$$R_C\Big|_{\beta L_2 \gg 1} = \frac{\frac{\rho_D^2}{\beta W} + R_C'\left(\frac{\rho_S^2 + \rho_D^2}{\rho_S + \rho_D}\right)}{(\rho_S + \rho_D + R_C'\beta W)} \tag{32a}$$

and

$$R_C\Big|_{\substack{\beta L_2 \gg 1 \\ \rho_S \ll \rho_D}} = \frac{\rho_D}{\alpha W}. \tag{32b}$$

From (32), it can be seen that the contact resistance is limited to the same value as R_C' (as given by (22)). Thus although silicided diffusions may superficially appear to offer the potential of reduced overall resistance, the contact resistance is still limited to the same value that limits a silicided contact hole.

C. Analysis of Interconnecting Silicided Diffusion Without Contacts

In addition to reducing the resistance between an aluminum contact and the source of a transistor, silicides can also be used to reduce the resistance between two MOSFET's connected by a diffusion. Such a structure is shown in Fig. 7. Again the relation between the silicide and diffusion voltages is described by (6a) and (6b). However, this time the boundary conditions are given as

1) At $x = 0$, $V_D = V$.
2) At $x = L$, $V_D = 0$.
3) At $x = 0$, $\left.\frac{dV_S}{dx}\right|_{x=0} = 0$.
4) At $x = L$, $\left.\frac{dV_S}{dx}\right|_{x=L} = 0$.

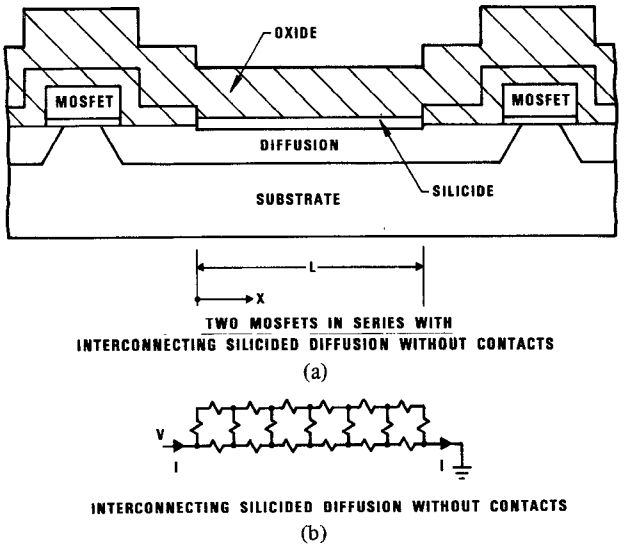

Fig. 7. Illustration showing (a) a cross section of two MOSFET's in series; and (b) the transmission line model for the central silicided section.

For the above described boundary conditions, the voltages in the respective layers are given as

$$V_D(x) = \frac{V[\rho_D \cosh \beta(L-x) - \rho_D \cosh \beta x - \rho_S \beta x \sinh \beta L]}{2\rho_D(\cosh \beta L - 1) + \rho_S \beta L \sinh \beta L} + \frac{V[\rho_D(\cosh \beta L - 1) + \rho_S \beta L \sinh \beta L]}{2\rho_D(\cosh \beta L - 1) + \rho_S \beta L \sinh \beta L} \tag{33}$$

and

$$V_S(x) = \frac{V[\rho_S \cosh \beta(L-x) - \rho_S \cosh \beta x + \rho_S \beta x \sinh \beta L]}{2\rho_D(\cosh \beta L - 1) + \rho_S \beta L \sinh \beta L} + \frac{V[\rho_D(\cosh \beta L - 1) + \rho_S \beta L \sinh \beta L]}{2\rho_D(\cosh \beta L - 1) + \rho_S \beta L \sinh \beta L}. \tag{34}$$

From (33) and (34) the resistance of the silicided layer indicated in Fig. 4(a) and (b) is given by

$$R_T = \frac{\rho_D \rho_S}{\rho_D + \rho_S}\frac{L}{W} + \frac{2\rho_D^2}{\rho_D + \rho_S}\frac{\tanh(\beta L/2)}{\beta W}. \tag{35}$$

In Fig. 8 the resistance of the silicided diffusion has been calculated as a function of length L for various values of specific contact resistivity. In general, it is seen that the resistance is determined by the sum of two separate contributions.

Again a critical value of length L_C can be defined such that

$$L_C = 2\left(\frac{\rho_c}{\rho_D + \rho_S}\right)^{1/2}. \tag{36}$$

For $L \ll L_C$, the resistance is given by

$$R_T\Big|_{L \ll L_C} = \frac{L}{W}\rho_D \tag{37}$$

which means that the contact resistivity is high enough that the presence of silicide has no effect on the resistance. For $L \gg L_C$, the resistance is given by

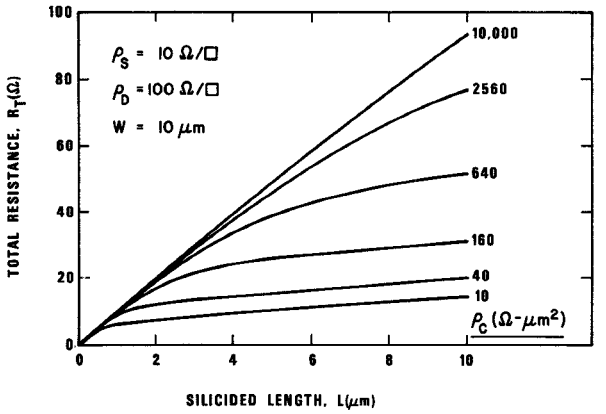

Fig. 8. Total resistance R_T of the interconnecting silicided diffusion without contacts versus silicided length L for different specific contact resistivities ρ_C.

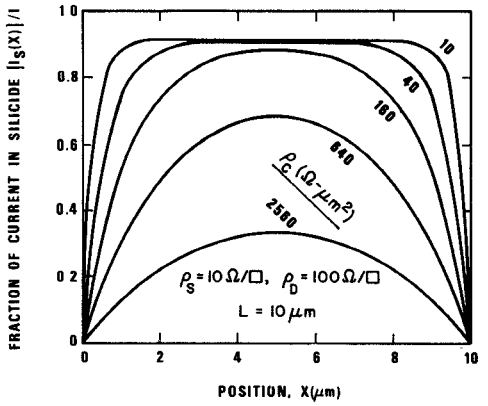

Fig. 9. The fraction of current in the silicide as a function of position, for different specific contact resistivities ρ_C.

$$R\big|_{L>>L_C} = \frac{2}{W}\left[\frac{\rho_D}{\rho_D+\rho_S}\right]^2 (\rho_c(\rho_D+\rho_S))^{1/2} + \frac{\rho_D\rho_S}{\rho_D+\rho_S}\frac{L}{W}. \tag{38}$$

In this case, as in Section II-A, the resistance is given as the sum of two contributions, a width-dependent contribution and a geometrical contribution. However, in (38) there are two contact resistance contributions since the current starts in the diffusion, goes into the silicide, and then returns to the diffusion. Thus the silicide-silicon interface is crossed twice.

The above two limiting cases of (35) are best comprehended by considering the fraction of the current in the silicide as a function of position. Using (2) and (34), the silicide current for the structure of Fig. 7 is given as

$$\frac{I_S(x)}{I} = \frac{\rho_D}{\rho_D+\rho_S}\frac{\sinh\beta L - \sinh\beta x - \sinh\beta(L-x)}{\sinh\beta L}. \tag{39}$$

In Fig. 9, the current in the silicide is plotted as a function of position for various values of contact resistivity. At low values of contact resistivity (or equivalently $L \gg L_C$), the current crowds at either end to enter the low sheet resistivity silicide. As the value of L_C or ρ_c increases, a significant fraction of the current does not enter the silicide. For very high values of ρ_C, little of the current enters the silicide and thus the limiting case defined by (37) applies.

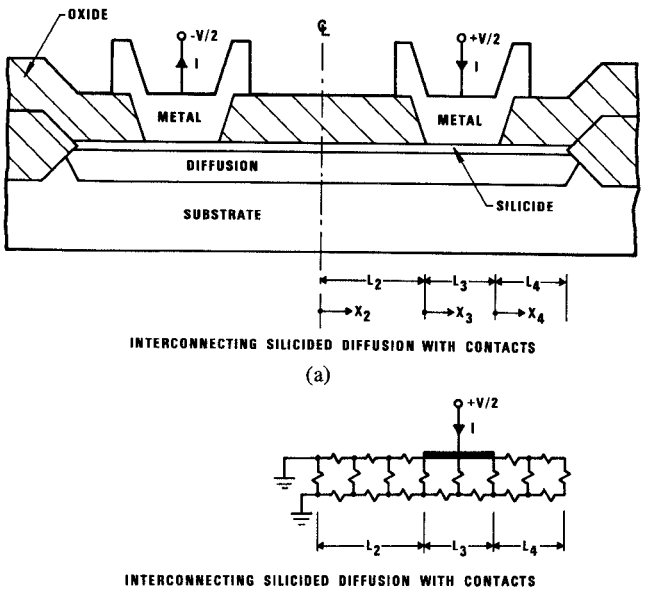

Fig. 10. Illustration showing (a) a cross section of a silicided, diffused resistor with contact; and (b) the transmission line model.

For long diffusion lines, the use of silicides will reduce the resistance between the two transistors shown in Fig. 7. The results of the calculations in this section show that the total resistance will be dominated by the contact resistance in many cases and, therefore, the geometrical resistance determined from the sheet resistivity of the silicide will be a secondary consideration.

D. Analysis of Interconnecting Silicided Diffusion with Contacts

The final example, shown in Fig. 10, is a totally silicided diffused resistor. The only boundary condition which differs from the case in Fig. 2(c) is in the silicide at $x_2 = 0$. Instead of $I_{S2}(0) = 0$, the appropriate boundary condition, by symmetry, is $V_{S2}(0) = 0$, which coupled with $V_{D2}(0) = 0$, results in

$$B_2 = -A_2 \tag{40a}$$

and

$$C_2 = 0. \tag{40b}$$

Otherwise, all previous relations for example 2 still apply. In particular, it can be shown that

$$2A_2 = -\frac{IR'_C}{\frac{\rho_S+\rho_D}{\rho_S}\sinh\beta L_2 + \frac{R'_C}{\rho_S}\beta W\cosh\beta L_2}. \tag{41}$$

In conjunction with the requirement that $V_{S2}(L_2) = V/2$, this permits the total resistance R_T to be calculated

$$R_T = \left(\frac{\rho_S\rho_D}{\rho_S+\rho_D}\right)\frac{2L_2}{W} + 2R_C \tag{42}$$

where the contact resistance R_C is given by

$$R_C = \frac{R'_C\left(\frac{\rho_S}{\rho_S+\rho_D}\right)\sinh \beta L_2}{\frac{\rho_S+\rho_D}{\rho_S}\sinh \beta L_2 + \frac{R'_C}{\rho_S}\beta W \cosh \beta L_2}. \quad (43)$$

One limiting case is of interest

$$R_C\Big|_{\substack{\beta L_2 >> 1 \\ \rho_D >> \rho_S}} = \frac{\rho_D}{\alpha W}\frac{1}{2}\left(\frac{\rho_S}{\rho_D}\right)^2 \quad (44)$$

which is a factor $\frac{1}{2}(\rho_S/\rho_D)^2$ times smaller than the value of R_C in Section II-B in the same limits.

IV. Impact of Silicided Diffusions on Device and Circuit Performance

In this section, the transmission line model developed in Sections II and III is used to examine the impact of silicided junctions on VLSI technologies. As the horizontal dimensions of an MOS device are scaled down, the vertical dimensions (gate-oxide thickness, junction depth, etc.) also need to be scaled down in order to reduce undesirable short-channel effects [8]. A consequence of this scaling of the vertical dimensions is an increase in sheet resistivity of diffused junctions which limits the performance of MOS devices [5], [6], and also increases circuit delay time if such diffusions are used as interconnect lines.

Before considering specific applications of transmission line models, it is instructive to examine the scaling property of diffused (or ion-implanted) junctions as the junction depth x_j is scaled down. In the past [5], [6], [8], the $1/x_j$ dependence of sheet resistivity has been extensively used. This dependence, however, is only valid for a relatively deep junction which can maintain a doping concentration close to solid solubility throughout its depth. For a very shallow junction, the peak doping concentration must be reduced in order to accomodate the ion-implantation range and the diffusion during annealing. This reduction of peak concentration results in an increase in sheet resistivity. In Fig. 11 we show SUPREM [15] simulations of arsenic- and boron-implanted junctions which have been subsequently driven in during typical annealing conditions to illustrate the dependence of sheet resistivity on junction depth. The arsenic junction simulation has used a 50-keV implant, annealed at 950°C for 20 min. The boron junction simulation has used a 15-keV implant, annealed at 975°C for 19 min [17]. For both types, the implant dose has been adjusted to obtain a specified junction depth for fixed annealing conditions. Also shown in Fig. 11 are the experimental data by Tsai *et al.* [16]. From Fig. 11 one can see the much stronger dependences of sheet resistivity on junction depth than $1/x_j$, which is shown by a broken curve. For the boron-diffused junction, the sheet resistivity ρ_D can be closely approximated by

$$\rho_D = k_1\left(\frac{1}{x_j}\right)^5 \quad (45)$$

where $k_1 = 1.3\ \Omega \cdot \mu m^5$, ρ_D is in ohms per square, and x_j in micrometers. Similarly, for the arsenic-diffused junction, the variation can be expressed as

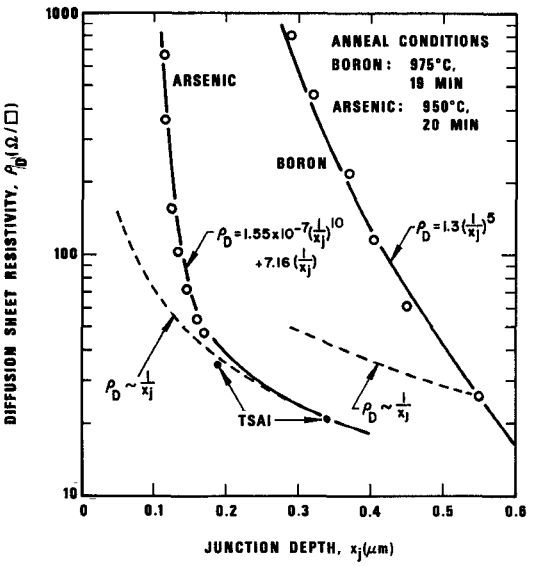

Fig. 11. SUPREM simulations of diffusion sheet resistivity ρ_D as a function of junction depth x_j for boron and arsenic. Data (·) are experimental from Tsai *et al.* [16].

$$\rho_D = k_2\left(\frac{1}{x_j}\right)^{10} + k_3\left(\frac{1}{x_j}\right) \quad (46)$$

where $k_2 = 1.55 \times 10^{-7}\ \Omega \cdot \mu m^{10}$, and $k_3 = 7.16\ \Omega \cdot \mu m$. For arsenic, the sheet resistivity varies as $1/x_j$ down to 0.2 μm, below which the resistivity starts to increase quite rapidly as the junction depth is decreased further. Although different annealing conditions may yield slightly different dependence, the general features remain unchanged. Therefore, the $1/x_j$ dependence previously assumed [5], [6], [8] gives an overly optimistic picture of scaled-down junctions.

A. Application to Scaled Device Performance

The above considerations, together with (30) and (31), describing the contact resistance of a silicided diffusion can be used to examine the effect of scaling of source-drain series resistance of an MOS device as shown in Fig. 2(a). In our scaling scheme, all the horizontal dimensions are assumed to scale down linearly with a scaling factor κ ($\kappa < 1$), whereas the junction depth only scales as $\kappa^{1/2}$ comprehending the difficulty to make very shallow junctions. A patterned gate length of 3 μm and a gate-oxide thickness of 600 Å is used as a reference (unscaled device) with $L_1 = L_2 = 1.5$ μm, $L_3 = L_4 = 3$ μm, and $x_j = 0.4$ μm. Fig. 12 shows the result of the calculation, which plots the total source-drain series resistance as a function of patterned gate length for boron-diffused junction with and without silicide. The silicide sheet resistivity is assumed to be constant, $\rho_S = 2\ \Omega/\square$. For a silicided case, two different specific contact resistivities (ρ_c, 10 and 100 $\Omega \cdot \mu m^2$) between silicide and diffused junction are considered, although ρ_c for a metal-semiconductor Schottky barrier can be expected to be a function of x_j due to the dependence on doping concentration in the semiconductor diffusion. By siliciding the source-drain diffusion, the total series resistance can be reduced by a factor of 2. Reducing the specific contact resis-

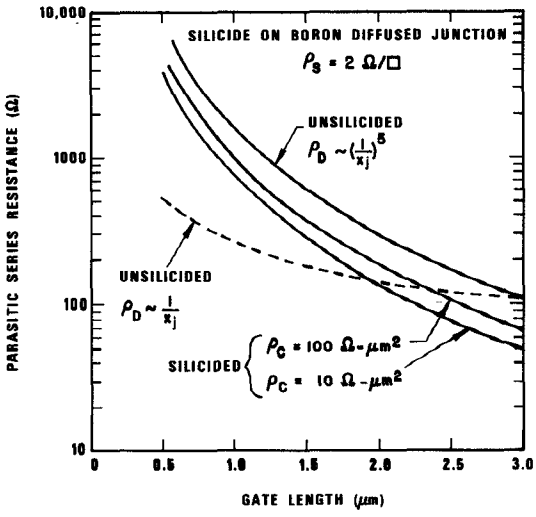

Fig. 12. Series source and drain resistance of scaled MOSFET's as a function of patterned gate length.

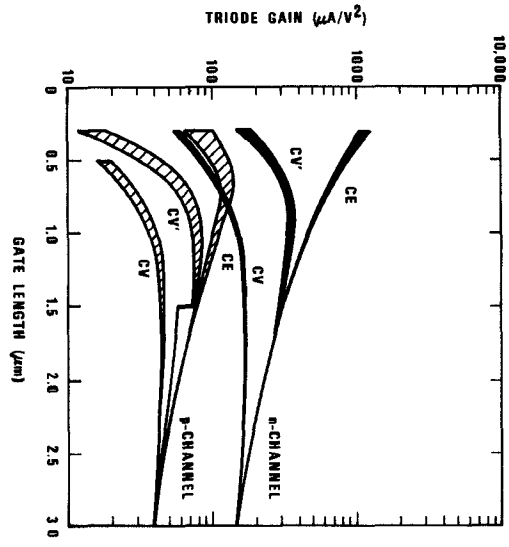

Fig. 13. Triode gain of scaled MOSFET's versus patterned gate length for n-channel and p-channel devices assuming constant field scaling (CE), constant voltage scaling (CV), and realistic scaling (CV').

tivity aslo improves the series resistance by approximately 40 percent. Also shown in Fig. 12 is the result from an optimistic $1/x_j$ dependence of diffused junction resistance without silicide. Clearly, this dependence underestimates the series resistance. For all the cases, a rapid increase of series resistance below 1 μm is also noted. This is due to the increased contribution from contact resistance.

This analysis of series resistance can be incorporated into the calculation of effective triode gain of an MOS device. The source-drain series resistance of the device serves as a feedback loop, and reduces the effective device gain [5], [6]. In our calculation of triode gain we also include such effects as the mobility rolloff due to parallel and perpendicular electric fields, and inversion-layer capacitance [6].

The mobility of carriers at Si-SiO_2 interface including the dependence on parallel and perpendicular electric field can be written as

$$\mu(E_x, E_y) = \frac{\mu_0}{\left(1 + \frac{E_x}{E_{cx}}\right)\left\{1 + \left(\frac{E_y}{E_{cy}}\right)^{\beta}\right\}^{1/\beta}} \tag{47}$$

where μ_0 is the low-field mobility, E_x and E_y are electric fields perpendicular and parallel to the interface, respectively. The values for E_{cx}, E_{cy}, and β have been recently determined experimentally [18]. For large gate voltages, the perpendicular electric field E_x is given approximately by

$$E_x = \frac{1}{2}\,\frac{V_G - \phi_{ms} - \psi_s}{t_{ox}}\,\frac{\epsilon_{ox}}{\epsilon_{Si}} \tag{48}$$

where t_{ox} is the gate-oxide thickness, ϵ_{ox} and ϵ_{Si} are the dielectric constants for oxide and silicon, respectively, ϕ_{ms} is the metal-semiconductor work function, and ψ_s is the surface potential. The factor of $\frac{1}{2}$ comes from the averaging of electric field over the charge distribution in the inversion layer [19]. The parallel field E_y can be obtained from the drain voltage V_D which is arbitrarily chosen as

$$V_D = \tfrac{1}{5}\,(V_G - V_T) \tag{49}$$

to describe the device operation in linear region. Then, E_y is given by

$$E_y = \frac{V_D}{L_e} \tag{50}$$

where L_e is the channel length. The effect of finite inversion-layer thickness is incorporated as a series capacitance to the gate-oxide capacitance [6], which causes a decrease of effective gate capacitance when the inversion layer thickness becomes comparable to the gate-oxide thickness. The inversion-layer capacitance is calculated from the average distance of inversion charge from the Si-SiO_2 interface [20].

In examining the device performance in scaled MOS technology three different scaling schemes have been considered. The first scheme is a constant field scaling (denoted as CE) [8] where the operating voltage is scaled down linearly with physical (horizontal) dimensions, starting at 5 V for 3-μm gate length. The second scheme is a constant voltage scaling (CV) where the operating voltage stays constant at 5 V. The third scheme that we consider is a variation of constant voltage scaling. In this scheme, the operating voltage is reduced stepwise from 5 to 3 V at gate length of 1.5 μm. This scaling scheme, denoted at CV', is expected to best describe the present trend in MOS industry.

In Fig. 13 we show triode gain of an n-channel and a p-channel MOS device as a function of patterned gate length. The triode gain is given by [21]

$$K' = \frac{\mu C \frac{W}{L_e}}{1 + \mu C \frac{W}{L_e}(V_G - V_T) R_T} \tag{51}$$

where R_T is the total series resistance shown in Fig. 12, C is a series combination of gate-oxide capacitance and inversion capacitance, W is the width of the device, μ is the mobility given by (47), and L_e is the effective electrical channel length, calculated as $L_e = L - 2\gamma x_j$, with $\gamma = 0.8$. $W = 9$ μm is assumed

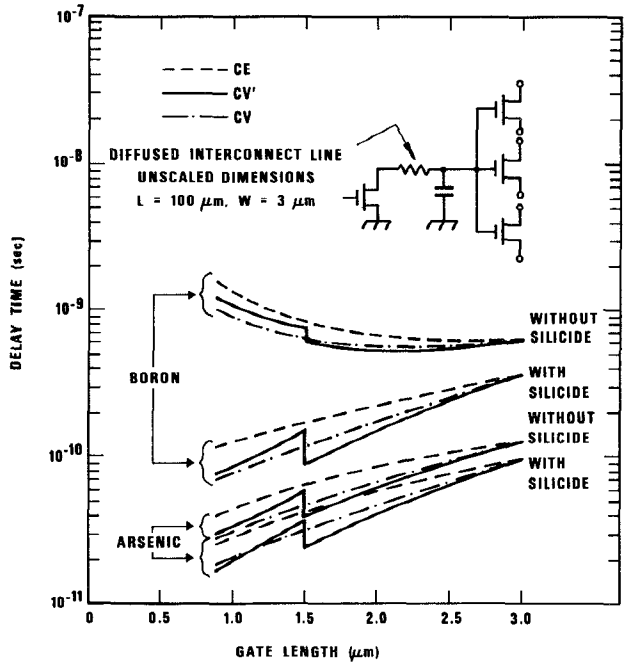

Fig. 14. Propagation delay time versus patterned gate length for boron- and arsenic-interconnect diffusion, with and without silicide.

for an unscaled device ($\kappa = 1$). The band in Fig. 13 refers to the best and the worst case of series resistance, the upper curve representing the diffused junctions with silicide, and the lower curve without silicide. The decrease of the gain below 1 μm is mostly due to the mobility degradation. As seen from this figure, the improvement of triode gain by siliciding source-drain is not expected to be very large although as the channel length decreases below 1 μm improvements up to 60 percent for p-channel devices can be expected. The improvement is larger for a p-channel device because of the larger series resistance of unsilicided boron junctions.

B. Application to Scaled Circuit Performance

As shown in the preceding subsection, not much improvement is expected on the triode gain by siliciding source-drain diffusions. However, as will be shown, the circuit performance does improve when a silicided diffusion line is used as an interconnect. This is illustrated in Fig. 14, where the circuit delay time of a simple circuit (see insert in Fig. 14) with a driven diffused interconnect line and three identical MOS load devices (fan-out = 3). The unscaled dimensions of the interconnect line are assumed to be 100 μm long by 3 μm wide. The capacitance of the line is estimated from the experimentally determined sidewall capacitance [22]. The circuit delay time can be expressed to a first order by

$$t_d = \frac{C_L}{g_c} + R_L C_L \tag{52}$$

where $g_c = K'(V_G - V_T)$ is the channel conductance of the driver in the linear region where K' is given by (51), R_L is the resistance of interconnect line, and C_L is the total load capacitance. Equation (35) is used to calculate R_L. Fig. 14 shows a dramatic improvement up to 200X of delay time for a boron-diffused junction with silicide. For an arsenic-diffused junction, the improvement is only a factor of 2, because the time delay is also limited by the intrinsic delay of the driver (C_L/g_c term). From Figs. 13 and 14 it is concluded that the major benefit of siliciding diffusion is a lower resistance of interconnect lines, rather than superior performance of each device. The improvement is larger for scaled-down devices and circuits because of the increasing sheet resistivity of diffused junctions.

V. Conclusions

Due to larger series resistances associated with boron junctions, the use of silicides is most beneficial to technologies using p-channel devices although a speed advantage for n-channel devices is still observed. In fact, it can be argued that, in a scaled technology, the use of silicides on the diffusions retains this partial level of interconnect that was lost due to the engineering tradeoffs exercised in shrinking device geometries. Otherwise, the high diffusions sheet resistance values obtained in a scaled technology would require an additional, probably metallic, interconnect line to replace the diffusion line.

The advantage of silicides is enhanced by new information on the dependence of sheet resistivity on junction depth. It was found that the diffusion sheet resistance increases much more rapidly with decreasing junction depth than has been assumed in previous scaling considerations [5], [6], [8]. Thus in many cases the parasitic series source and drain resistance will dominate the characteristics of circuits using small-geometry devices.

In this paper it has been shown in Section III-A that the contact resistance is width dependent rather than area dependent for silicide lengths greater than the characteristic length L_C as shown in Fig. 3. In this approximation, as described by (15), the contact resistance depends equally on both the diffusion sheet resistance and the specific contact resistivity. This result is consistent with results obtained by previous authors [12], [14]. However, it was also found that in most cases the contact resistance will dominate over the resistance due to the silicide sheet resistance.

To a point, the use of silicides will eliminate much of the parasitic source and drain resistance. However, not only does the contact resistance have an explicit dependence on the diffusion sheet resistance, it is expected that ρ_c itself will increase as junction depths decrease and sheet resistances increase [23]. The latter is due to the reduced surface concentration of the diffusions as a result of scaling the junction depth. These phenomena together will serve to place a fundamental limit on the extent to which the series source and drain resistance can be reduced. Implicit in the above is also a fundamental limit to device scaling.

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Threshold-Voltage Temperature Drift in Ion-Implanted MOS Transistors

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Abstract—**Ion implantation has been widely employed to adjust the threshold voltage of MOS transistors made on low-conductivity substrates. However, the temperature variation of device characteristics associated with the ion implantation has not been fully understood. In this paper, an analysis of the effect of the ion implantation on the threshold-voltage drift is presented, and simple but accurate design equations for predicting the temperature coefficients of the threshold voltages of implanted devices relative to those of unimplanted devices are given. Experimental results from four basic types of devices exhibit close agreement with theory. The analysis presented here is directly applicable to the design of an on-chip NMOS voltage reference based on the threshold voltage difference due to the ion implantation.**

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List of Symbols

C_{OX}	Gate oxide capacitance per unit area, ϵ_s/t_{OX}.
KT/q	Thermal voltage, 26 mV at 300 K.
n_i	Intrinsic concentration, $\approx 1.4 \times 10^{10}$ cm^{-3}.
N_a	Bulk density.
N_{ai}	Enhancement acceptor implant density.
N_{di}	Depletion donor implant density.

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