ECE 124A
VLSI Principles
Lecture 4

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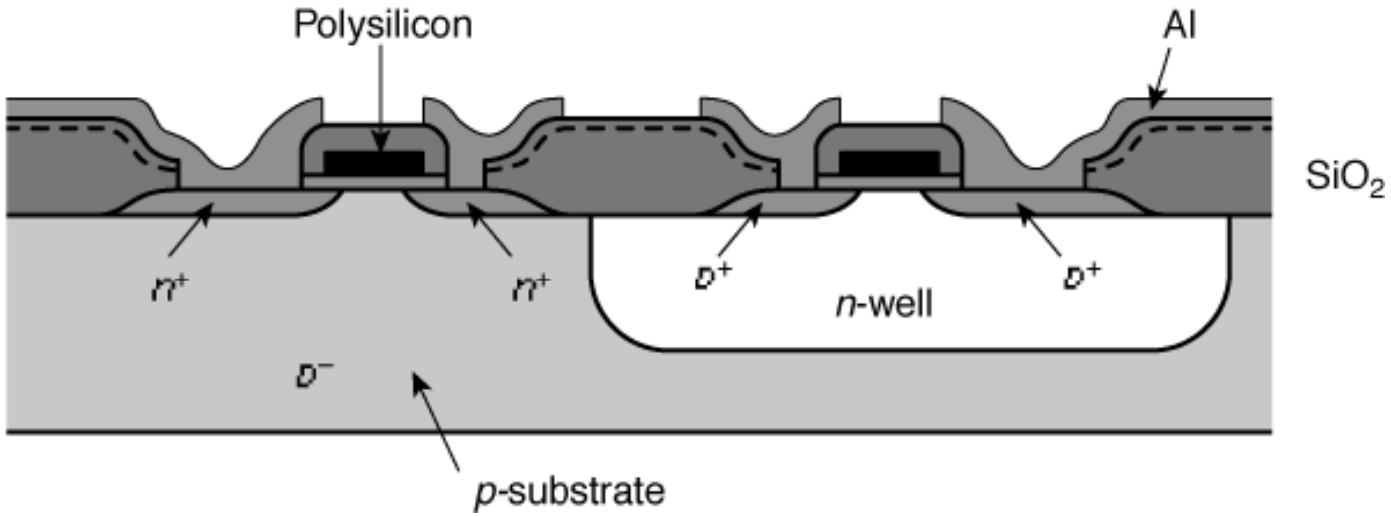
CMOS Process



A single-well CMOS….

Note the LOCOS (Local Oxidation of Si) process used for isolation of different transistors

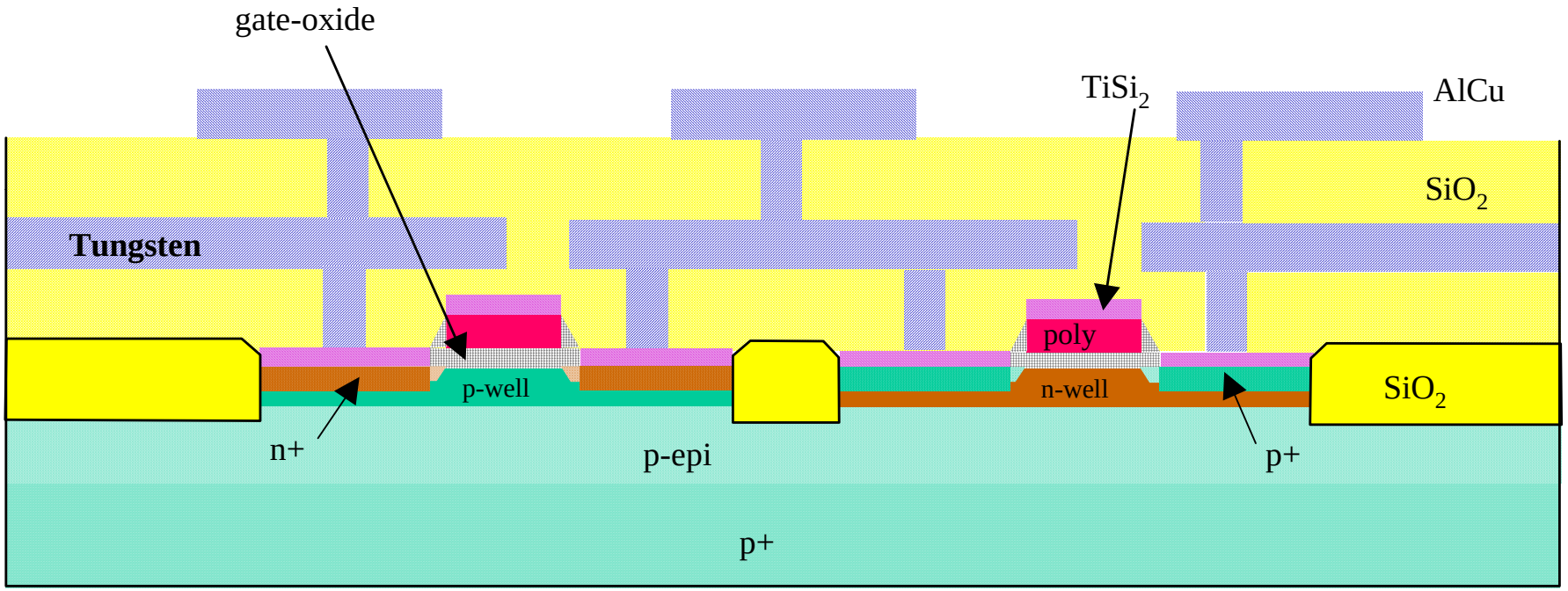
A problem with LOCOS is….Bird's Beak!.....which can eliminate the active areas…..in scaled CMOS technology

(solution: use STI-shallow trench isolation)

Basic Steps-I

- **Si Wafer:**
  - Single-crystalline, lightly-doped wafer (6-12 inch diameter)
  - Thickness of at most 1mm
  - Obtained by cutting a single crystal ingot into thin slices
  - An epitaxial layer is grown over the surface of the wafers before device processing
  - A starting p- wafer has a typical resistivity of 25-50 Ohm-cm, which corresponds to a doing level of the order of 10^{15} cm^{-3}
  - Defect density must be very low
  - Well dopings are of the order of 10^{16} to 10^{17} cm^{-3} (this explains the lower doping of the p substrate
  - Crystal orientation: all ICs are manufactured using (100) surface orientation. Why? (fewer imperfections on a (100) surface….gives significantly better Si/SiO_2 interface)

A Modern CMOS Process



Dual-Well Trench-Isolated CMOS Process
----allows more precise control of substrate doping

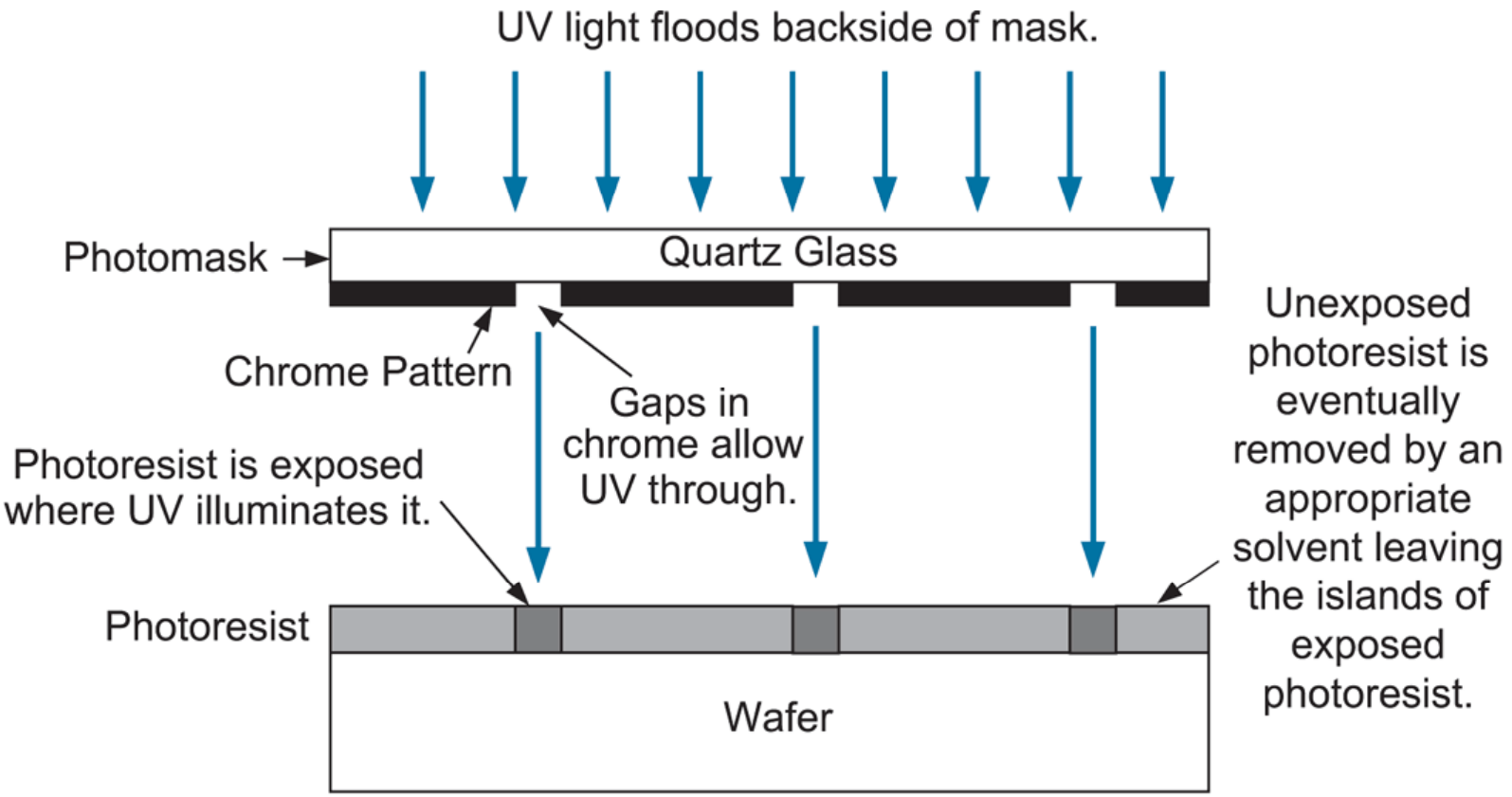
Basic Steps-II

- **Photolithography:**
  - Applied throughout the manufacturing process
  - In each processing step, a certain area of the chip needs to be masked out---using an appropriate optical mask
  - Desired processing step can be selectively applied to the remaining regions
  - Needed for a number of processing steps:
    - oxidation, etching, metal and polysilicon deposition, ion implantation
  - Different operations involved in a typical photolithographic process
    - Oxidation layering, photoresist (PR) coating, stepper exposure, PR development and bake, acid etching, spin-rinse-dry

Negative PR: a light sensitive polymer that is originally soluble in an organic solvent, but has the property that the polymers cross-link when exposed to light, making the affected areas insoluble.

Positive PR: originally insoluble but soluble after exposure

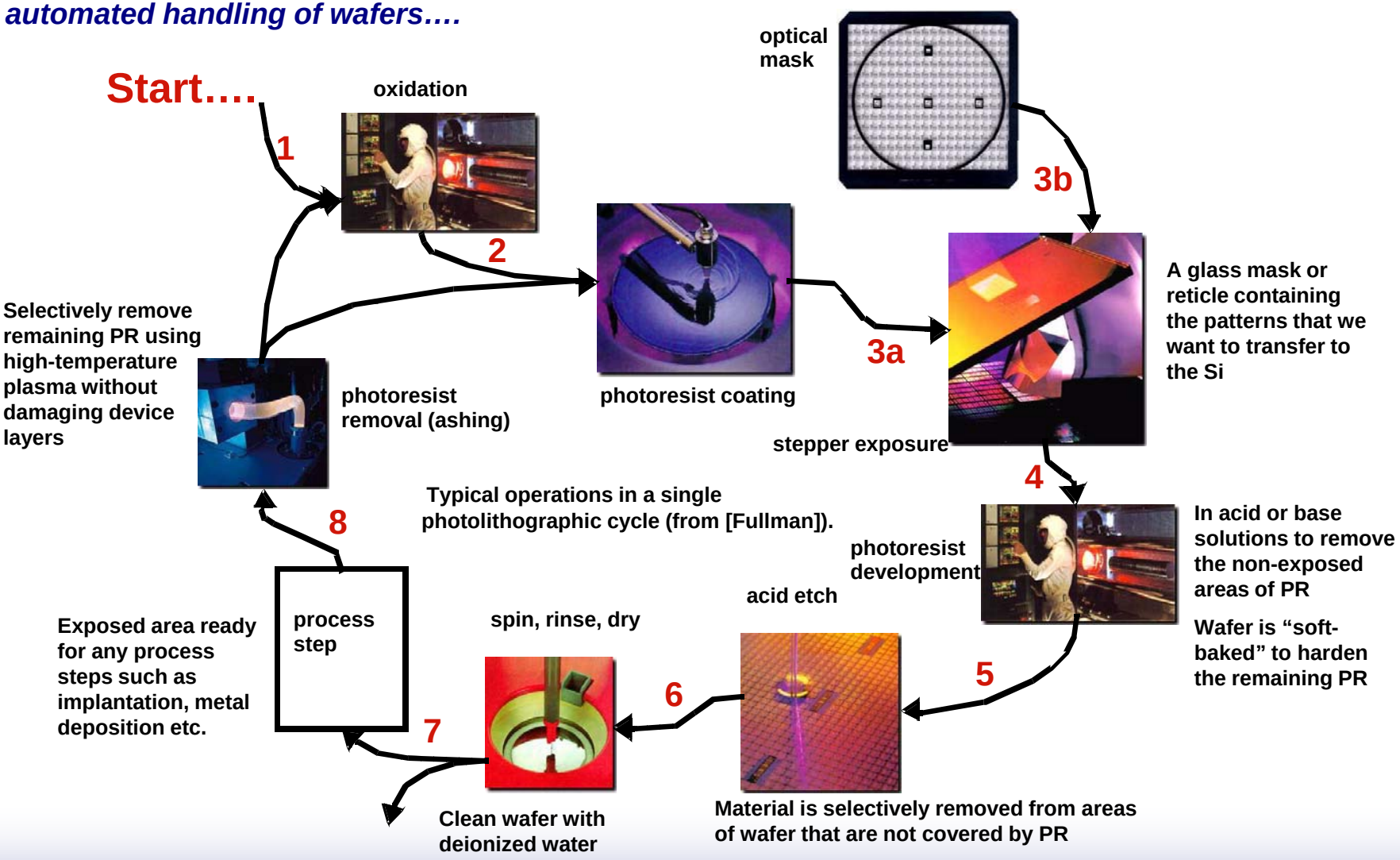
Photolithography:



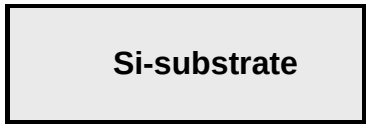
Photomasking with negative photoresist

Photo-Lithographic Process

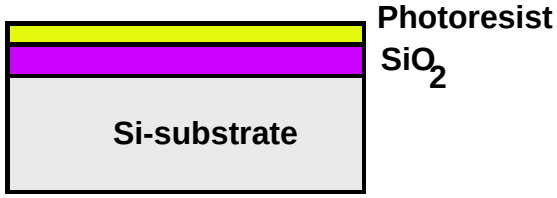
Clean room is needed: density of dust particles around 1-10 per cubic-foot of air!
automated handling of wafers….



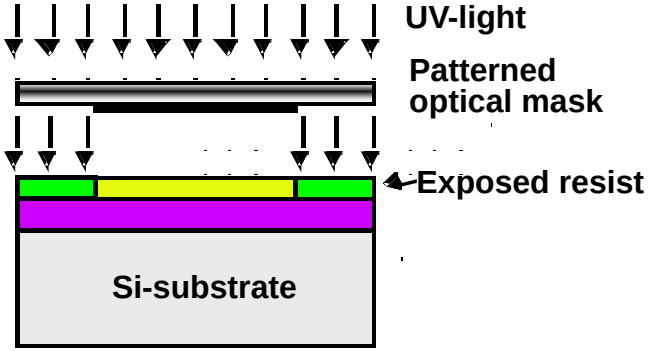
Patterning of SiO2



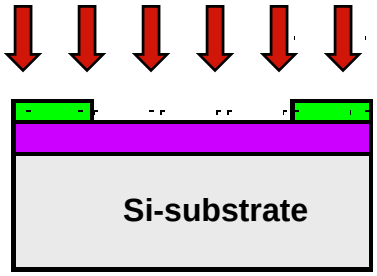
(a) Silicon base material



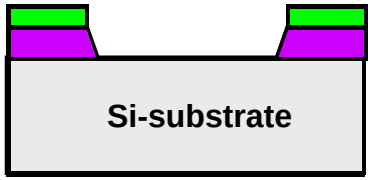
(b) After oxidation and deposition of negative photoresist



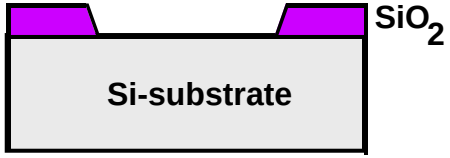
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO_2

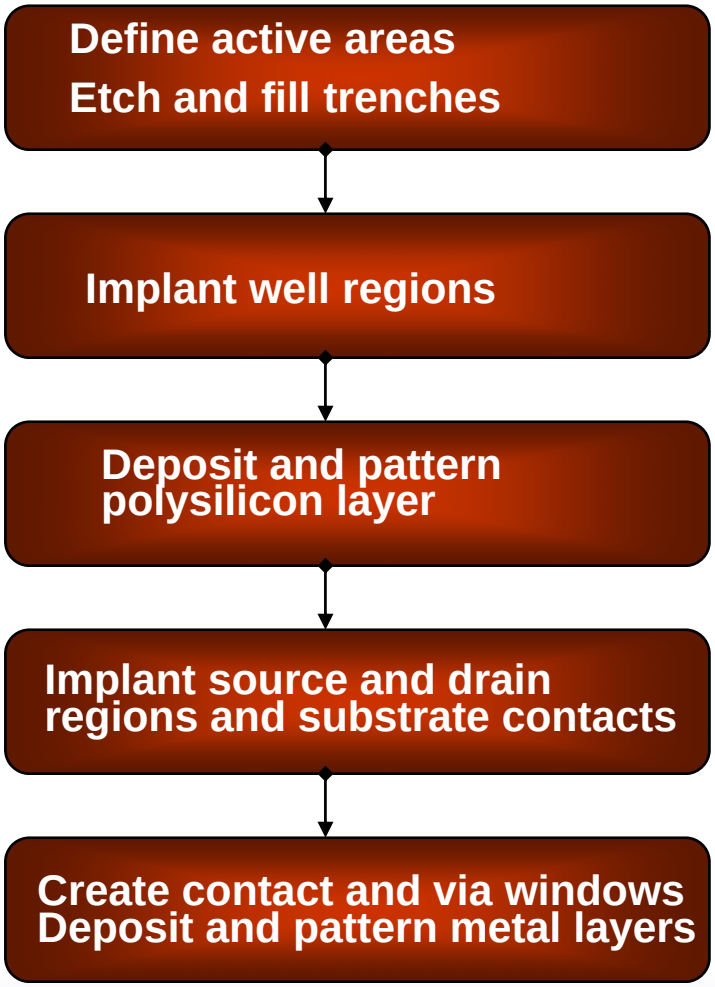


(e) After etching



(f) Final result after removal of resist

CMOS Process at a Glance



Device isolation: Local Oxidation of Si (LOCOS)—Bird's Beak problem….

Shallow Trench isolation (STI): better suited for small device geometries. Plasma etch trench + grow thin "liner" oxide (10-20 nm) layer + deposit oxide in trench

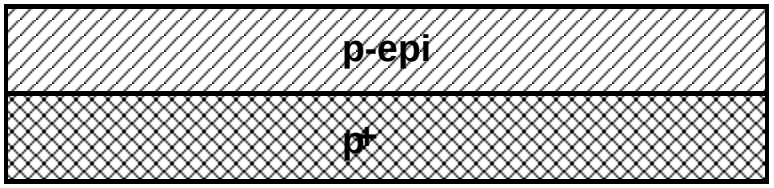
Recurring Process Steps-I

- Diffusion
  - Wafers placed in quartz tube embedded in a heated furnace (900-1100 C)
  - Dopants introduced through a gas
  - Dopants diffuse into the exposed surface
  - Final dopant concentration greatest at the surface and decreases in a gaussian profile deeper into the material
- Ion Implantation:
  - Dopants are introduced as ions in the material
  - Implantation system directs and sweeps a beam of purified ions over the Si surface
  - Wafer needs annealing (wafer is heated to 1000 C for 15-30 minutes) to repair lattice damage and to activate the dopants

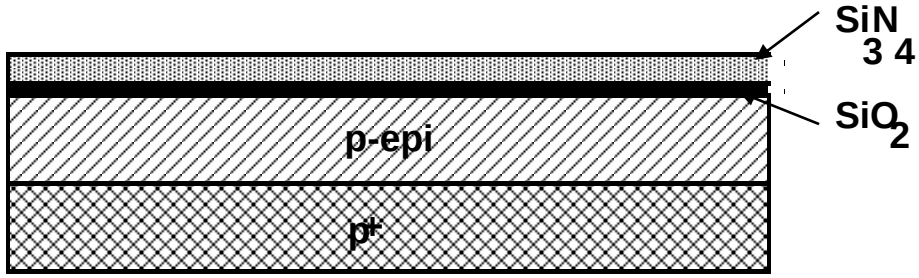
Recurring Process Steps-II

- Deposition
  - Many of the materials (gate oxide, silicon nitride, poly etc) are directly deposited
  - Using a chemical deposition process (CVD etc)
- Etching:
  - Wet etching: uses acid or basic solutions
  - Dry etching: uses plasma (like sandblasting…)
- Planarization
  - Surfaces must be flat
  - Chemical Mechanical Polishing (CMP) before deposition

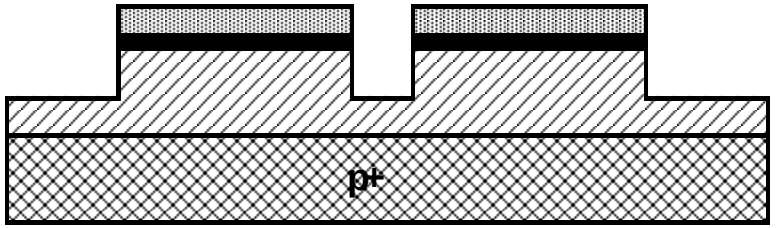
CMOS Process Walk-Through



(a) Base material: p+ substrate with p-epi layer

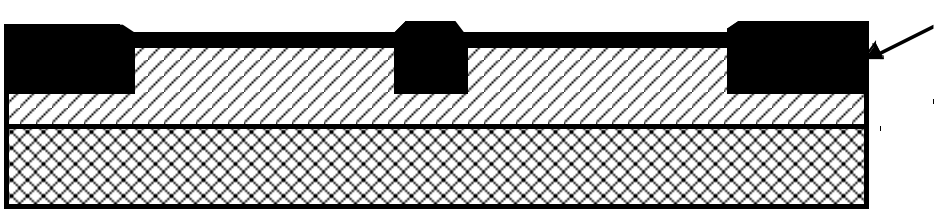


(b) After deposition of gate-oxide and sacrificial nitride (acts as a buffer layer)

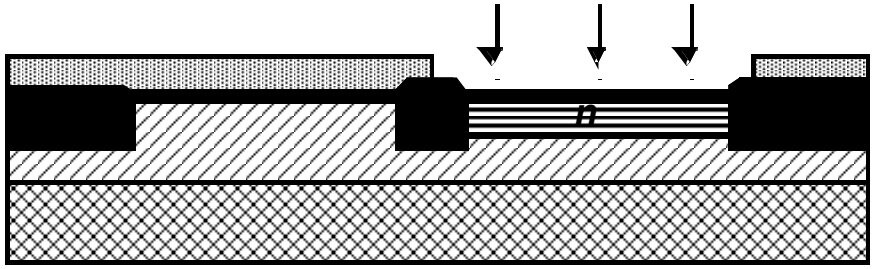


(c) After plasma etch of insulating trenches using the inverse of the active area mask

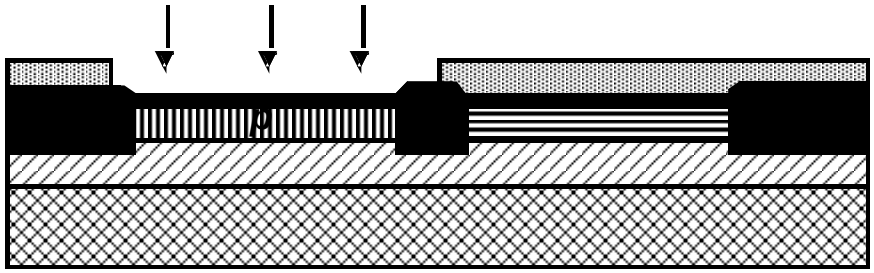
CMOS Process Walk-Through



(d) After trench filling, CMP planarization, and removal of sacrificial nitride

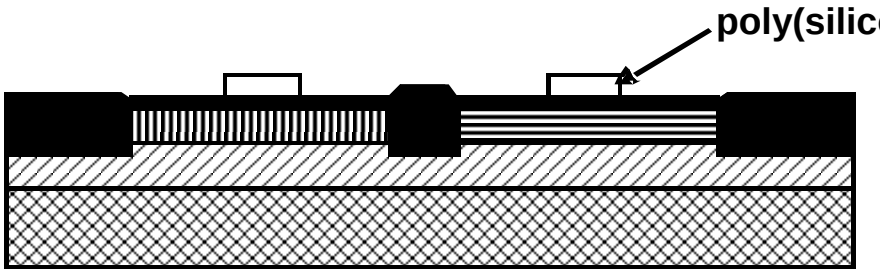


(e) After n-well and V_{Tp} adjust implants

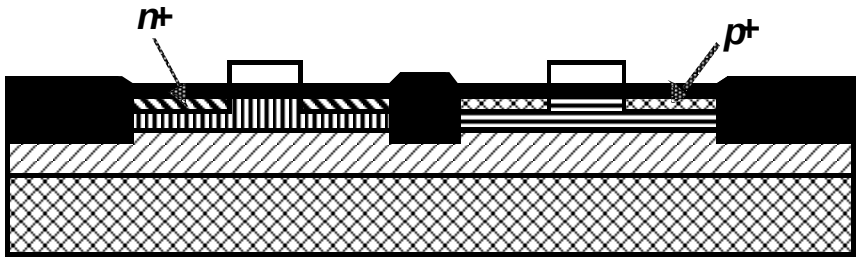


(f) After p-well and V_{Tn} adjust implants

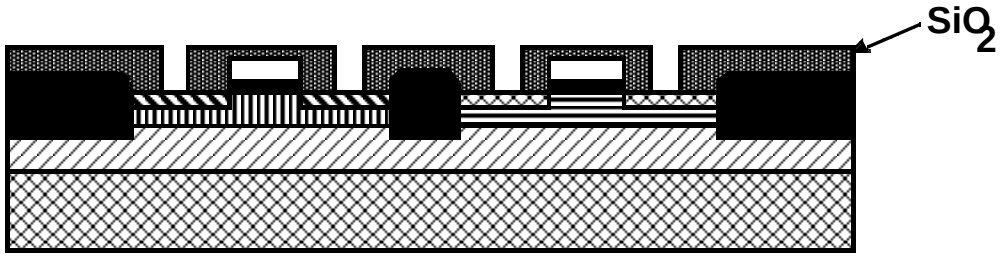
CMOS Process Walk-Through



(g) After polysilicon deposition and etch

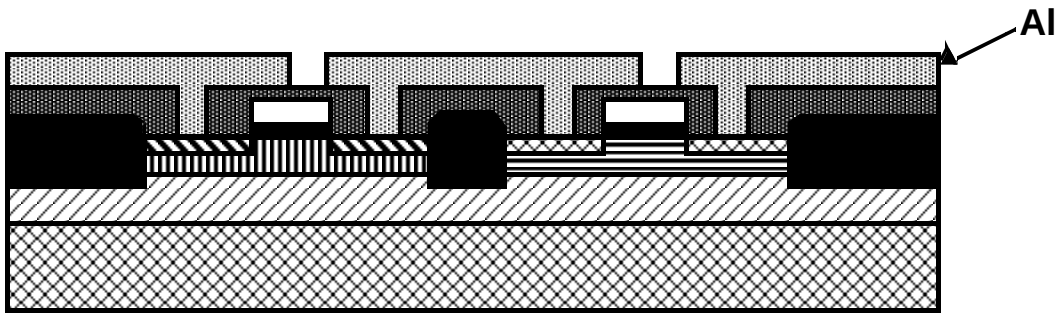


(h) After *n*+ source/drain and *p*+ source/drain implants. These steps also dope the polysilicon.

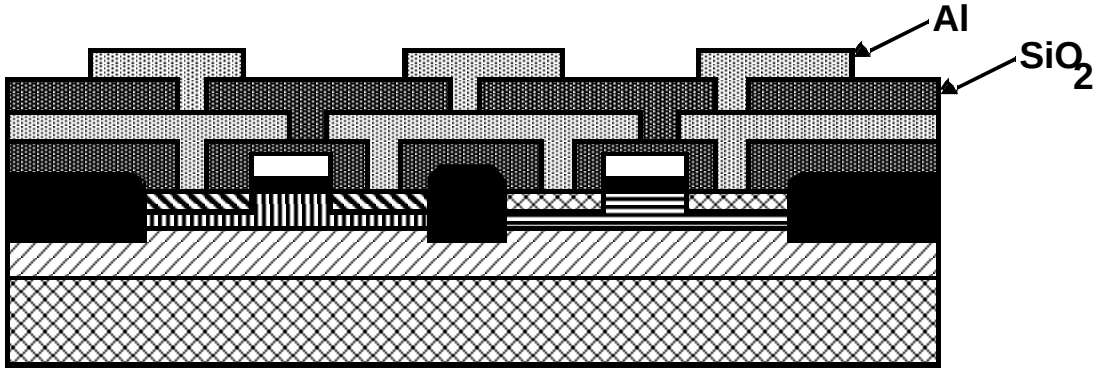


(i) After deposition of SiO_2 insulator and contact hole etch.

CMOS Process Walk-Through



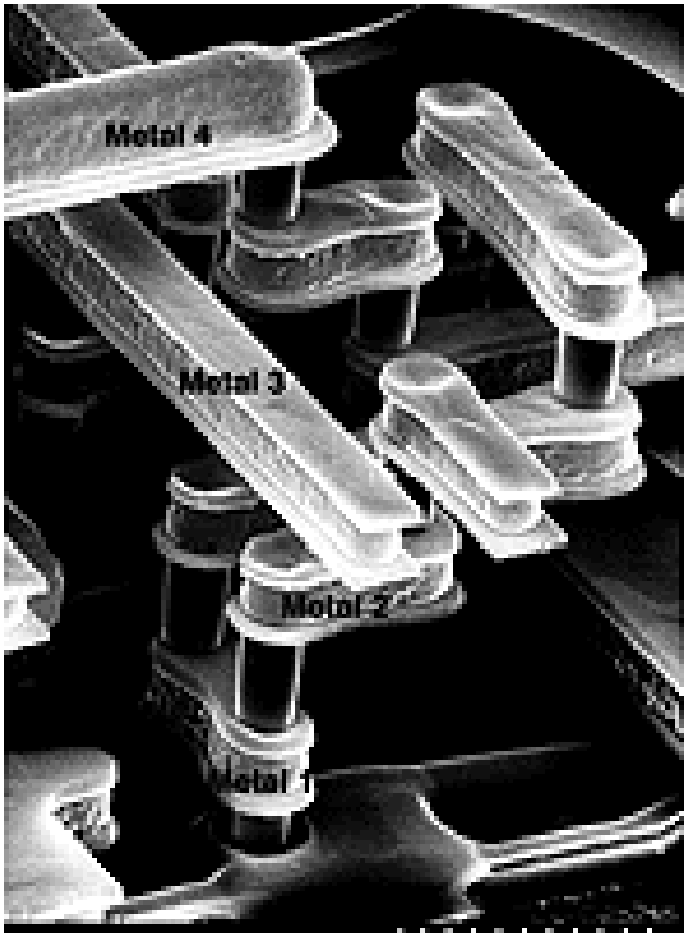
(j) After deposition and patterning of first Al layer.



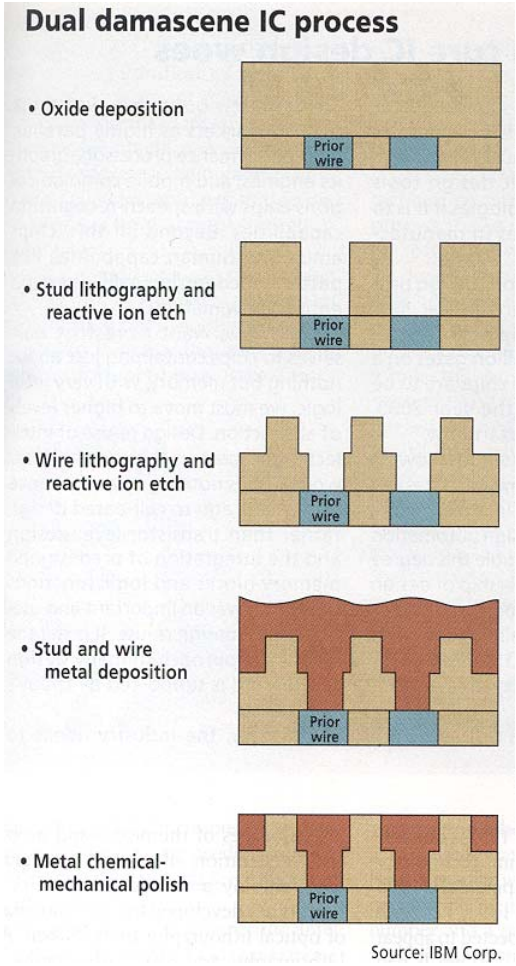
(k) After deposition of SiO_2 insulator, etching of via's, deposition and patterning of second layer of Al.

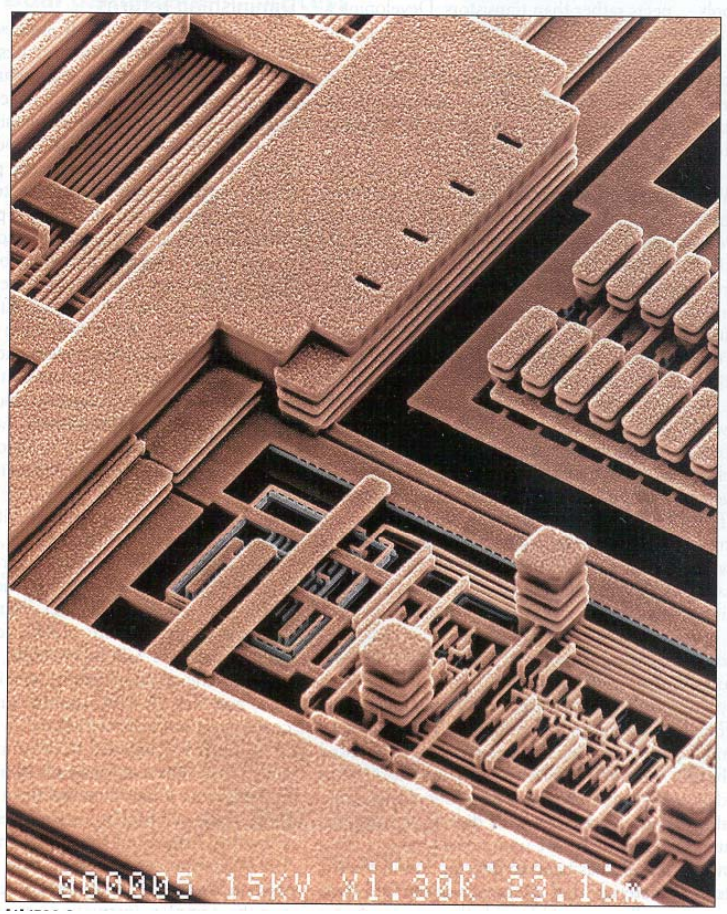
Advanced Metallization

Older (prior to 1997) VLSI interconnect technology: used AlCu for lines and W for vias….

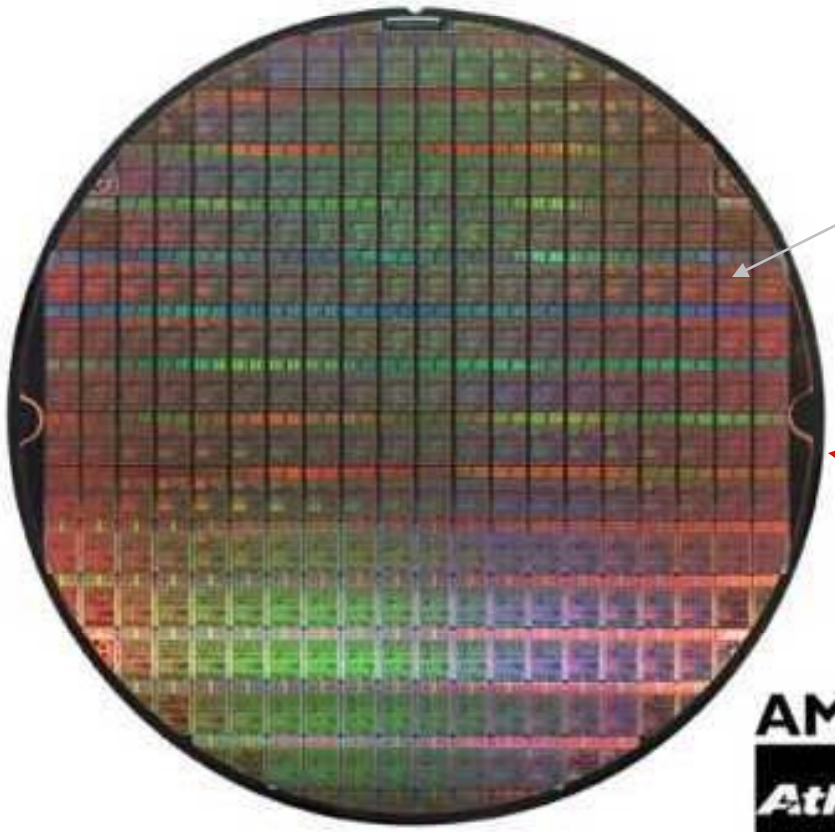


Advanced Metallization: Cu based





Fully Processed Wafer

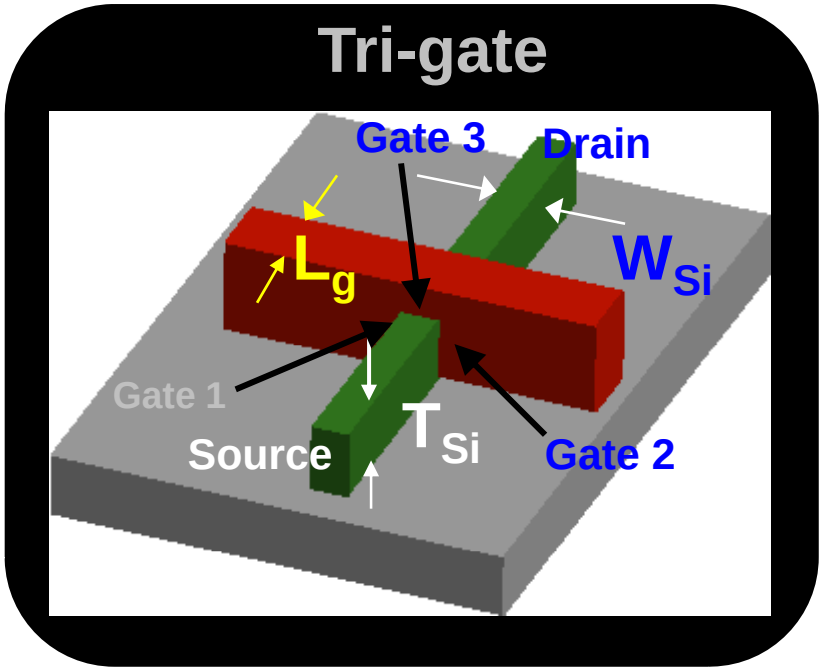


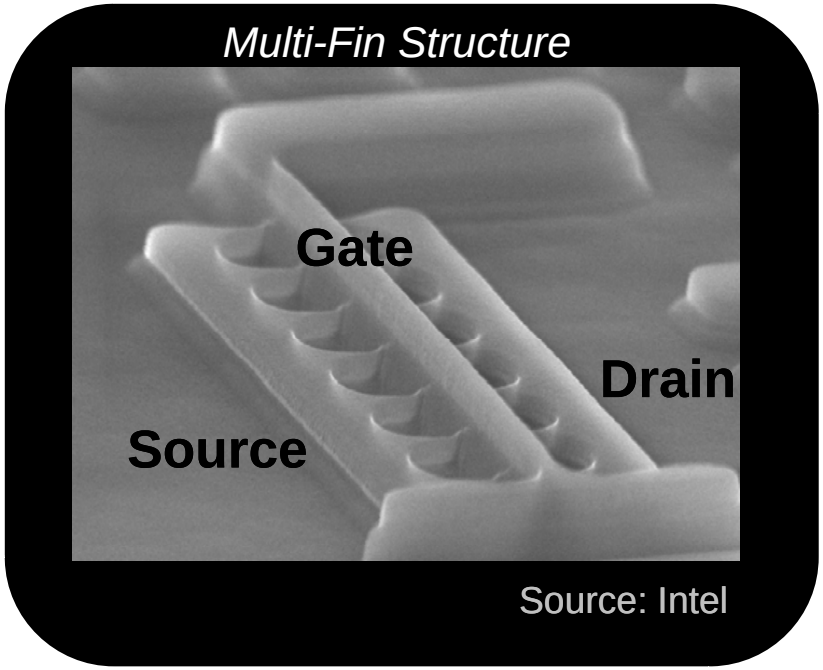
Going up to 12" (30cm)

From http://www.amd.com

New Transistors: Double Gate FETs

(FinFETs—Berkeley; Tri-Gate---Intel)





Improved short-channel effects
Higher ON current for lower SD Leakage

Even better FETs: **i) Gate-All-Around FETs--- ultimate case is GAA Si Nanowire FET or ii) Carbon Nanotube FETs (back-gated or top-gated structures)**