ECE 124A
VLSI Principles
Lecture 5

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Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: Minimum line width
  - scalable design rules: lambda parameter
  - absolute dimensions (micron rules)
- Design rules are also determined based on reliability and manufacturability issues

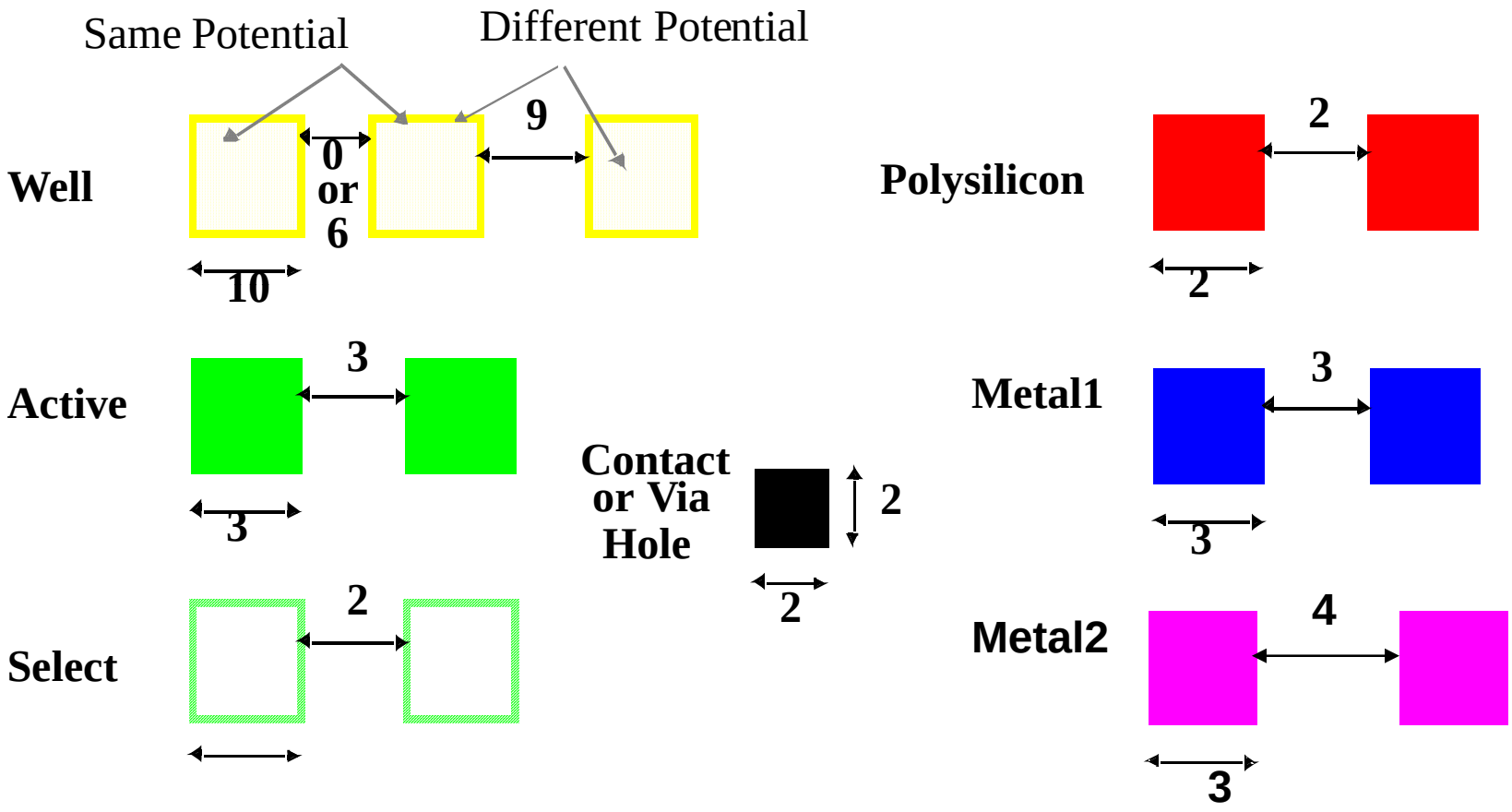
CMOS Process Layers

Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n+,p+)	Green	
Select (p+,n+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

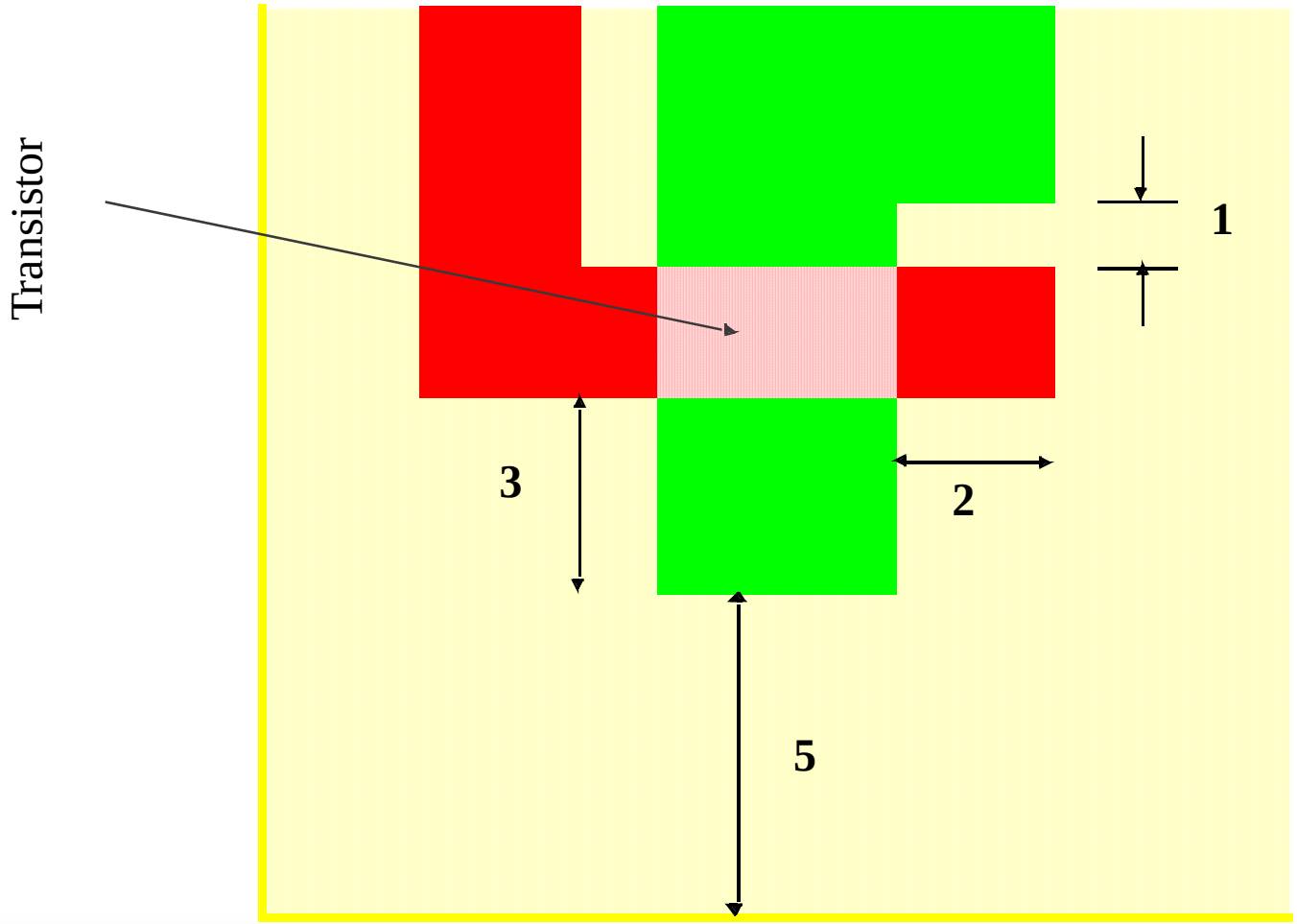
Layers in 0.25 μm CMOS process

Layer Description	Representation
metal	m1, m2, m3, m4, m5
well	nw
polysilicon	poly
contacts & vias	ct, v12,v23,v34,v45, nwc, pwc
active area and FETs	ndif, pdif, nfet, pfet
select	nplus, pplus, prb

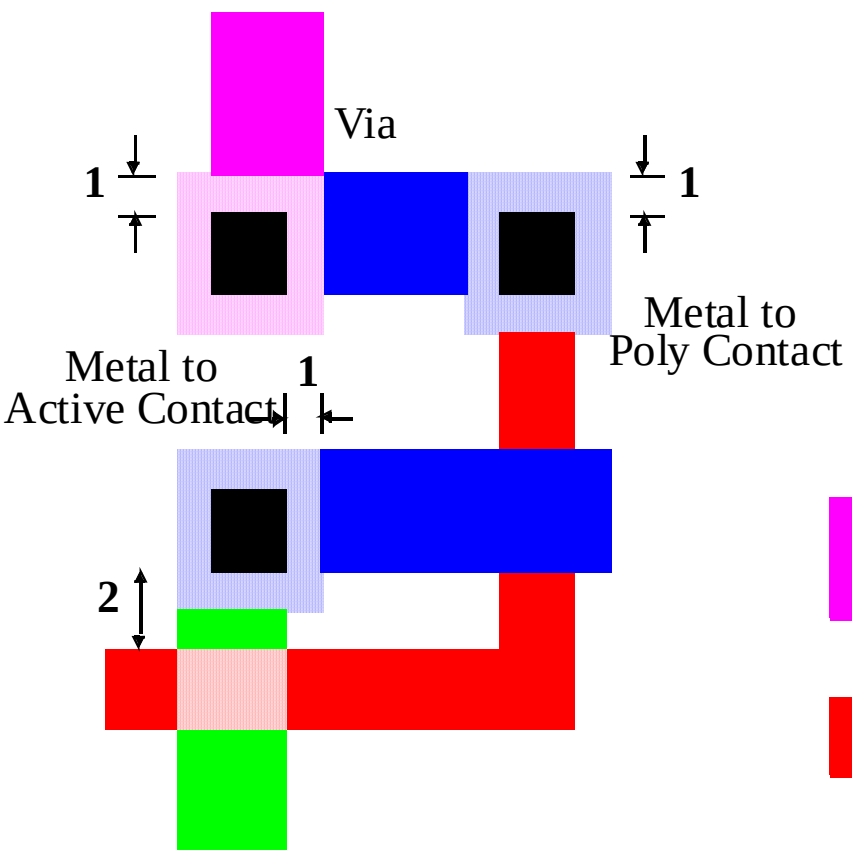
Intra-Layer Design Rules

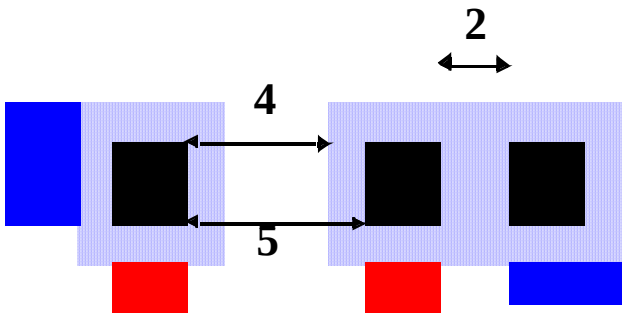


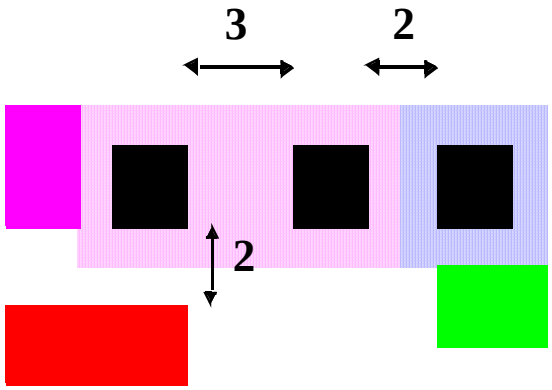
Transistor Layout



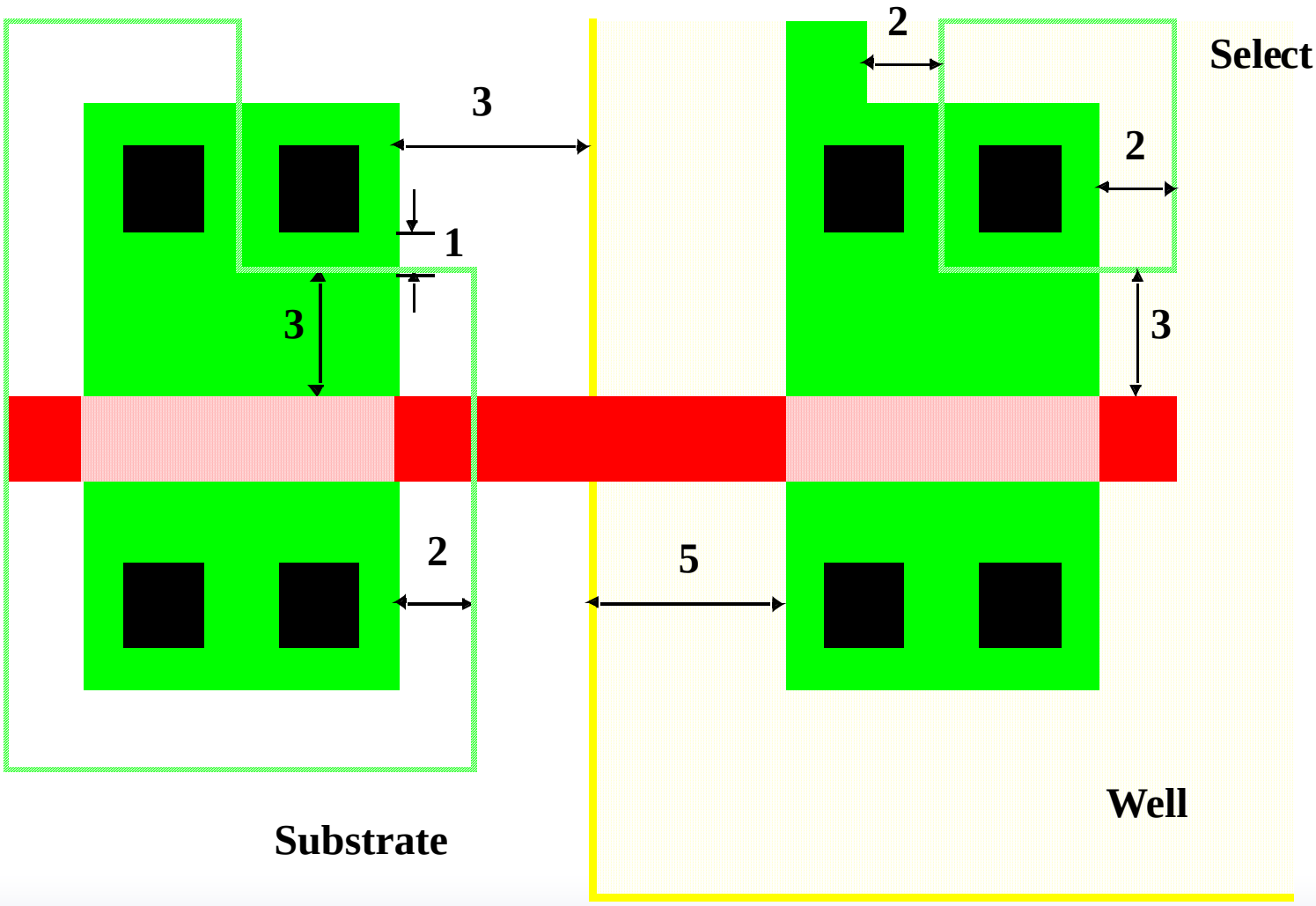
Vias and Contacts



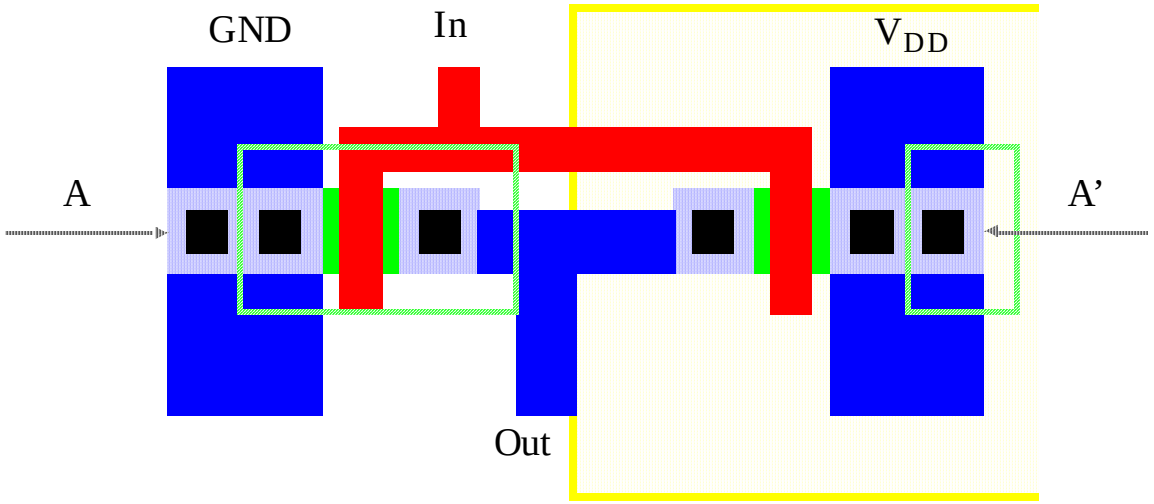




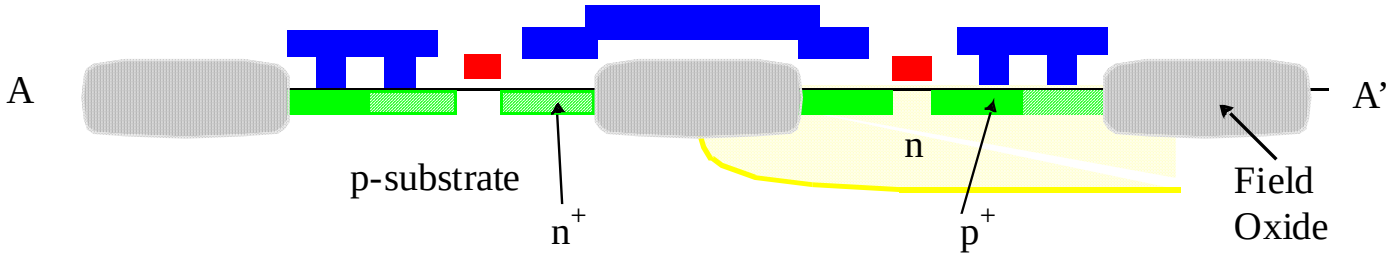
Select Layer….an interface for generating the mask



CMOS Inverter Layout

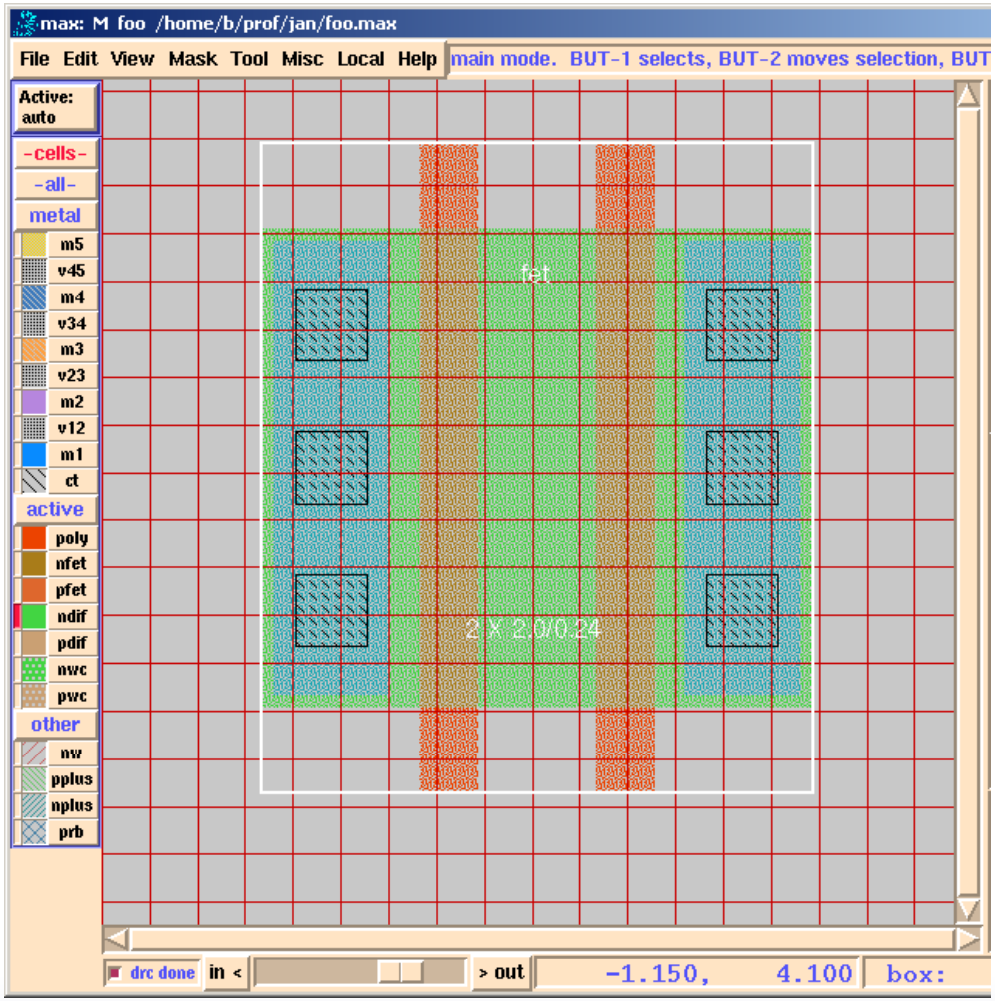


(a) Layout

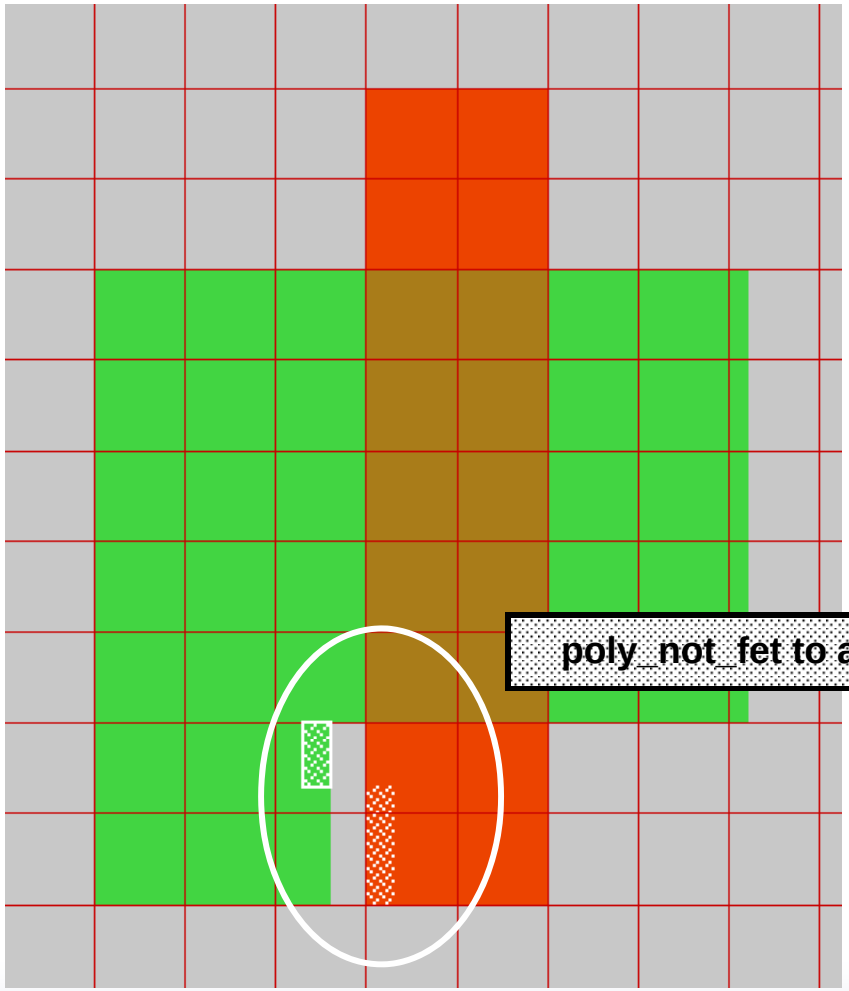


(b) Cross-Section along A-A'

Layout Editor….MAX

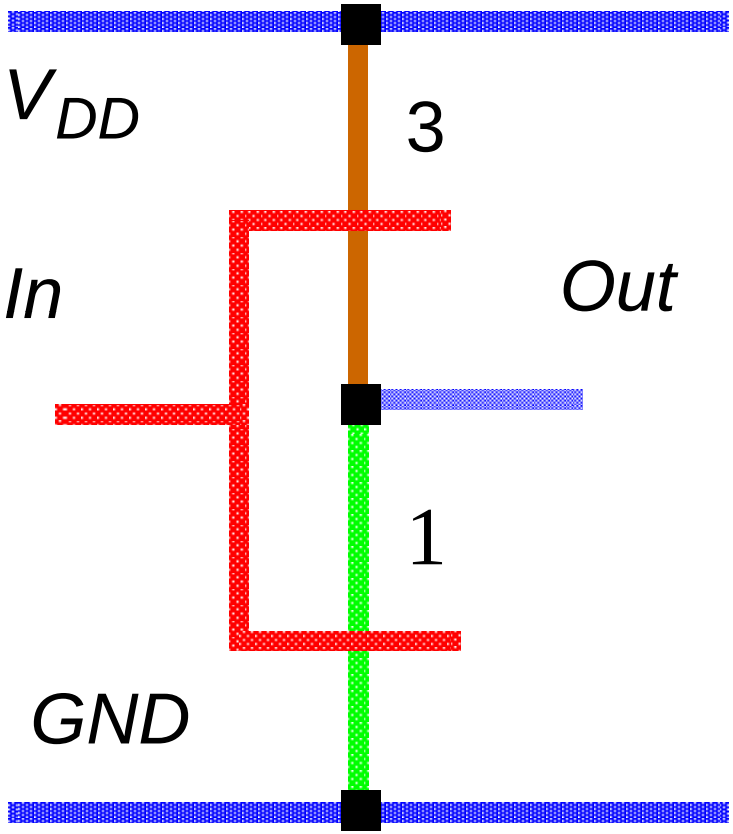


Design Rule Checker



poly_not_fet to all_diff minimum spacing = 0.14 um.

Stick Diagram….see Section 1.5.5 in text

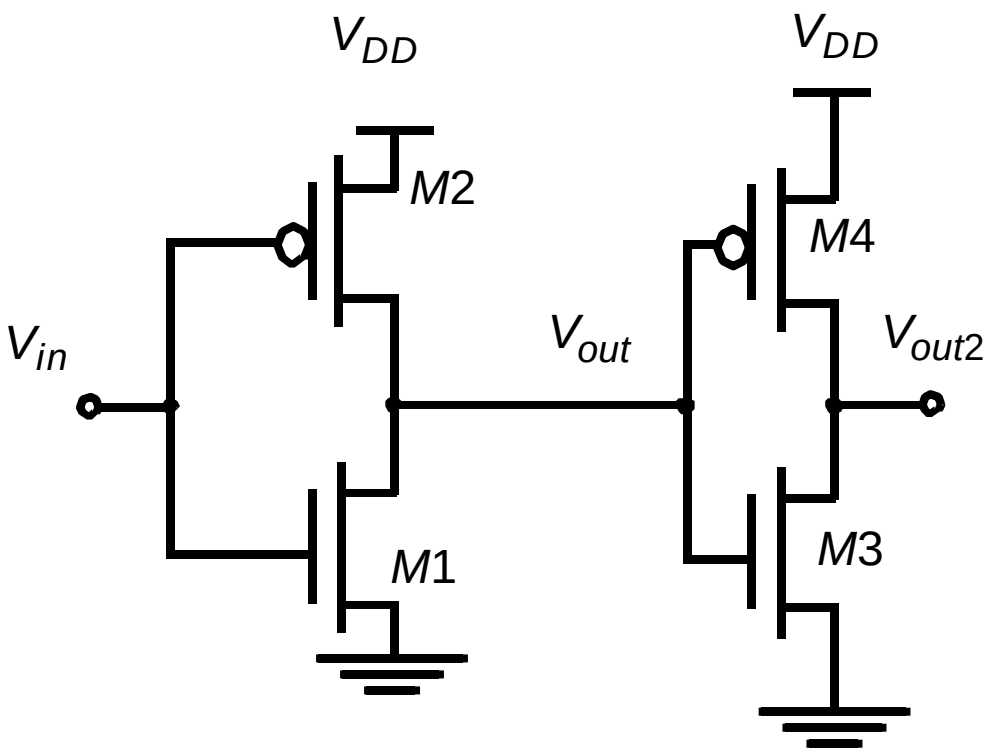


Stick diagram of inverter

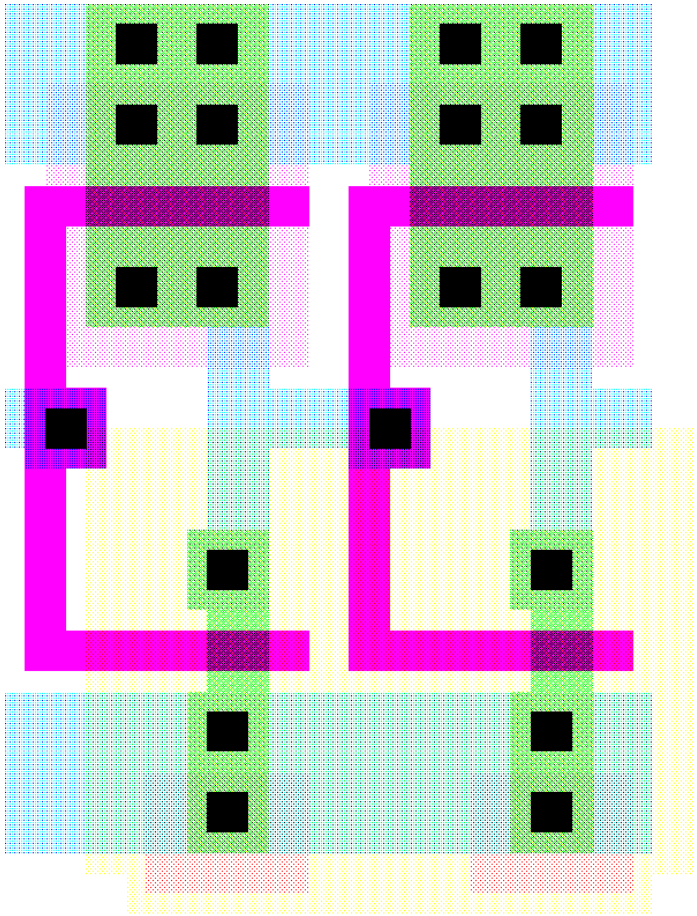
Allows quick layout planning & area estimation without detailed layout

- Dimensionless layout entities
- Only topology is important
- Determine height and width of cell by counting number of wire tracks and multiplying by wire pitch (width+spacing)
- Final layout generated by "compaction" program

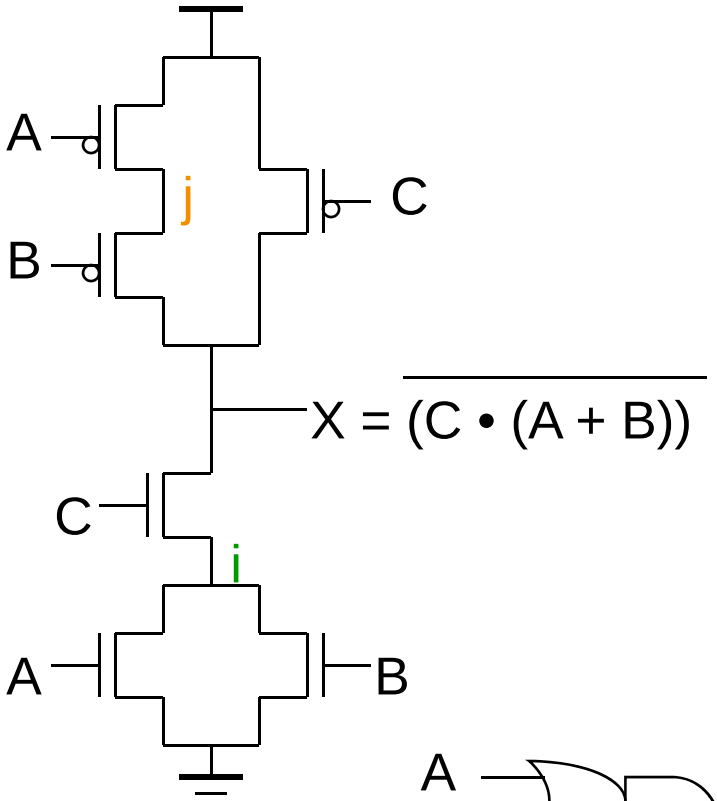
Circuit Under Design

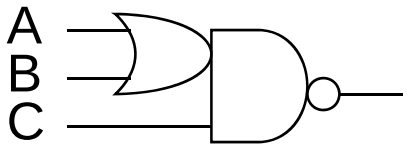


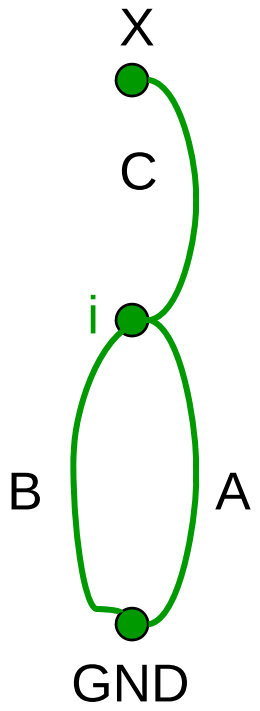
Its Layout View



Logic Graph

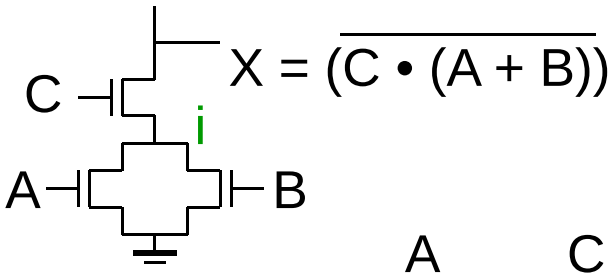


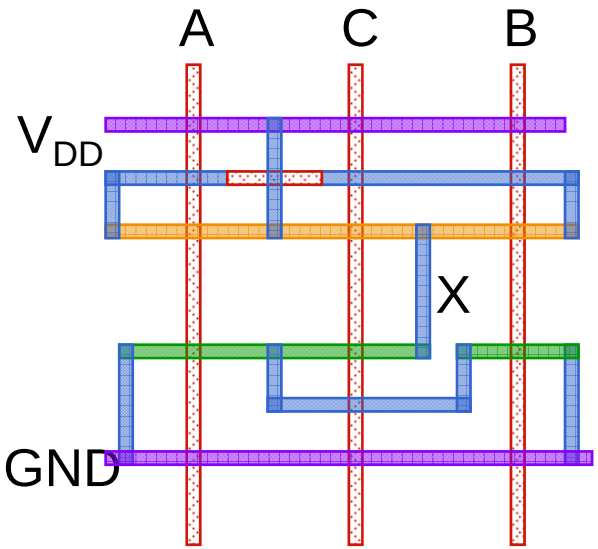


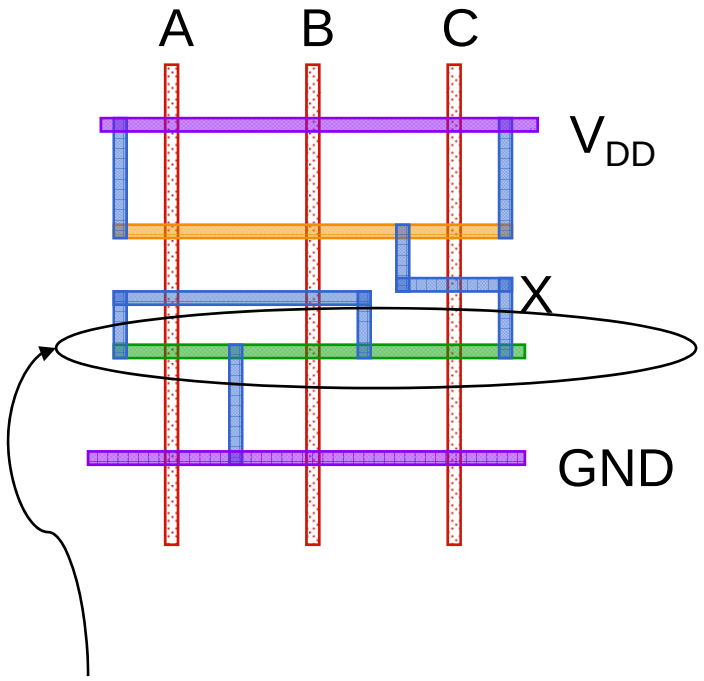


PDN

Two Stick Layouts of $\overline{(C \bullet (A + B))}$



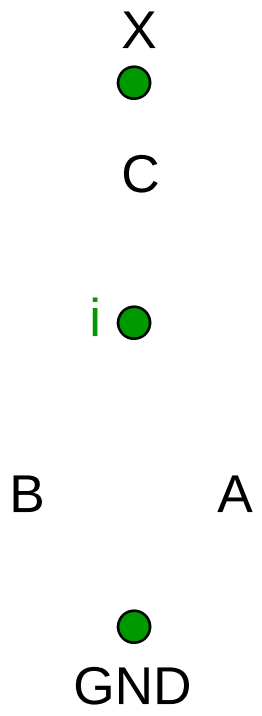




uninterrupted diffusion strip

Consistent Euler Path

- An uninterrupted diffusion strip is possible only if there exists a Euler path in the logic graph
  - Euler path: a path through all nodes in the graph such that each edge is visited once and only once.



- For a single poly strip for every input signal, the Euler paths in the PUN and PDN must be consistent (the same)

Consistent Euler Path

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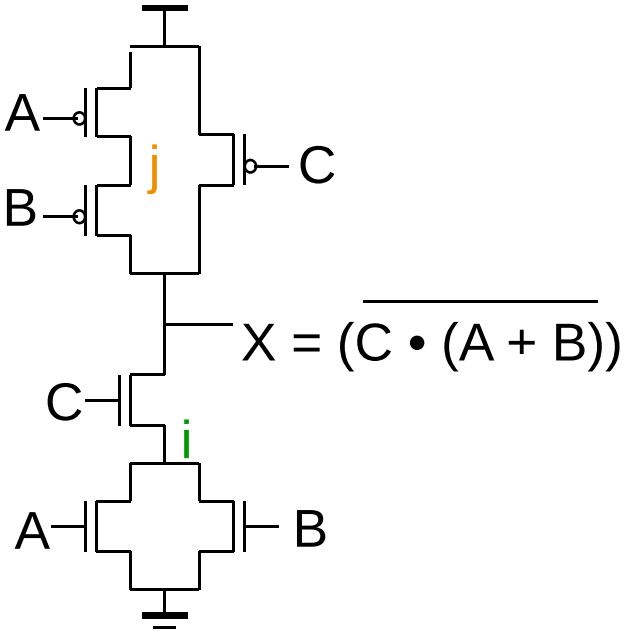
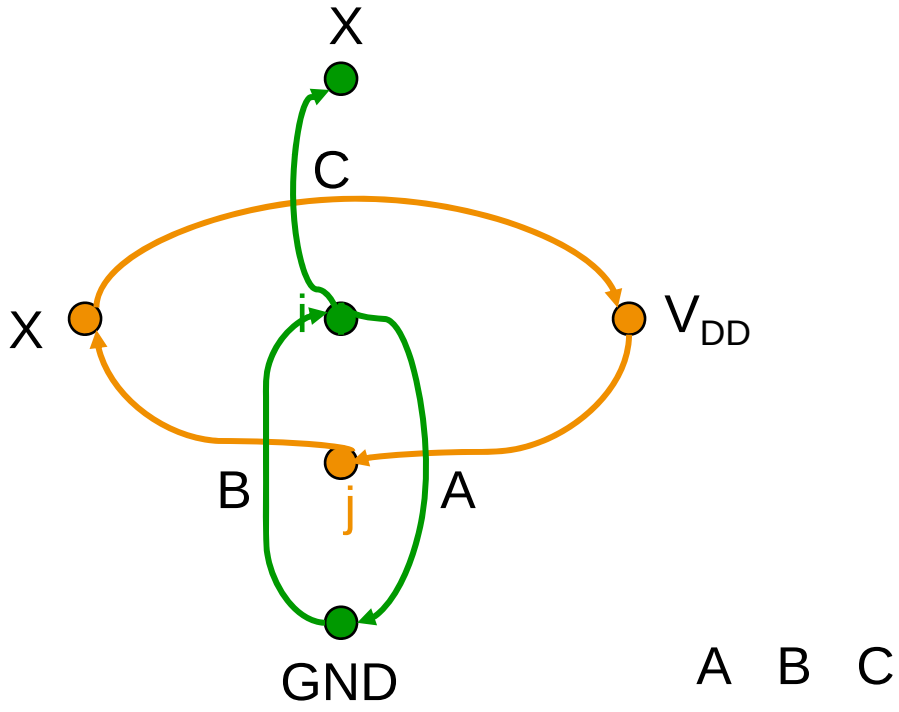


$$X = \overline{(C \bullet (A + B))}$$



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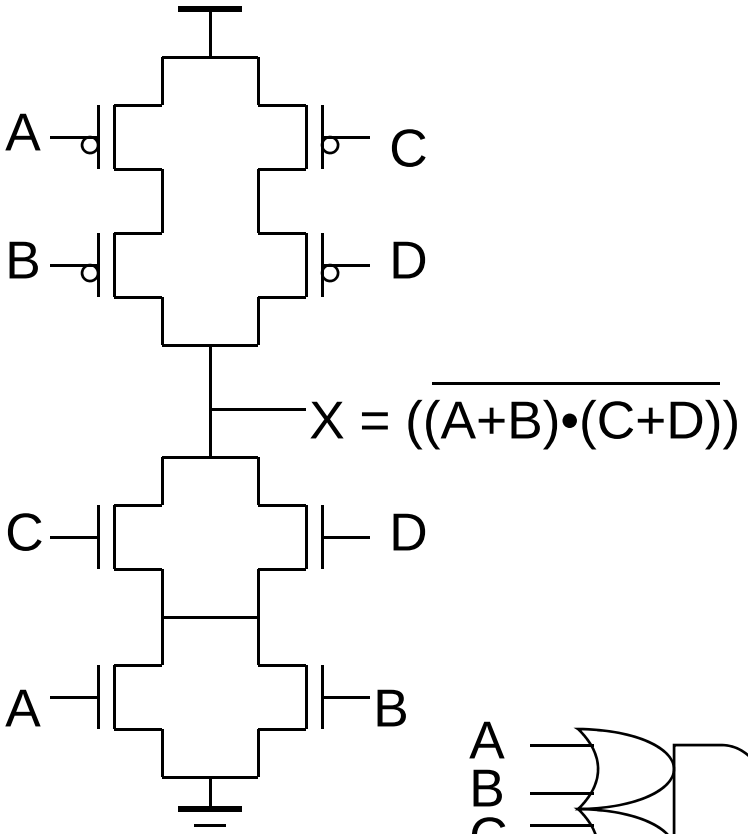
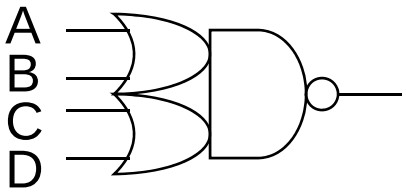
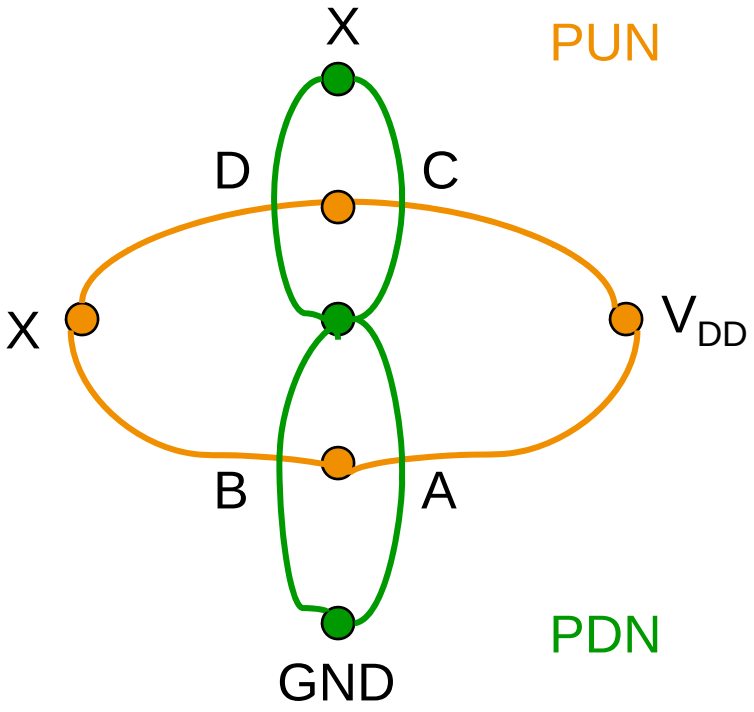
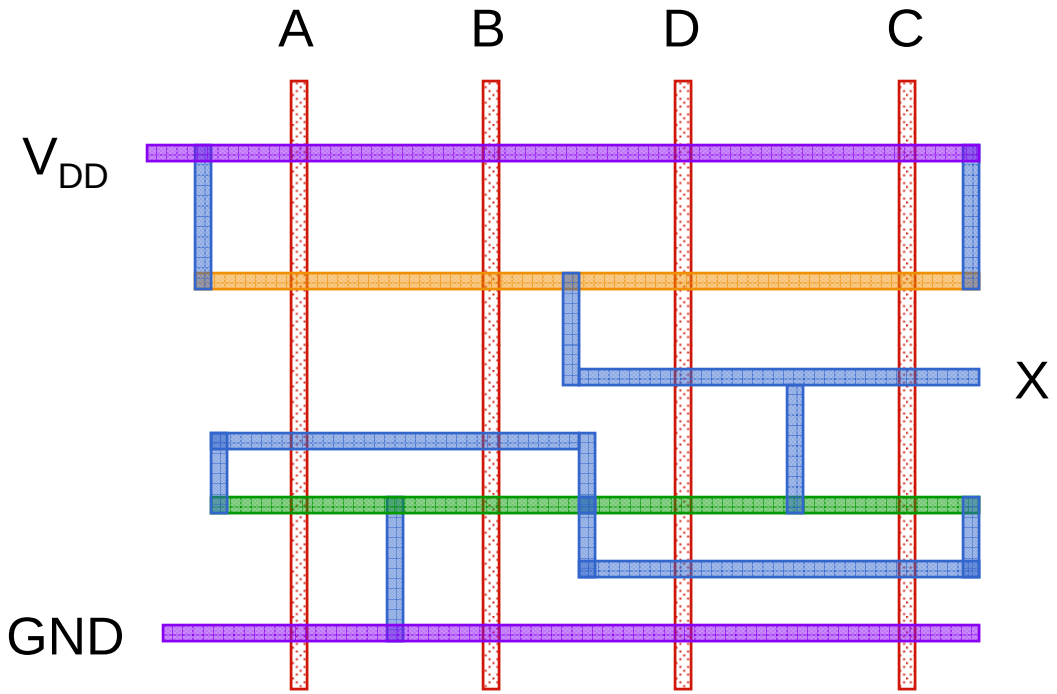
Logic Graph







Layout



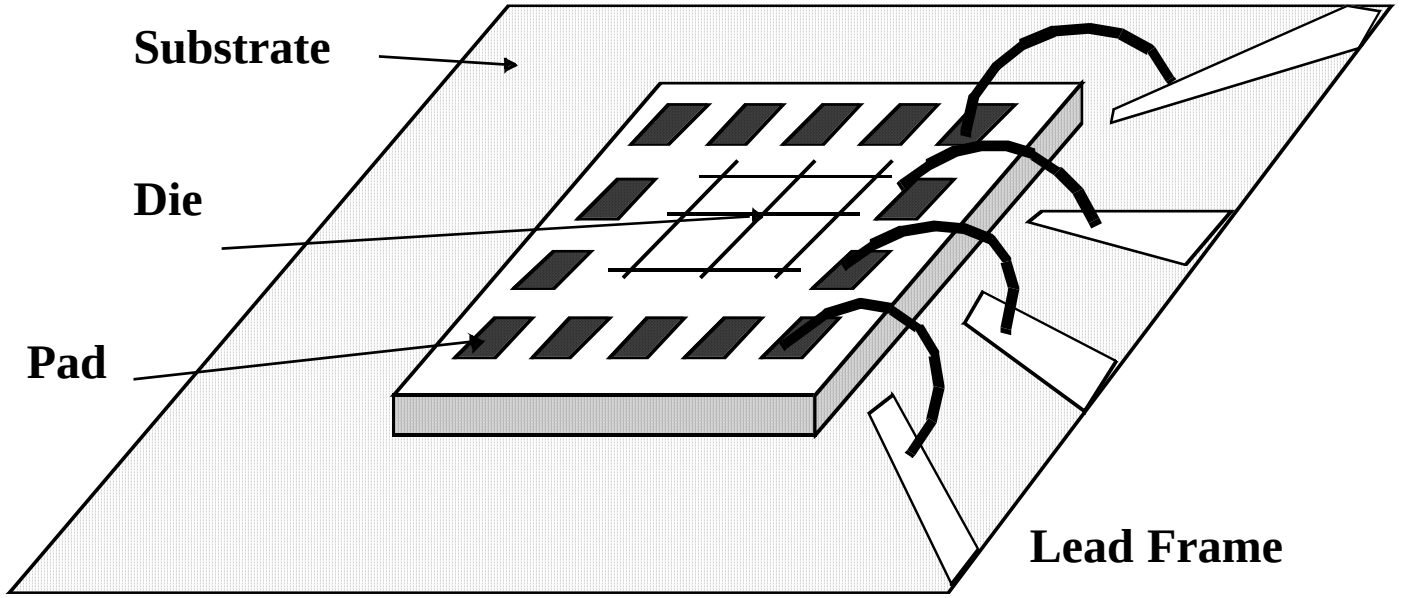
$$X = \overline{((A+B)\bullet(C+D))}$$

Packaging Requirements

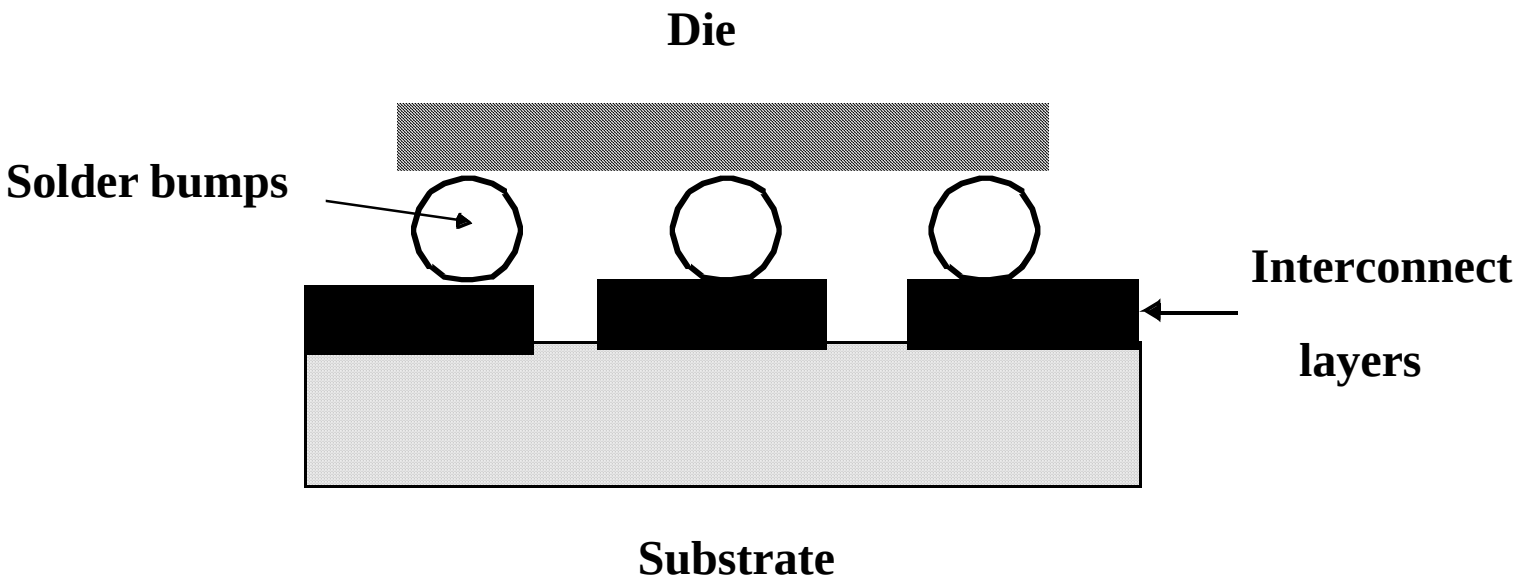
- **Electrical: Low parasitics**
- **Mechanical: Reliable and robust**
- **Thermal: Efficient heat removal**
- **Economical: Cheap**

Bonding Techniques

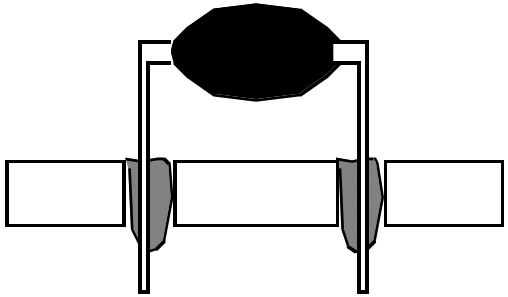
Wire Bonding



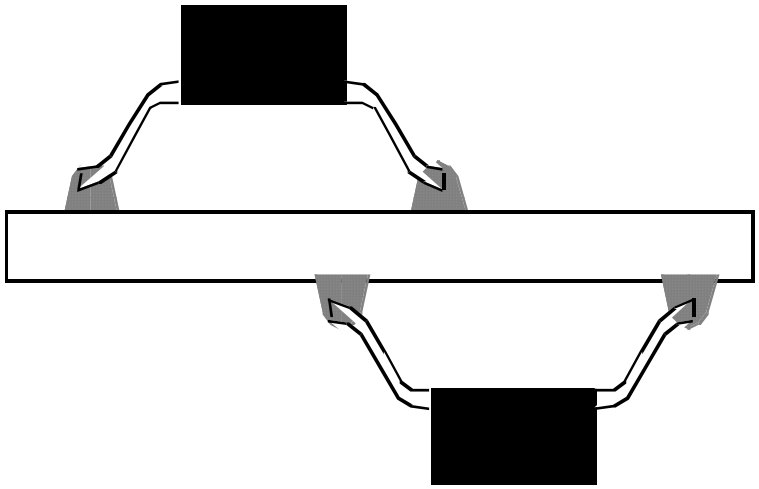
Flip-Chip Bonding



Package-to-Board Interconnect



(a) Through-Hole Mounting



(b) Surface Mount

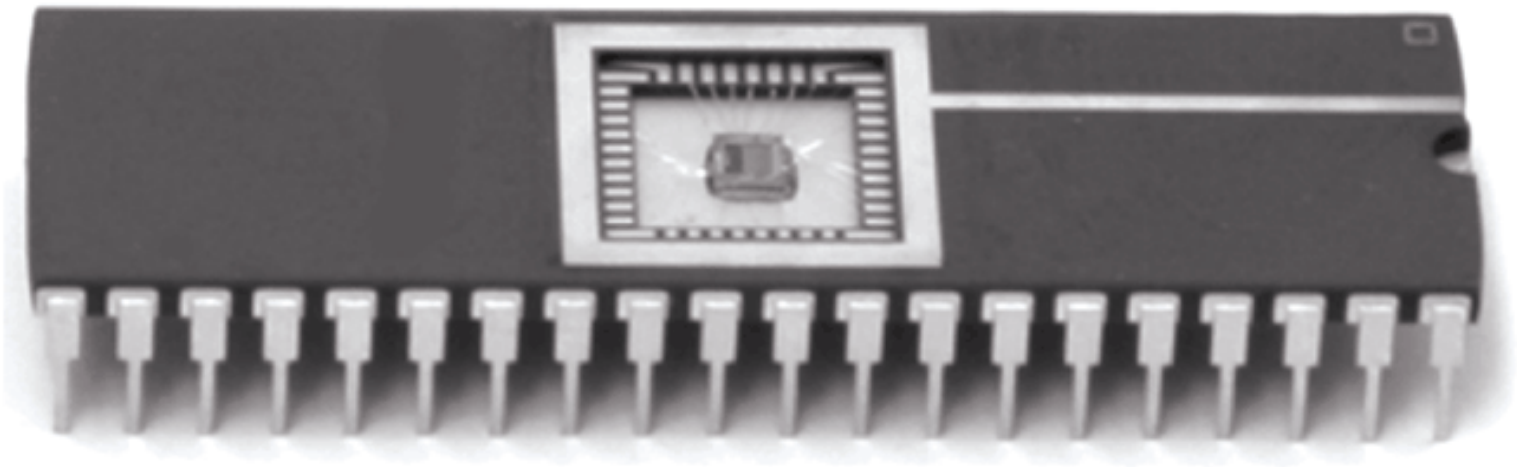
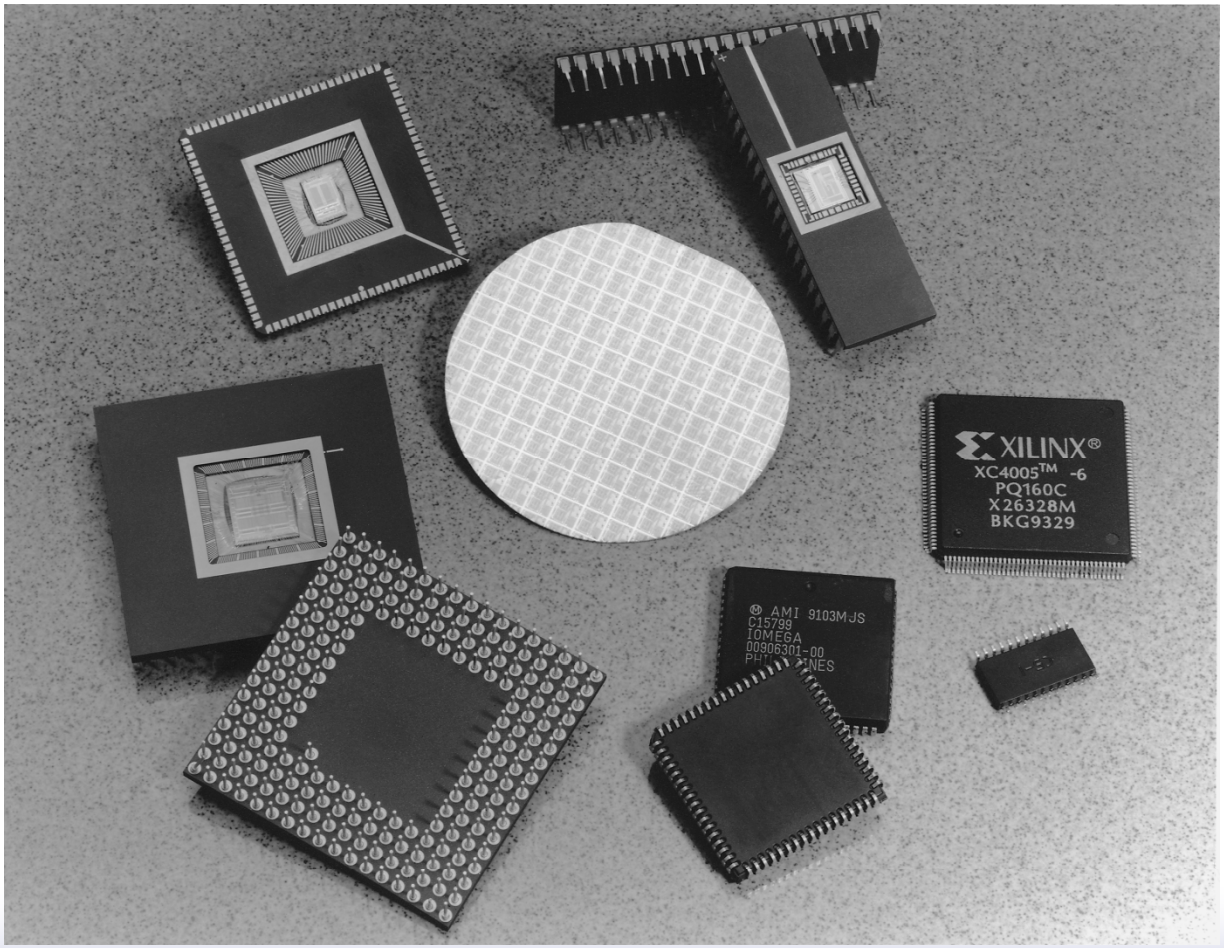


FIG 1.71 Chip in a 40-pin dual-inline package

Package Types



Package Parameters

Package Type	Capacitance (pF)	Inductance (nH)
68 Pin Plastic DIP	4	35
68 Pin Ceramic DIP	7	20
256 Pin Pin Grid Array	5	15
Wire Bond	1	1
Solder Bump	0.5	0.1

Typical Capacitances and Inductances of Various Package and Bonding Styles (from [Sze83])

Multi-Chip Modules