ECE 225
High Speed Digital IC Design
Lecture 1

Introduction:
Nanometer Scale CMOS Issues & Emerging Technologies for VLSI

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Course Description….

- Advanced digital CMOS design concepts
- Nanometer scale issues in VLSI
  - CMOS scaling, nanoscale issues including variability, power and thermal management, interconnects, reliability, aging
- Emerging Technologies for VLSI
  - Classical and non-classical CMOS
  - Non-Si device and interconnect technologies

Textbook and References

- Reference Books
  - Modern VLSI Devices by Yuan Taur and Tak Ning, Cambridge Univ. Press, Second edition, 2009.
  - Design of High-Performance Microprocessor Circuits, Chandrakasan, Bowhill and Fox (Eds.), IEEE Press, 2001.
  - Emerging Nanoelectronics: Life With and After CMOS, Eds. A. M. Ionescu and K. Banerjee, Springer, 2004.
  - Basic Reference: ECE 124A Text Book: CMOS VLSI Design: A Circuits and Systems Perspective (3rd Edition), Neil H. E. Weste and David Harris, Addison Wesley, © 2005.

Other Reference Materials

- To be posted on the class web site:
  http://www.ece.ucsb.edu/courses/ECE125/125_W11Banerjee/default.html

Prerequisites

- ECE124A or equivalent is recommended
- Basic Circuit Analysis (both analytical and simulation based)
- Other
  - Logic design
    - Combinational and clocked logic, Gates, latches, flip-flops, etc.
  - Fundamentals of electromagnetic theory (physics)
    - Resistance, capacitance, inductance, power/energy

Preparation for the course

- Computing environment and tools
  - Setup computer account, and the compute environment
  - Familiarize with the schematic and layout editors
  - Familiarize with the parasitic extractor and circuit simulator
- Theory
  - Review device physics (refer to ECE 124A lecture notes)
  - Review logic design, computer architecture, and electromagnetics
- Projects
  - You should start formalizing your project ASAP
  - **Must work on your own**

Review-I: Basic Understanding of the MOSFET

- *Band Diagrams*
- *I-V curves*
- *Static/dynamic behavior*
- *Parameters (process, temperature, voltage) that impact device behavior*
- *Impact on circuit parameters (delay, power, NM)*

Review-II: Implementation & Sizing of Complex Gates…

- *Described as: Boolean function, K-map, Truth Table, or propositions*
- *Sizing of gates to get equivalent inverter size (based on worst case delay) ---with and without considering internal capacitances*

Review-III: Circuit Level Implementation Choices for Complex gates

- *Implement a function F with*
  - *Static CMOS*
  - *Pass Transistors or transmission-gates*
  - *Pseudo-NMOS*
  - *Dynamic Logic (including Domino)*
- *Pros and Cons of each of the methods (in terms of delay, power, area, noise margins etc.)*

Review-IV: Elmore Delay

Know how to apply Elmore delay to find the delay between any two points in a:

- *Given RC tree*
- *Given topology of gates (find their equivalent RC…)*

Review-V: Optimization of a Design

- *Optimizing a design in terms of delay and power dissipation*
- *Choosing optimal number and sizes to minimize the delay for*
  - *Inverter chain*
  - *Gates (Logical Effort)*
- *Trade-off between delay and power dissipation*

Review-VI: Sequential Circuits

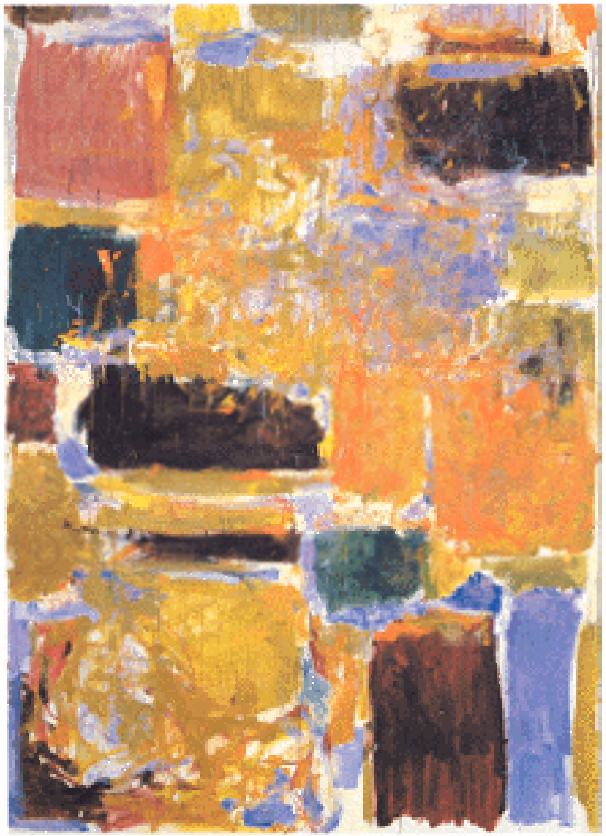
- *Design of foreground memory elements*
  - *Latches*
  - *Filp Flops*
- *Timing parameters (understand in terms of circuit design and topology)*
  - *setup time*
  - *hold time*
  - *clock skew*

Review-VII: Semiconductor Memories

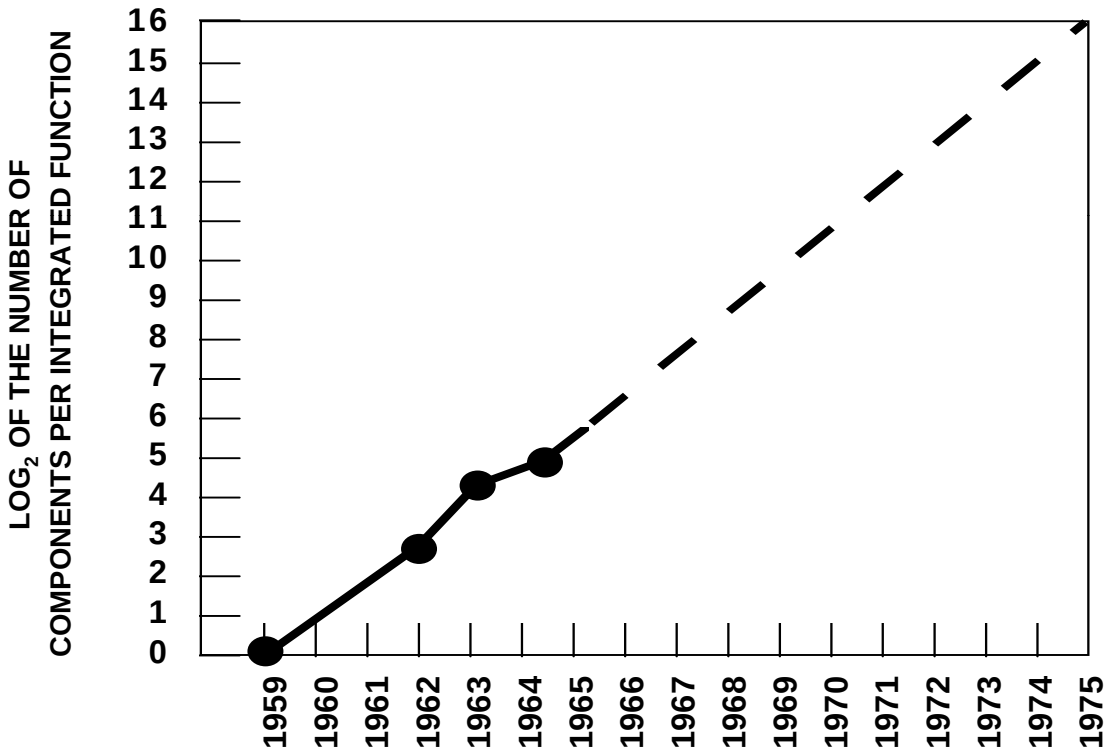
- *Basic Types*
- *SRAM (circuit level implementation…., read and write operations, sizing issues)*
- *DRAM (circuit level implementation, read and write operations, processing issues)*

Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in future?

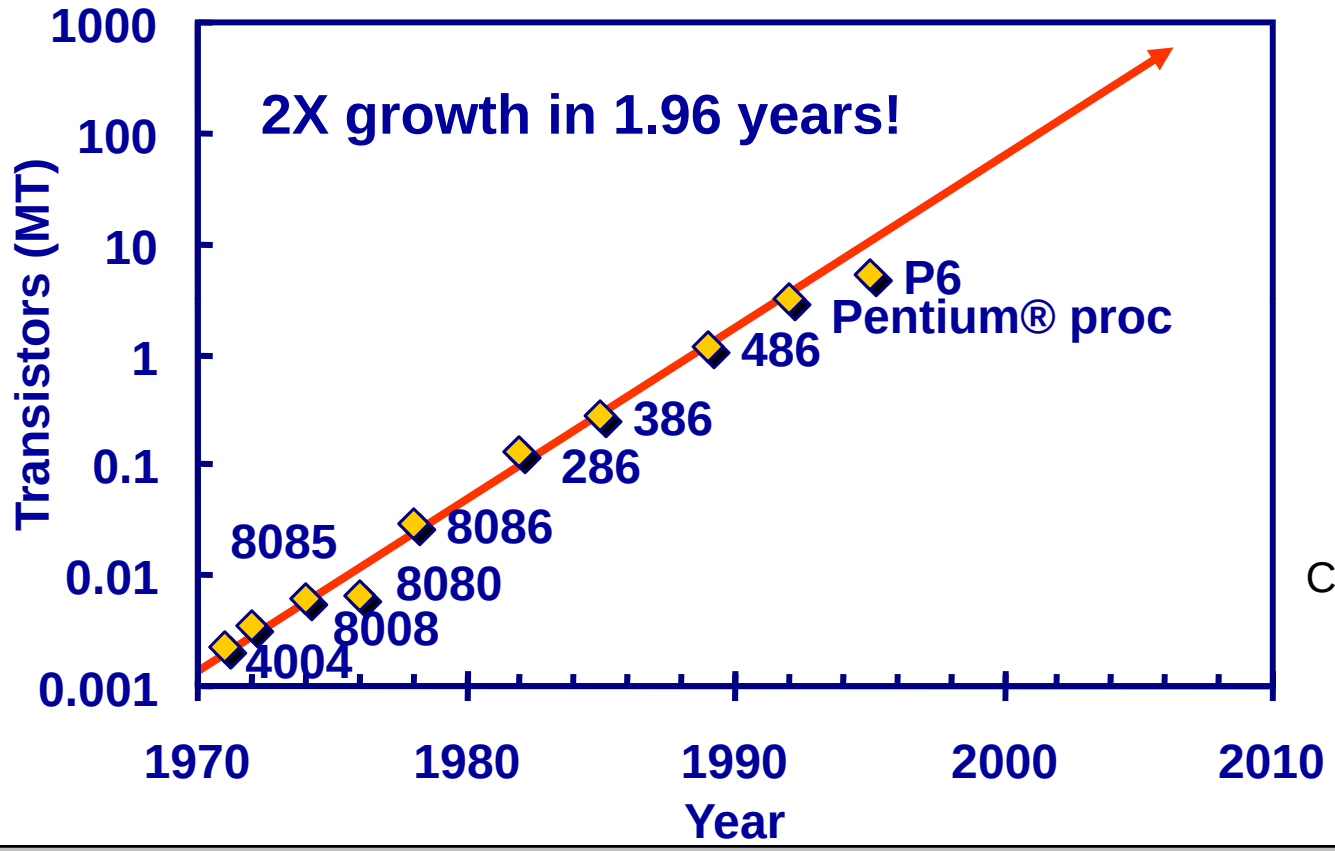


Moore's Law



Electronics, April 19, 1965.

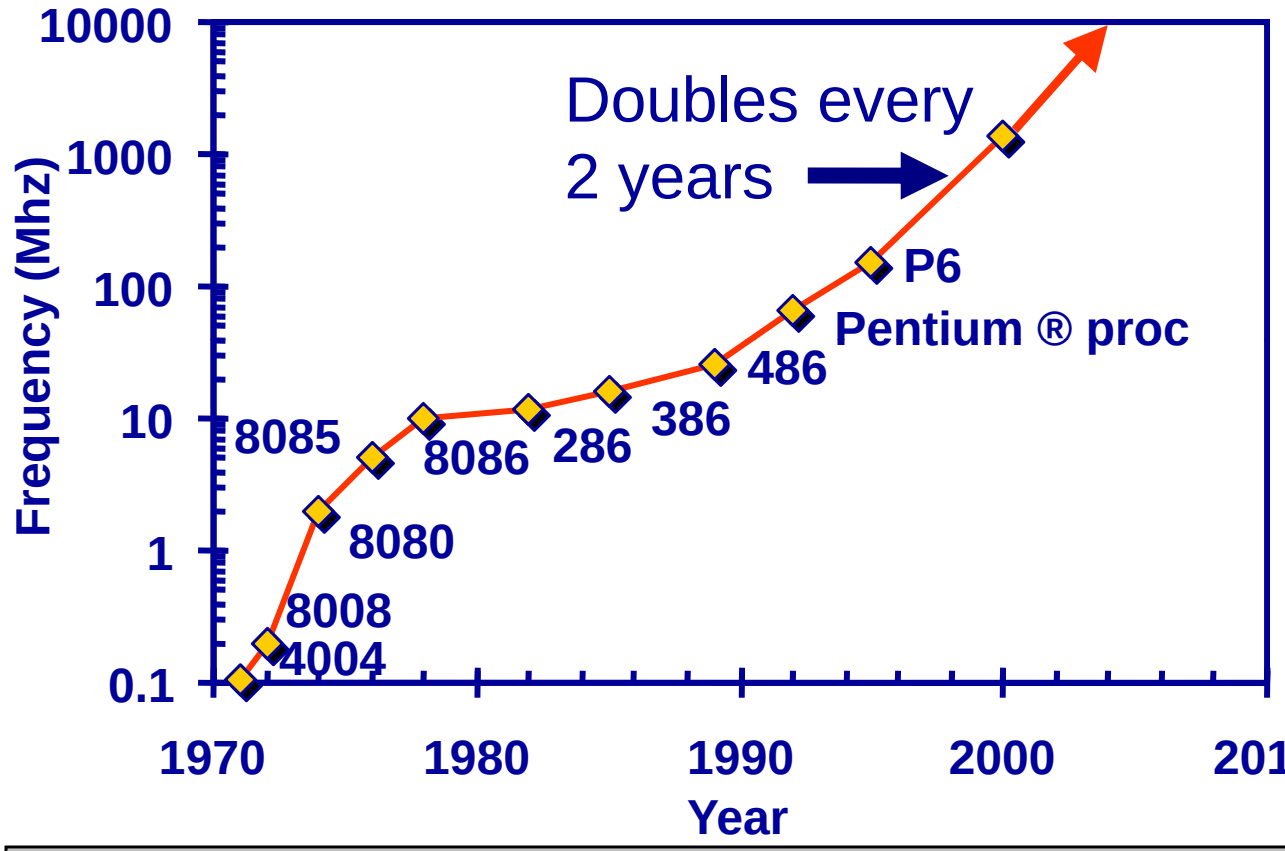
Moore's law in Microprocessors



Courtesy, Intel

Transistors on Lead Microprocessors double every 2 years

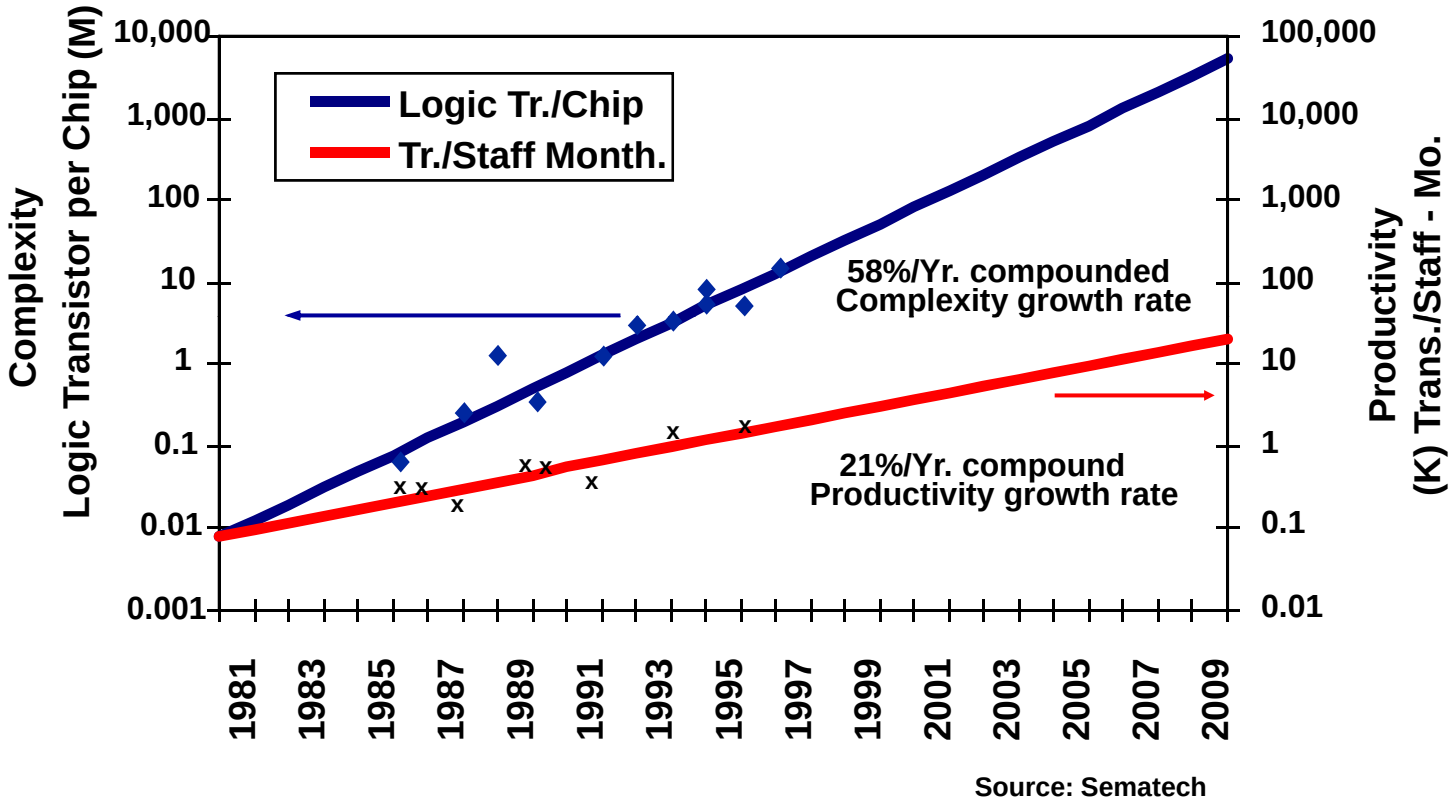
Frequency



Courtesy, Intel

Lead Microprocessors frequency doubles every 2 years

Productivity Trends



Complexity outpaces design productivity

Courtesy, ITRS Roadmap

Challenges in Digital Design

∝ DSM

"Microscopic Problems"

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

∝ 1/DSM

"Macroscopic Issues"

- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

Everything Looks a Little Different

?

…and There's a Lot of Them!

VLSI Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Robustness
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

VLSI Designer's Tasks

- Job of VLSI designer: design a circuit block to meet one or more objectives:
  - Maximize speed, performance
  - Minimize power consumption
  - Minimize area
  - Noise immunity (robustness)
- How?
  - Choice of circuit style (static, dynamic, etc)
  - Circuit design, transistor sizing
  - Interconnect design, efficient layout

VLSI Design Challenges

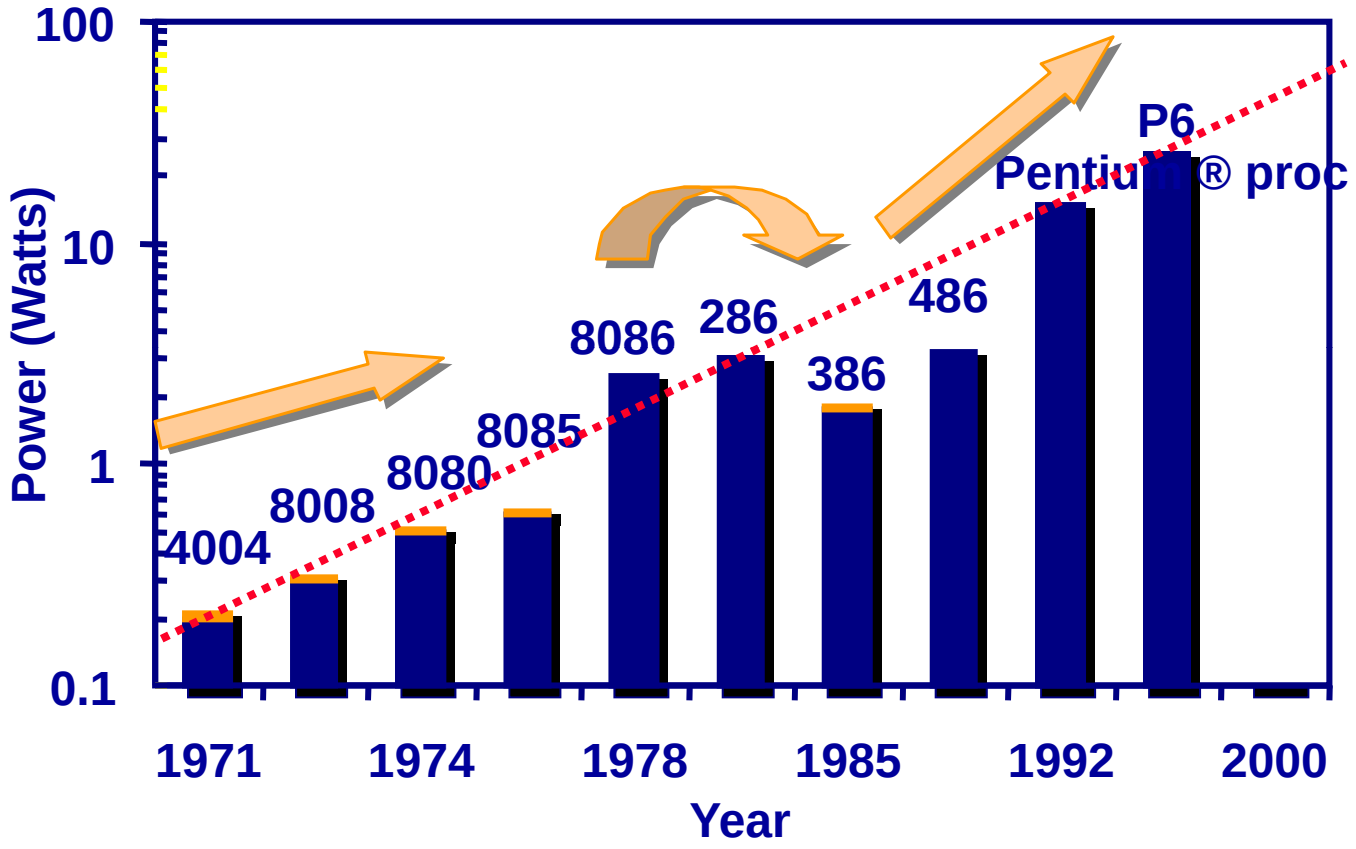
- design challenges
  - Power consumption, especially leakage power. Also affects chip cooling.
  - Noise issues, as transistors and wires move closer together. Design of noise-tolerant circuits.
  - Clocking: distributing high-frequency clock with minimum of skew (difference in clock arrival time between points on a chip)
  - Reliability issues such as electromigration, NBTI, TDDB, and ESD

Variability affects all of the above…..

VLSI Design Challenges

- design challenges (continued)
  - Scaling: continue to make transistors smaller. Why? Smaller transistors are faster, can put more transistors on a die
  - Integration: combining large VLSI systems to form a “system-on-a-chip”
    - Design for reuse
    - Design for testability
    - Advanced CAD tools required

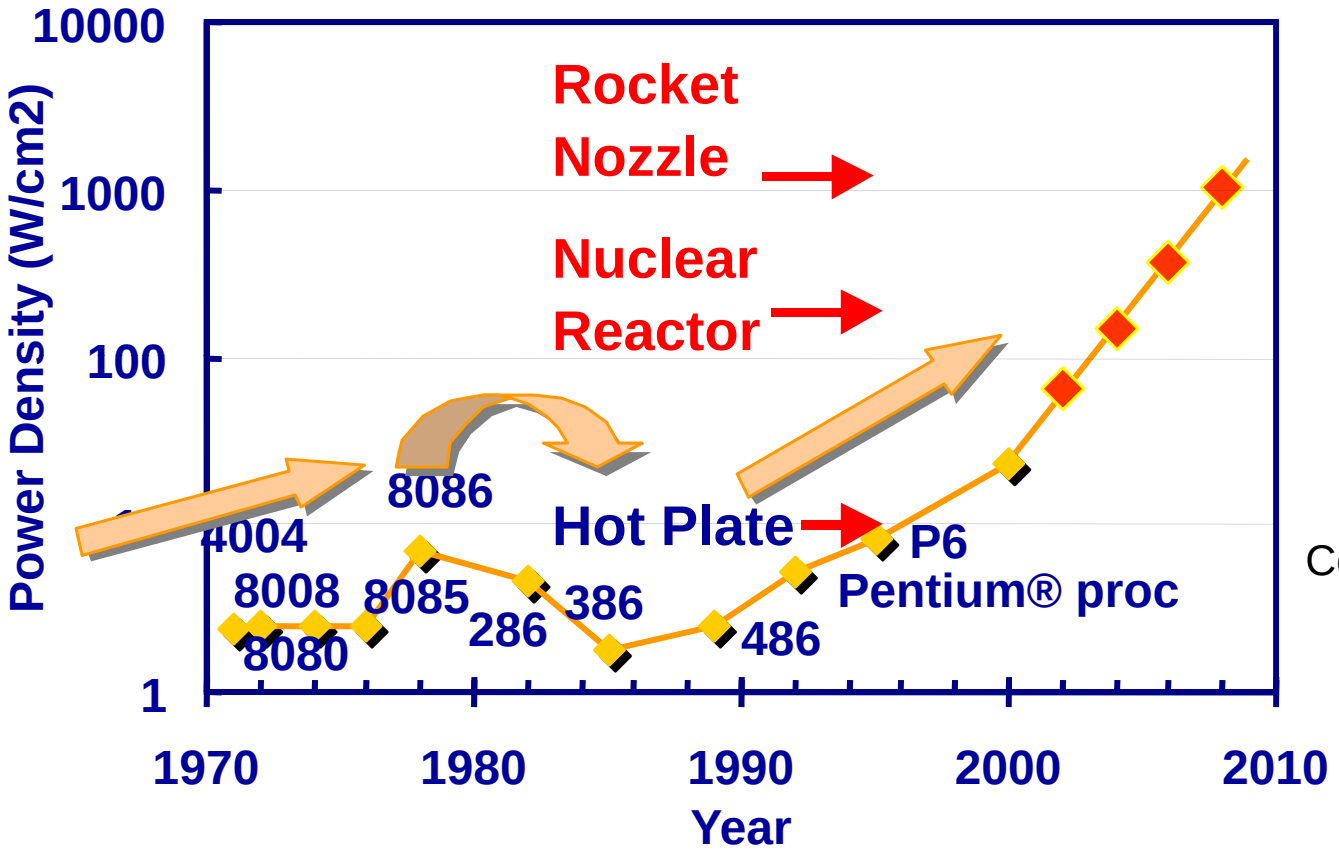
Power Dissipation



Courtesy, Intel

Lead Microprocessors power continues to increase

Power density

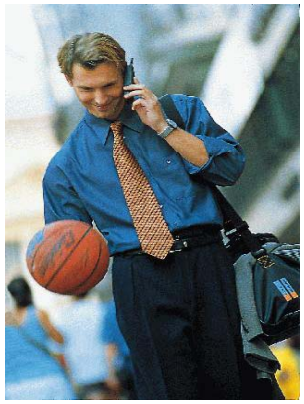


Courtesy, Intel

Power density too high to keep junctions at low temp

Not Only Microprocessors

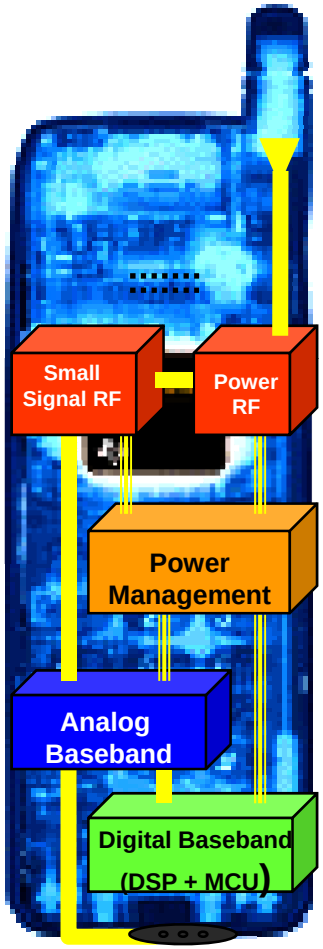
Cell Phone



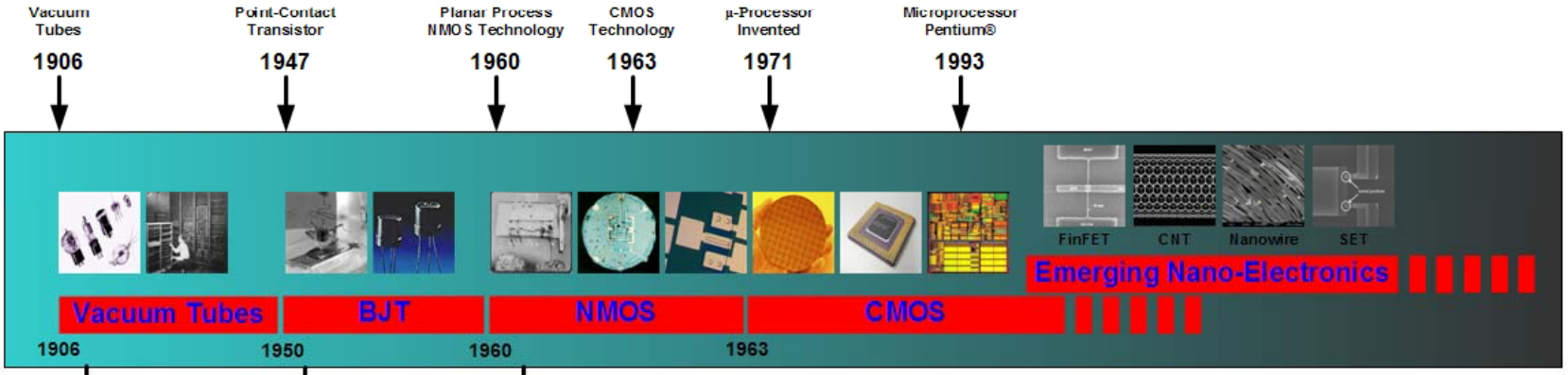
Digital Cellular Market (Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

(data from Texas Instruments)



Historical Perspective....



CMOS

(1) Easier control over processing (2) High circuit integration density (3) low cost (4) low power consumption
Due to technology scaling, leakage power dissipation and associated thermal problems are increasingly becoming major barriers in further advancement of CMOS technology.

Technology	Circuit level	System level
1. Scaling	1. Gate sizing	1. Heat sink
2. Copper wiring	2. Sleep transistor	2. Packaging materials
3. Low-k dielectrics	3. Stack forcing	3. Cooling techniques
	4. Variable Threshold CMOS (VTCMOS)	4. Heat pipes or folded fin assemblies
	5. Multi-Threshold CMOS (MTCMOS)	5. Refrigeration
	6. Input vector modification	
	7. Adaptive supply and body biasing	
	8. Optimal Vdd and Vth selection	

NMOS

(1) Easier control over processing (2) High circuit integration density (3) low cost (4) Lesser power dissipation than BJT (5) NMOS preferred over PMOS due to higher electron mobility (hence higher speed).
NMOS integrated circuits have large static power consumption.

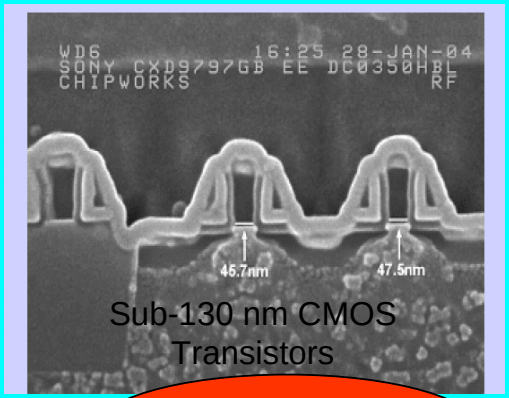
BJT

Bipolar junction transistors have high current drive capability and superior analog performance. This type of transistor is widely used as an amplifier and is also a key component in oscillators, high-speed integrated circuits, and switching circuits.
Device parameters for BJT are hard to control. Power consumption of BJT is extremely high limiting its integration density.

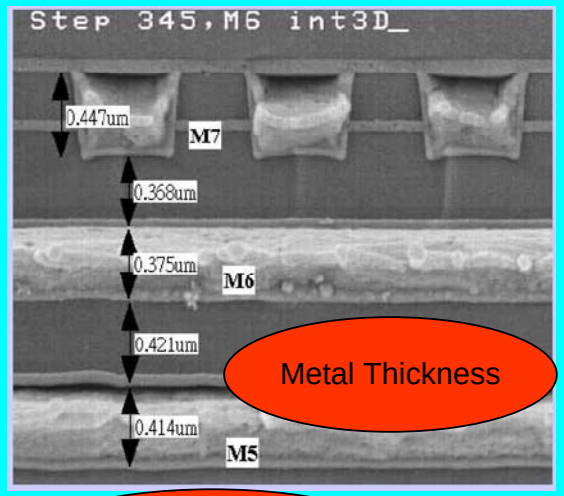
Vacuum Tube

During World War II, urgent military requirements started to push the vacuum-tube technology. The technology had fully matured with a wide range of tubes—diodes, pentodes, CRT's, klystrons, and traveling-wave tubes—in high-volume manufacture. Vacuum tubes were the key component in an array of electronic equipment that seemed to meet all conceivable information needs. Radio equipment—AM, FM, and microwave—was in wide use.
Vacuum tubes had low speed, short life, high power consumption. They were bulky and fragile. These disadvantages eventually limited their further progress.

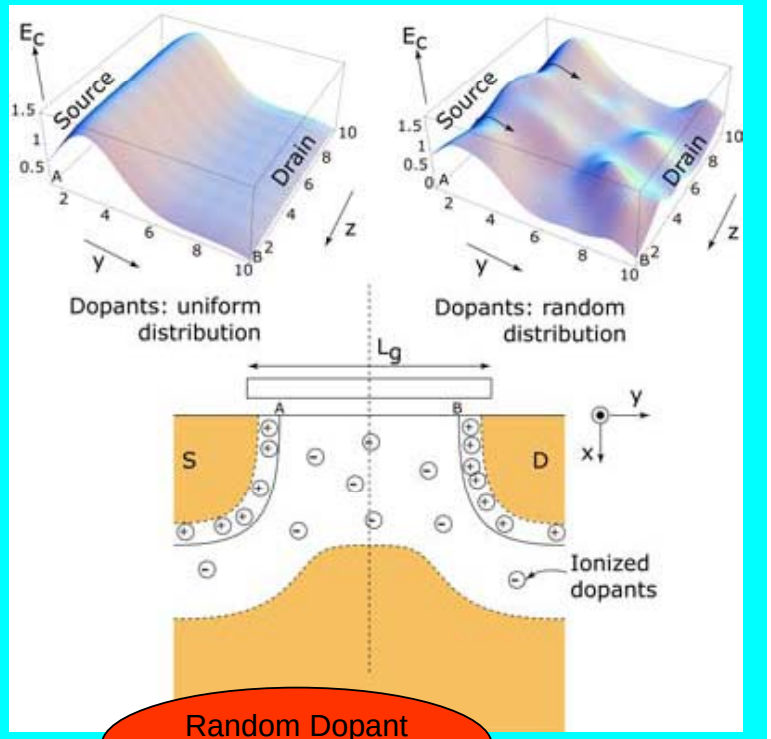
Process, Temperature and Voltage Variations



Transistor channel length

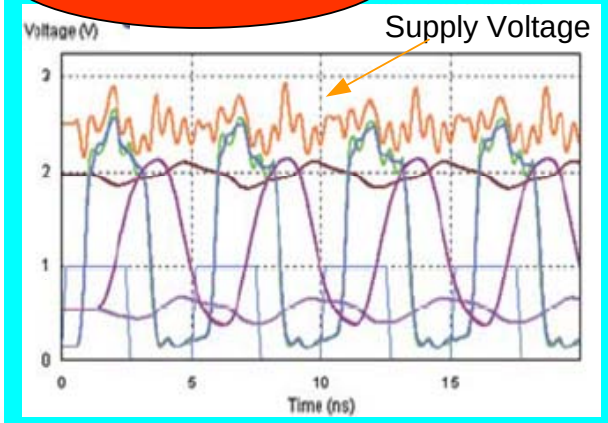


Metal Thickness

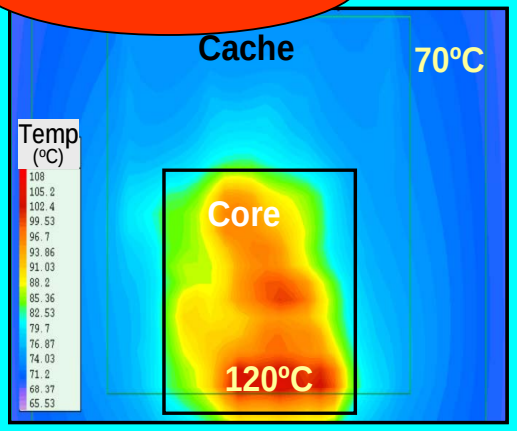


Random Dopant Fluctuations

Power Supply Voltage

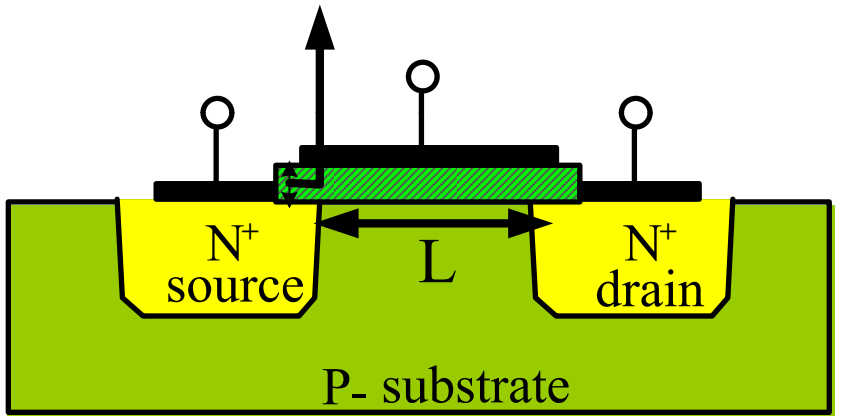


Chip Temperature



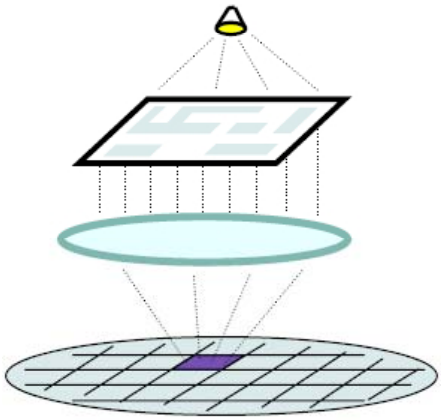
Key Parameter Variations

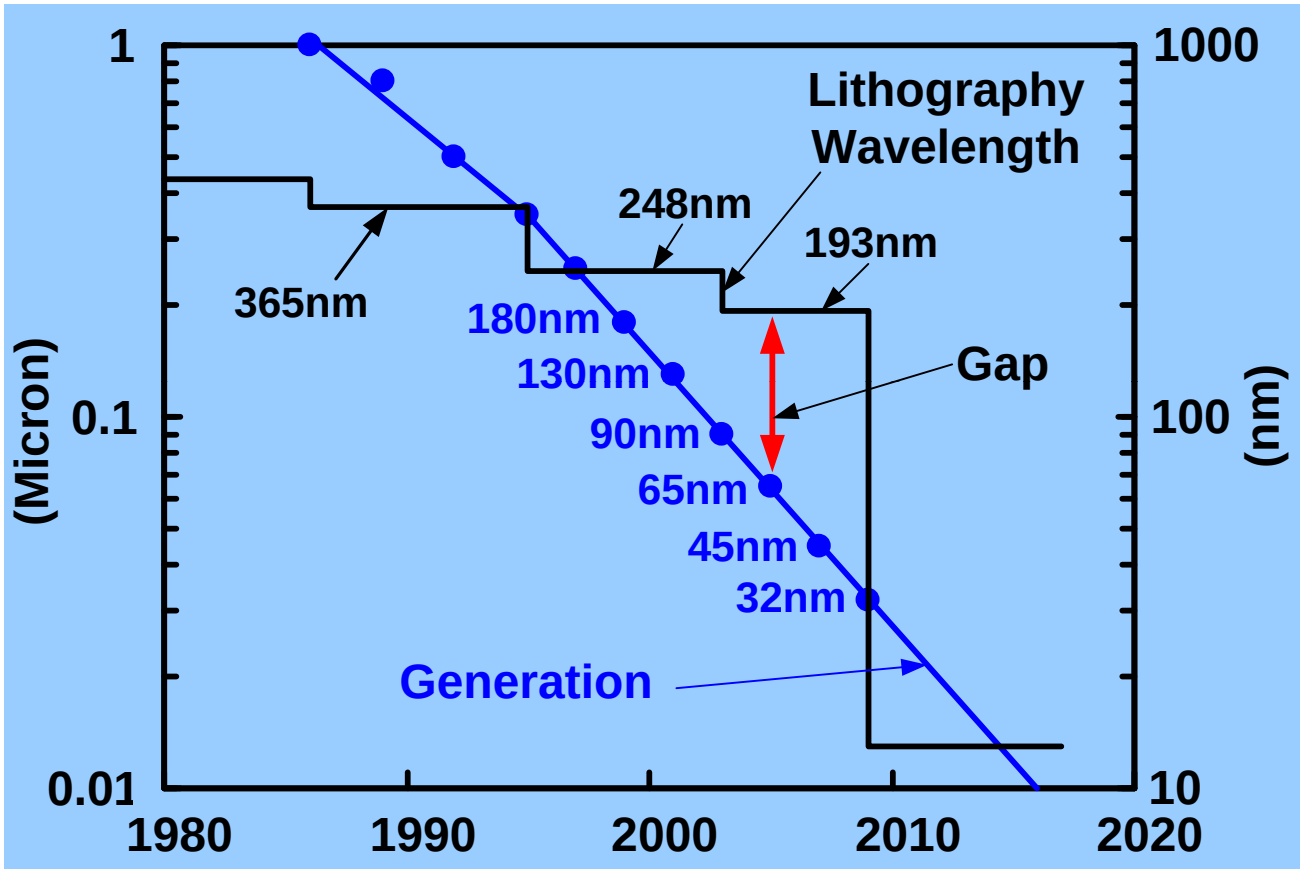
- Within-die Parameter Variations
  - Channel Length (*L*)
  - Oxide Thickness (*tox*)
  - Temperature (*T*)
  - Supply Voltage (V_{dd})



- Die-to-Die Parameter Variations
  - Channel Length (*L*)
  - Temperature (*T*)

Why Channel Length Variations are Increasing?



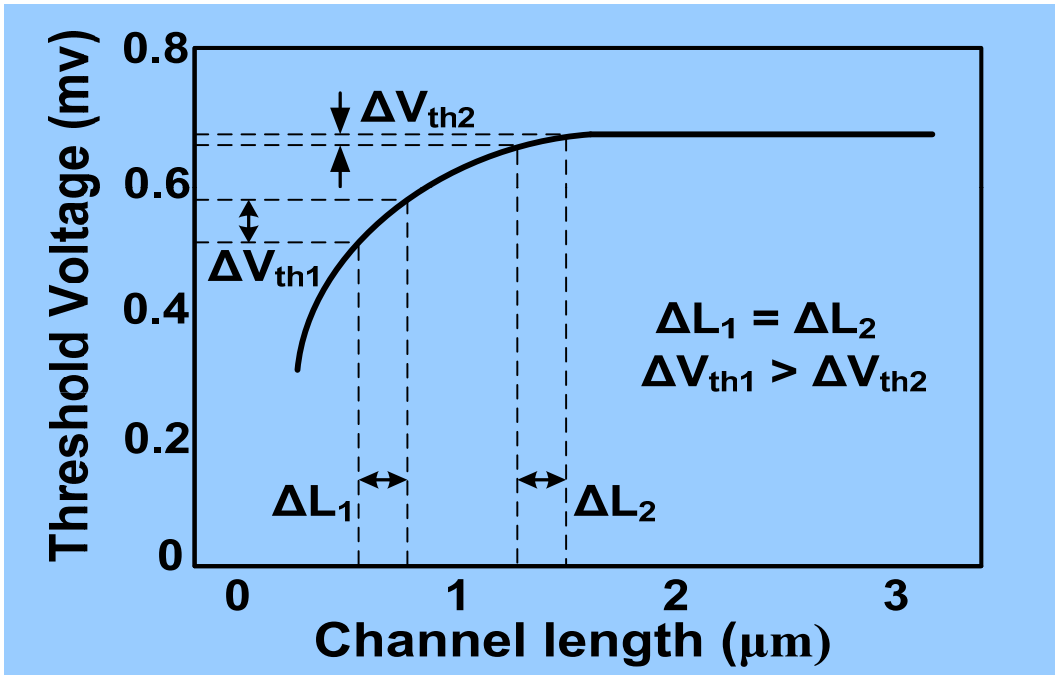


(S. Borkar et al. DAC2003)

- Minimum feature size is scaling faster than lithography wavelength
- Channel length exhibits significant amount of variations

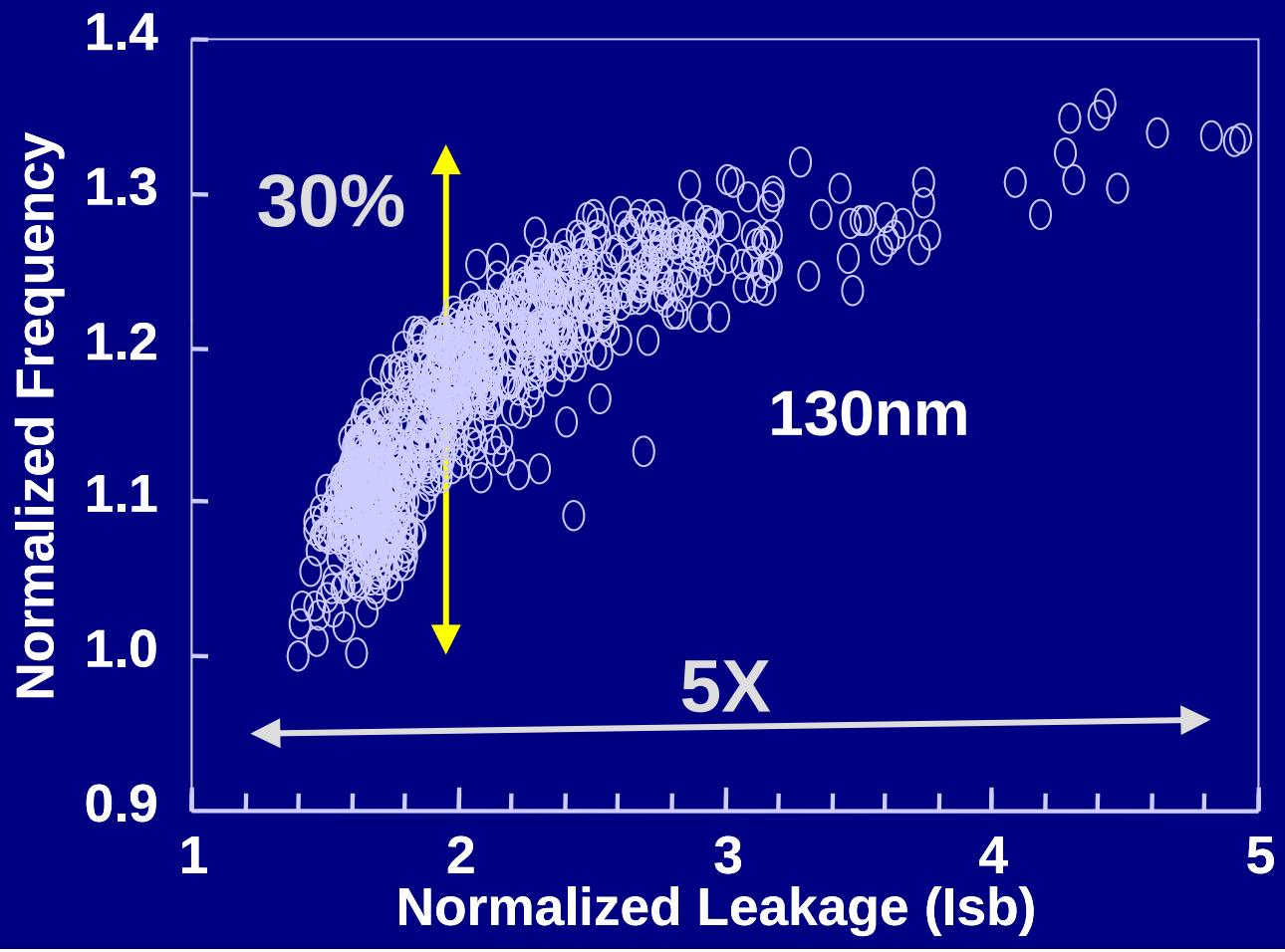
Impact of Device Scaling

Threshold voltage roll-off



- With technology scaling, the same amount of channel length variations result in greater variations in threshold voltage

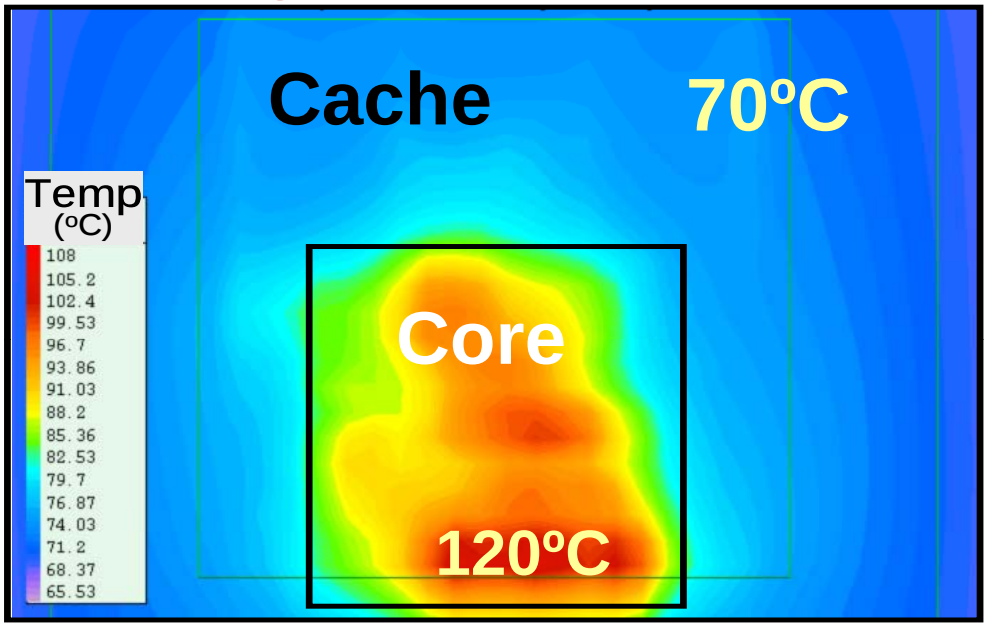
Impact of Static Variations



Frequency ~30%

Leakage Power ~5-10X

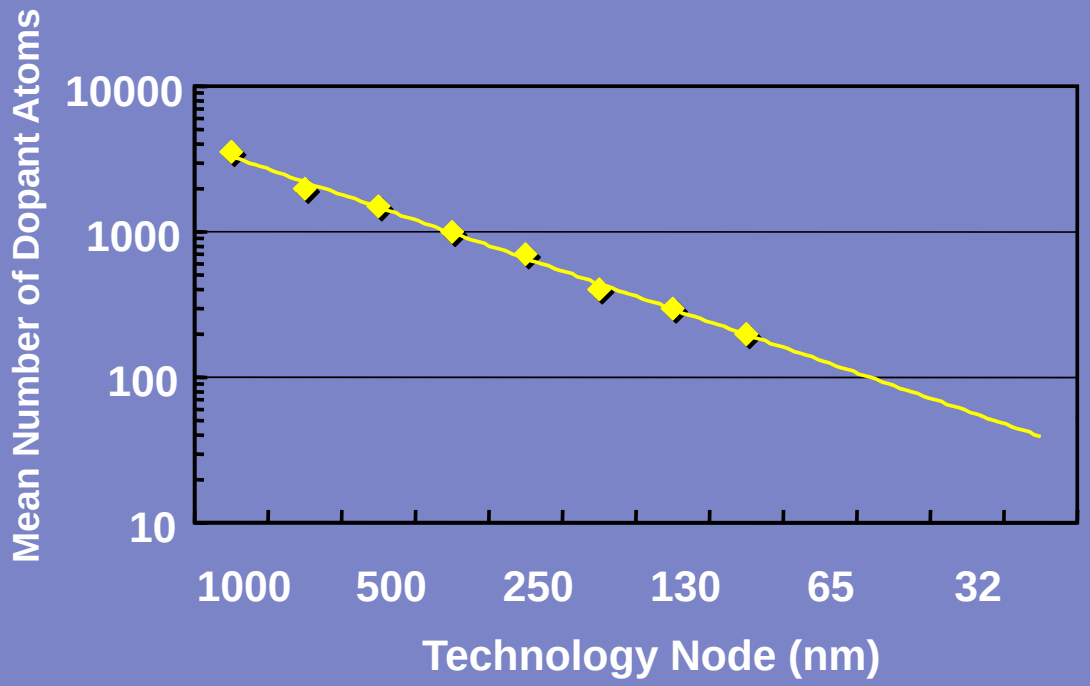
Why On-Chip Temperature Variations are Increasing?

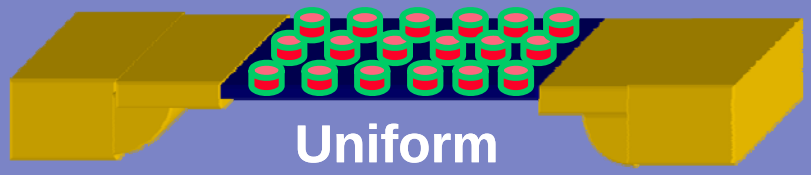


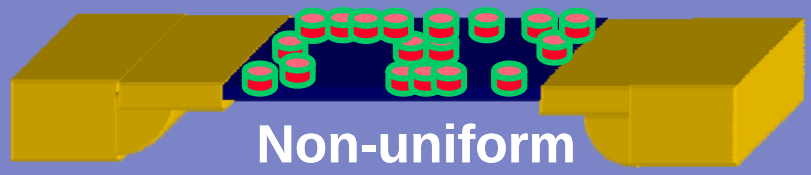
Temperature map of a high-performance microprocessor
Courtesy of S. Borkar, Intel Corporation.

- Difference in power dissipation of various blocks
- Dynamic power management techniques such as clock gating
- Leakage power distribution

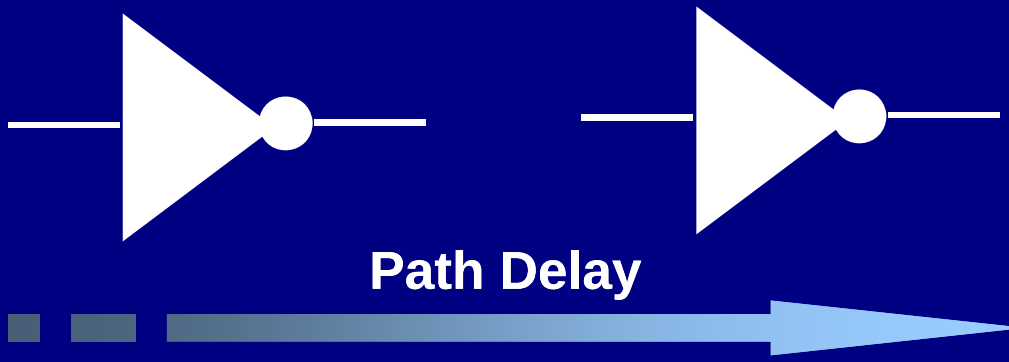
Random Dopant Fluctuations (Intrinsic)

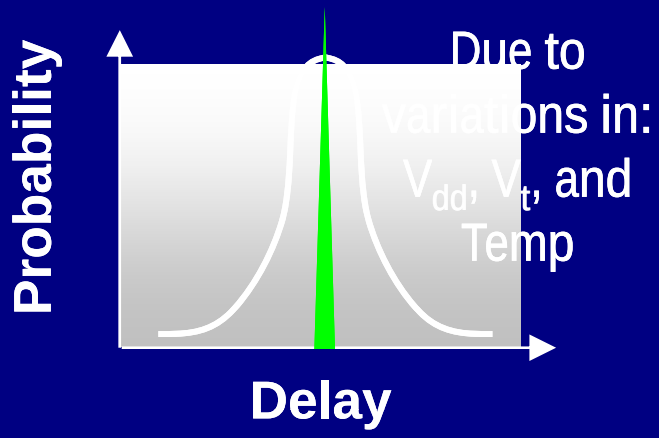


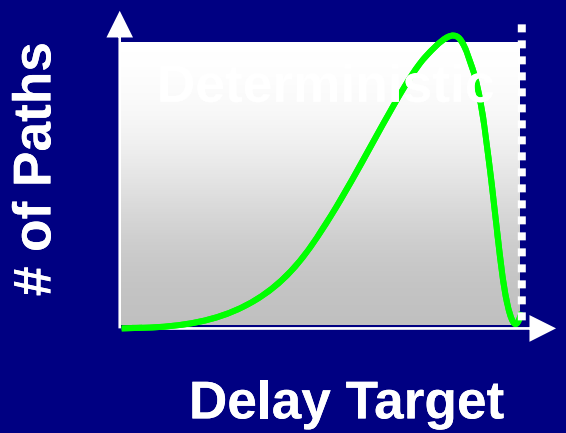


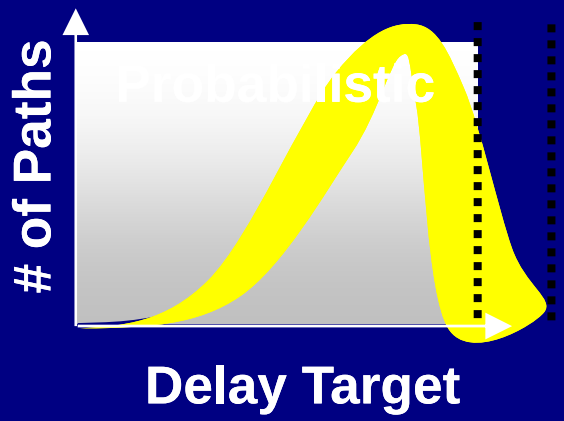


Probabilistic Design









Deterministic design techniques inadequate in the future

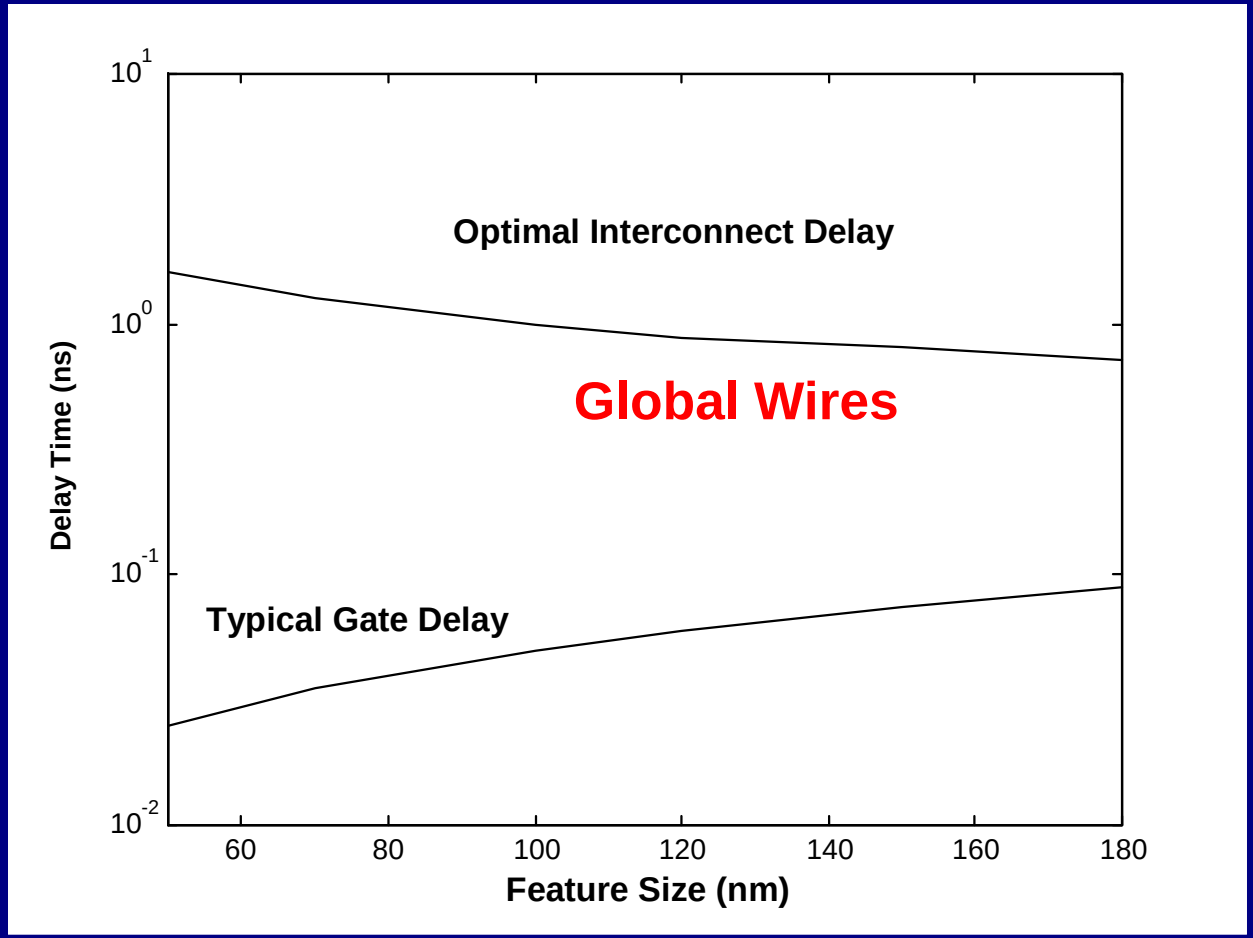
Shift in Design Paradigm

- Multi-variable design optimization for:
  - Yield and bin splits
  - Parameter variations
  - Active and leakage power
  - Performance

Today:
Local Optimization
Single Variable

Tomorrow:
Global Optimization
Multi-variable

IC performance is being dominated by interconnects

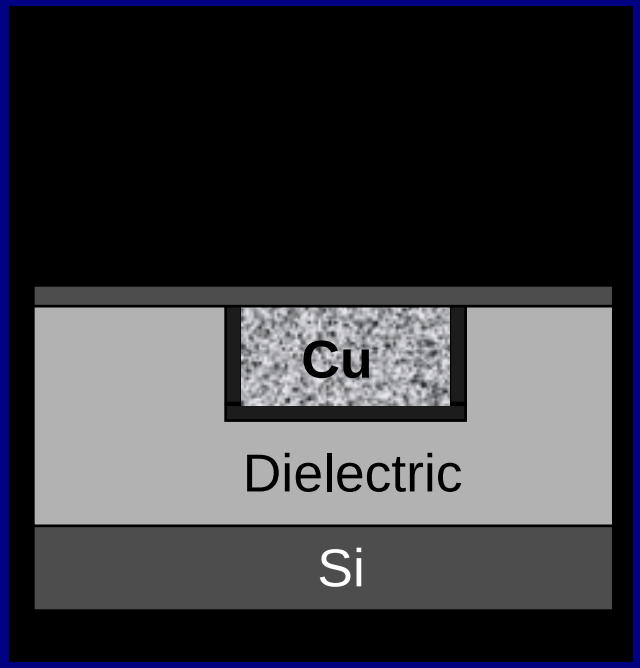


K. Banerjee et al., Proc. IEEE, May 2001.

Cu Resistivity: Effect of Scaling

Effect of Cu Diffusion Barrier

- Barriers have higher resistivity
- Barriers can't be scaled below a minimum thickness



Effect of Grain Boundary Scattering

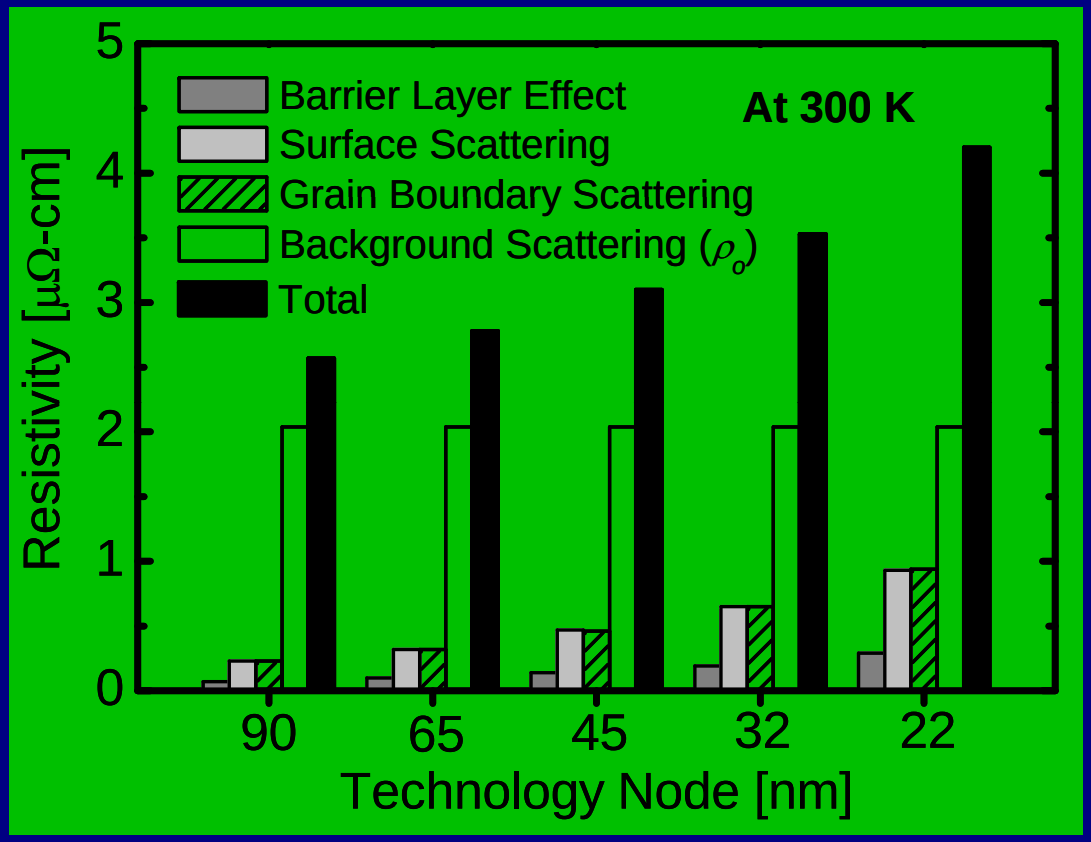
- e scattering from the G-bs
- increases effective resistivity

Effect of Electron Scattering

- e scattering from the surface
- further increase in effective resistivity

Problem is worse than anticipated in the ITRS roadmap

Cu Resistivity: Effect of Scaling



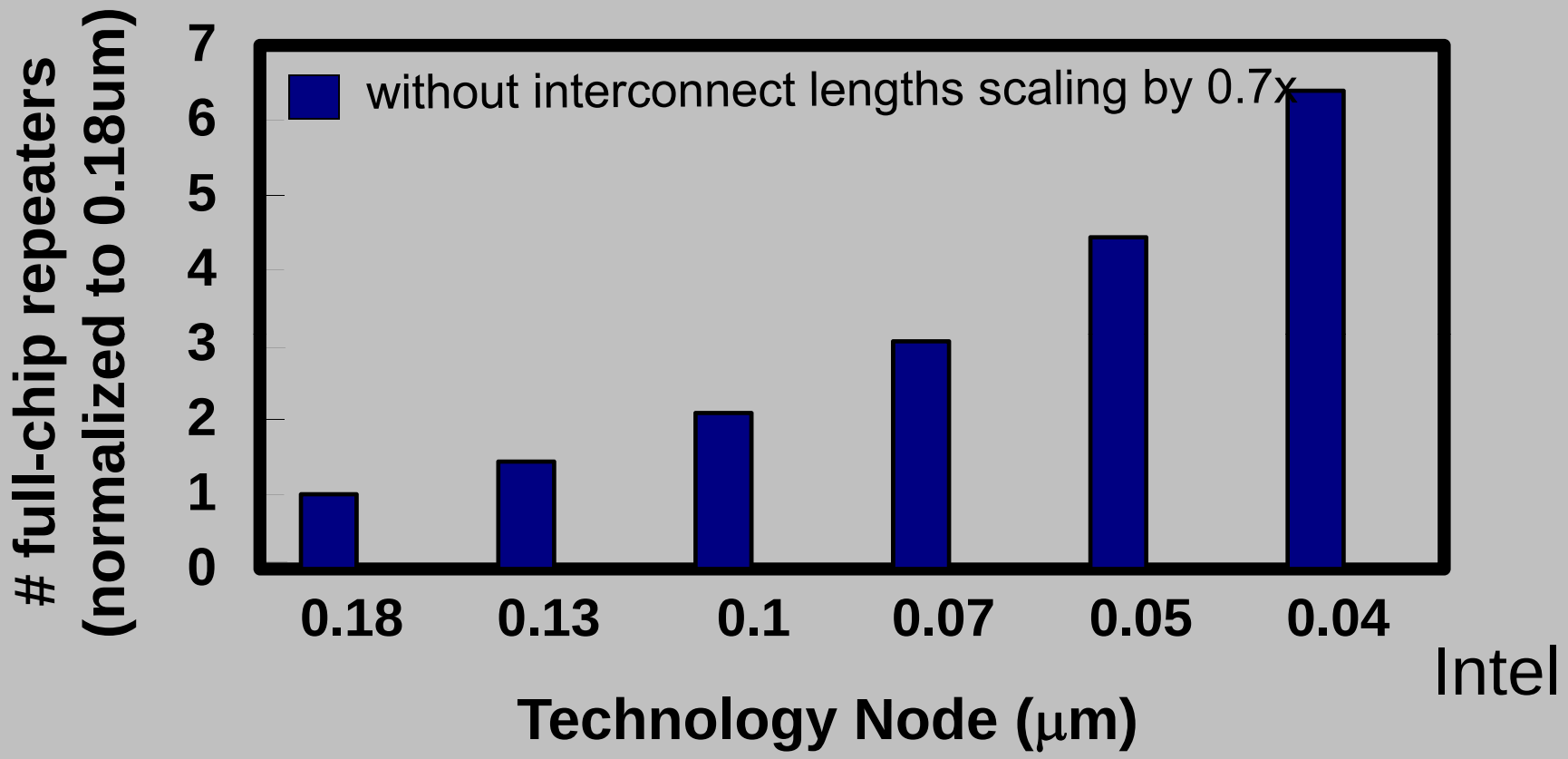
Based on analytical model in

W. Steinhogl et al., *J. Appl. Phys.*, 2005.

Im, Srivastava, Banerjee and Goodson, IEEE TED 2005.

Cu barrier layer, grain boundary and surface scattering leads to steep increase in Cu resistivity

Increasing Number of Repeaters



- **Increase in Cu resistivity will cause increase in size and number of repeaters**

Other Issues….

- Frequency of signals on interconnects is rising rapidly
- Frequency dependent impedance extraction is a major hurdle
  - Field solvers are unable to handle the complexity of VLSI interconnects
- Need to develop models for interconnect geometry dependent calculation of high frequency impedance
- Interconnect variability adds to the complexity of extraction….
- Situation is even more complex in 3-D ICs…..

Reliability Issues….affects design

- Electromigration in metal interconnects
- Self-heating issues
- Time-dependent dielectric breakdown
- NBTI
- Electrostatic discharge (ESD)

*Nanoscale CMOS Problems and **Solutions***

- High E-field: mobility degradation
  - Use Ge or SiGe (introduce strain) and increase mobility
- Gate: tunneling and depletion
  - Use high-k dielectric, metal gate (work function engineering)
- Source/Drain: parasitic contact resistance
  - Use Schottky S/D
- Channel: reduced Vg-Vt causes reduction in Ion (electrostatics)
  - Use DG, FinFET or Tri-gate to retain gate control over channel, minimize Ioff

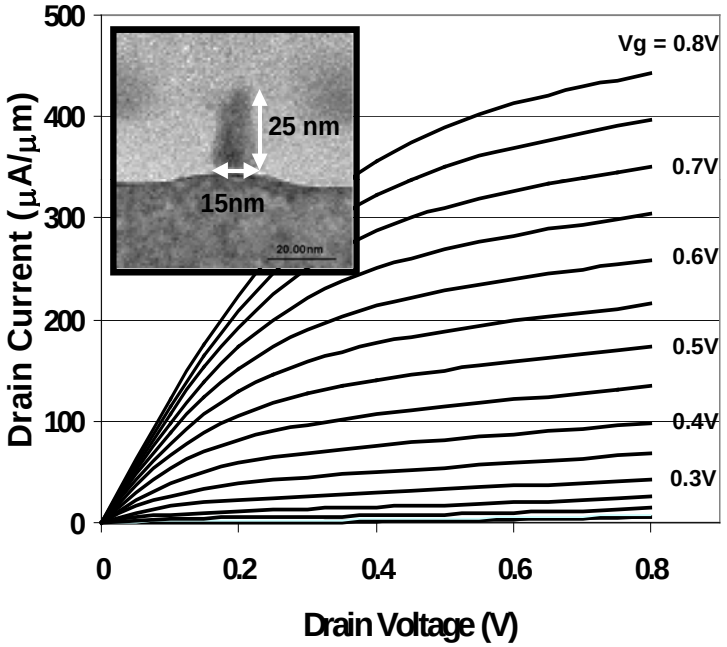
Pushing CMOS: the 10 nm wall

- **Smart engineering, new materials and evolutionary architectures have continuously pushed the CMOS limits…**

  I_{on} > 700 μA/μm
  I_{off} < 1000 pA/μm
  @ room temperature
  low operating power logic

- **Key problems of sub-10 nm MOSFET**

  (i) electrostatic limits
  (ii) source-to-drain tunnelling
  (iii) carrier mobility
  (iv) process variations
  (v) static leakage
  (vi) power density

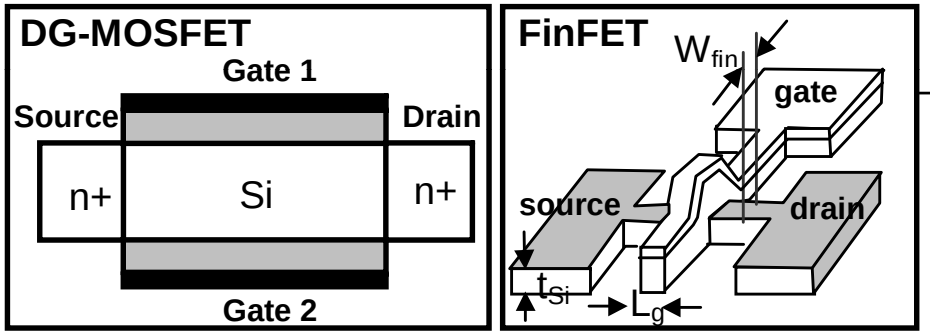


Intel's 15 nm channel length MOSFET

Emerging Device Architectures

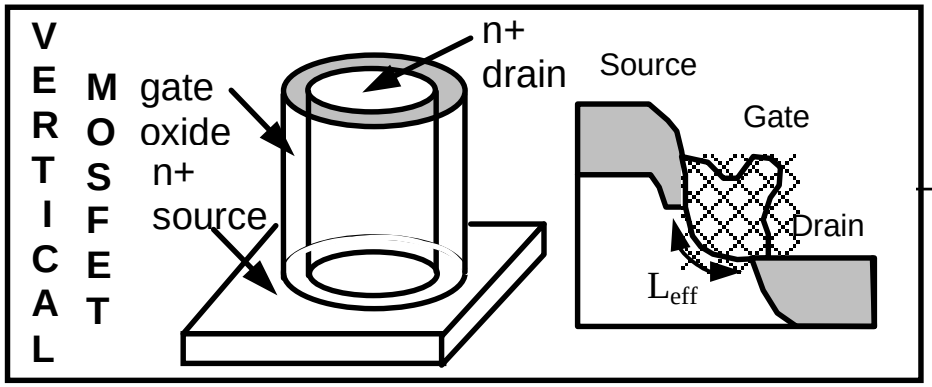
- **Double/Multi-Gate, FinFET and vertical MOSFET**

Better control of the channel charge (current) → overdrive



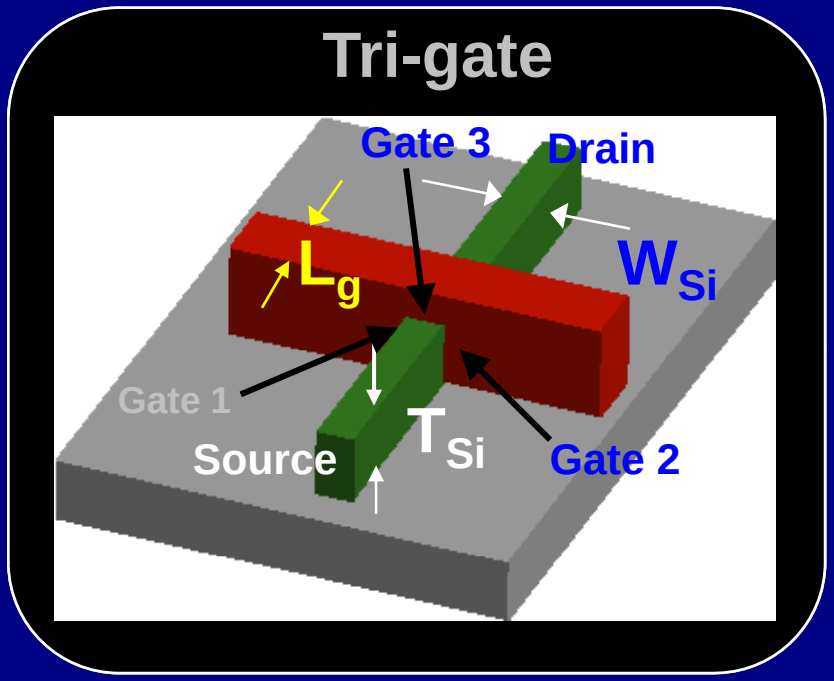
- excellent scalability: reduced SCE, V_T roll-off and DIBL
- better transconductance
- exploits SOI architecture

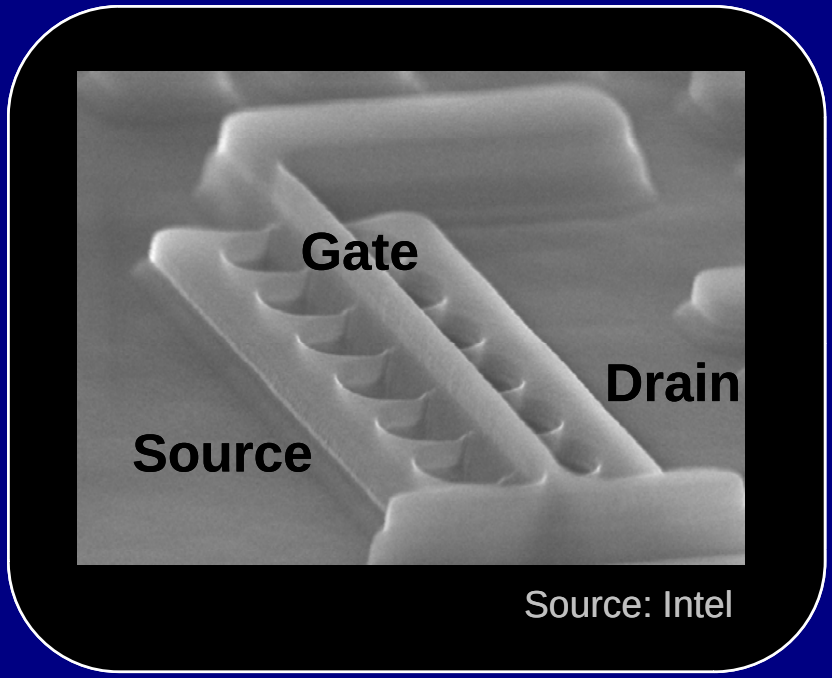
Both PMOS and NMOS up to 8nm shown



- lithography quasi-independent
- high level of functional integration

Tri-Gate and Multi-Fin Double Gate Devices





Improved short-channel effects
Higher ON current for lower SD Leakage

Identifying new parameters that may vary and impact circuit metrics

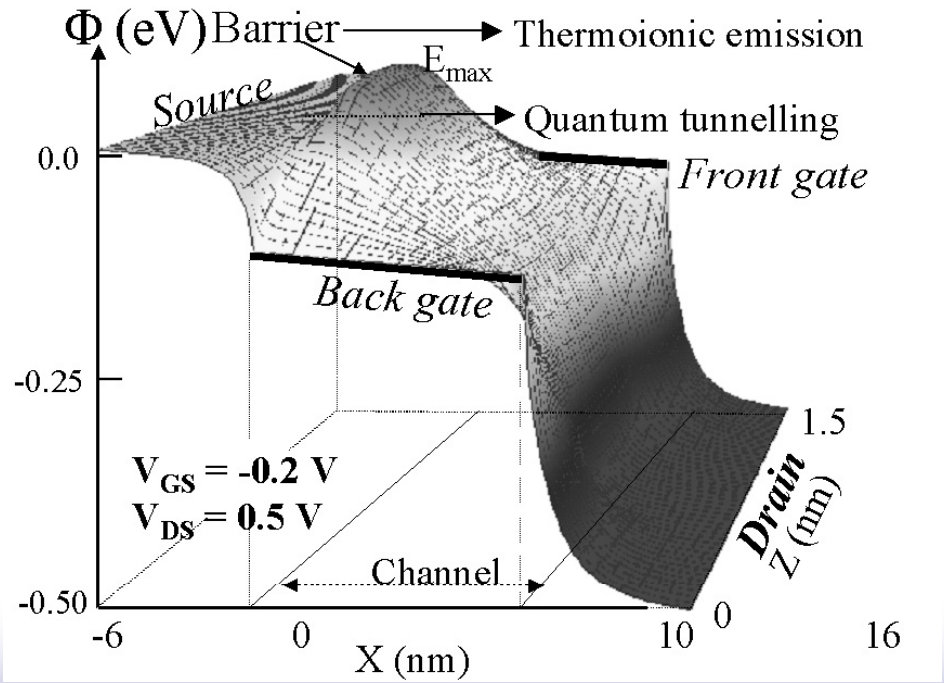
Emerging Device Architectures

- **Ballistic MOSFET**
  - → **channel length less than carrier mean free path defines the basic of ballistic transport**
  - → No collisions: **no carrier mobility**
  - → **ballistic is benefic effect** → significant current increase

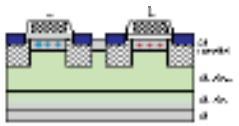
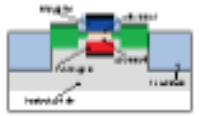
New conduction mechanisms:
(i) Thermoionic emission
(ii) Quantum tunnelling

Nice but…

voltage/power scaling with L reduction does not apply because current is limited by electron supply at source



Non-classical CMOS: a comparative study

					
DEVICE	ULTRA-THIN BODY SOI	BAND-ENGINEERED TRANSISTOR	VERTICAL TRANSISTOR	FINFET	DOUBLE-GATE TRANSISTOR
CONCEPT	Fully depleted SOI	SiGe or Strained Si channel; bulk Si or SOI	Double-gate or surround-gate structure (No specific temporal sequence for these three structures is intended)		
APPLICATION/DRIVER	Higher performance, Higher transistor density, Lower power dissipation				
ADVANTAGES	-Improved subthreshold slope -V_t controllability	-Higher drive current -Compatible with bulk and SOI CMOS	-Higher drive current -Lithography independent L_g	-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND	-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND
SCALING ISSUES	-Si film thickness -Gate stack -Worse short channel effect than bulk CMOS	-High mobility film thickness, in case of SOI -Gate stack -Integration	-Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM effect	-Si film thickness -Gate stack -Process complexity -Accurate TCAD including QM effect	-Gate alignment -Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM effect
DESIGN CHALLENGES	-Device characterization -Compact model and parameter extraction	-Device characterization	-Device characterization -PD versus FD -Compact model and parameter extraction -Applicability to mixed signal applications		
MATURITY	Development				

Where are we heading?

- **Emerging Materials/Devices for VLSI:**
  - **Classical and non-classical CMOS**
  - **3-D ICs (already discussed in previous lecture)**
  - **Beyond CMOS (carbon nanotube, graphene based)**
  - **Novel Interconnect Technologies (CNT, Graphene Nanoribbons, RF, Optical, etc)**
- **Green Electronics**
  - **Low Power Interconnects**
  - **Small Subthreshold Swing Devices (sub-kT/q devices)**
    - **Tunnel FETs**
    - **Nanoelectromechanical switches**
  - **On-Chip Energy Storage (capacitive, inductive)**

Device driven circuit design or Circuit driven device design?-----or perhaps device-circuit co-design?