ECE 225
High-Speed Digital IC Design
Lecture 11

MOSFET Scaling and Non-Classical CMOS

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Gate Leakage

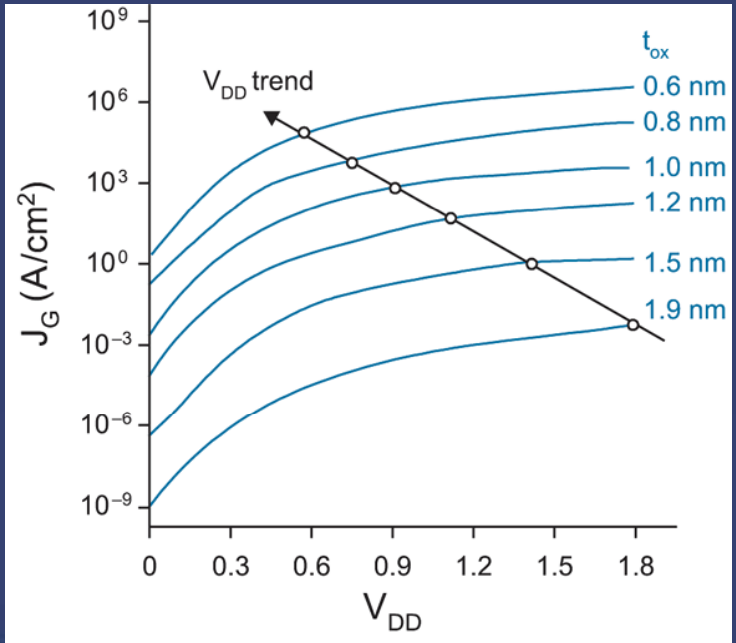
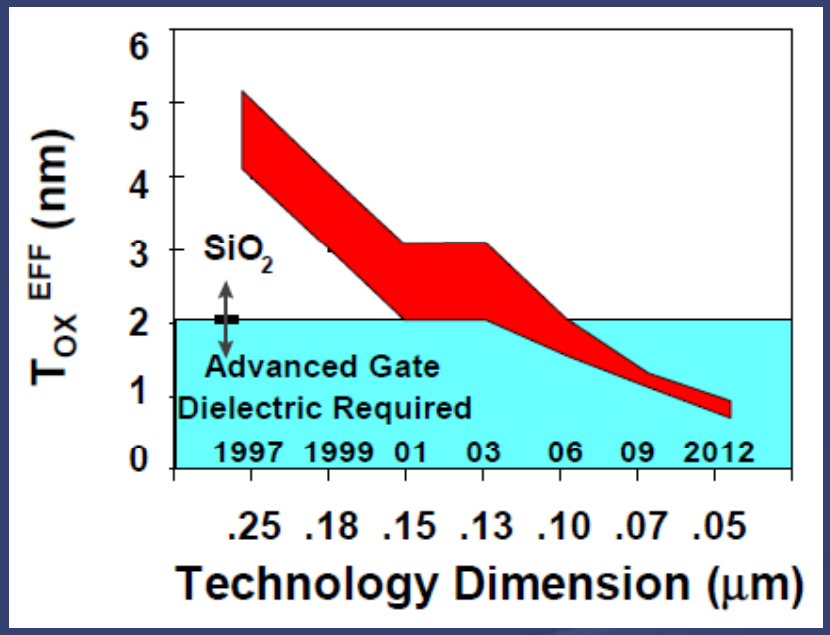
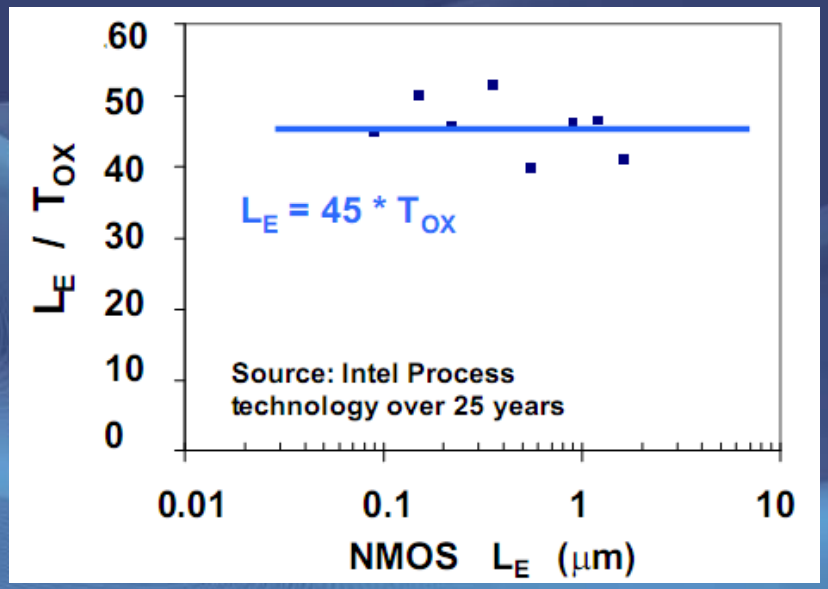


FIG 2.20 Gate leakage current from [Song01]





- *Increases with gate oxide (SiO2) scaling*
- *High-k gate oxides can be used to lower gate leakage*
- *Independent of temperature*

Junction Leakage

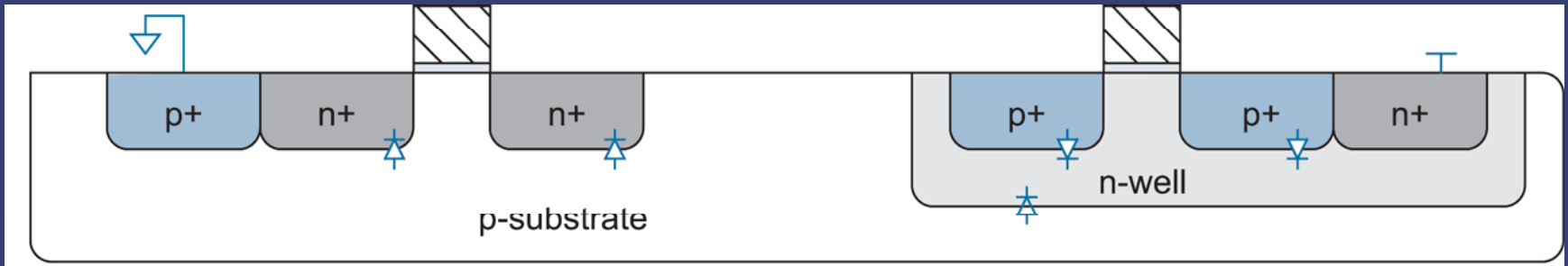


FIG 2.19 Reverse-biased diodes in CMOS circuits

- *Less significant than gate and subthreshold leakage*
- *Increases with temperature*

Leakage

- Effect of leakage current
  - "Wasted" power: power consumed even when circuit is inactive
  - Leakage power raises temperature of chip
  - Can cause functionality problem in some circuits: memory, dynamic logic, etc.
- Reducing transistor leakage
  - Long-channel devices
  - Small drain voltage
  - Large threshold voltage V_T

Leakage

- Leakage vs. performance tradeoff:
  - For high-speed, need small V_T and L
  - For low leakage, need high V_T and large L
- Process scaling
  - V_T reduces with each new process (historically)
  - Leakage increases ~10X!
- One solution: dual-V_T process
  - Low-V_T transistors: use in critical paths for high speed
  - High-V_T transistors: use to reduce power

Temperature Effects

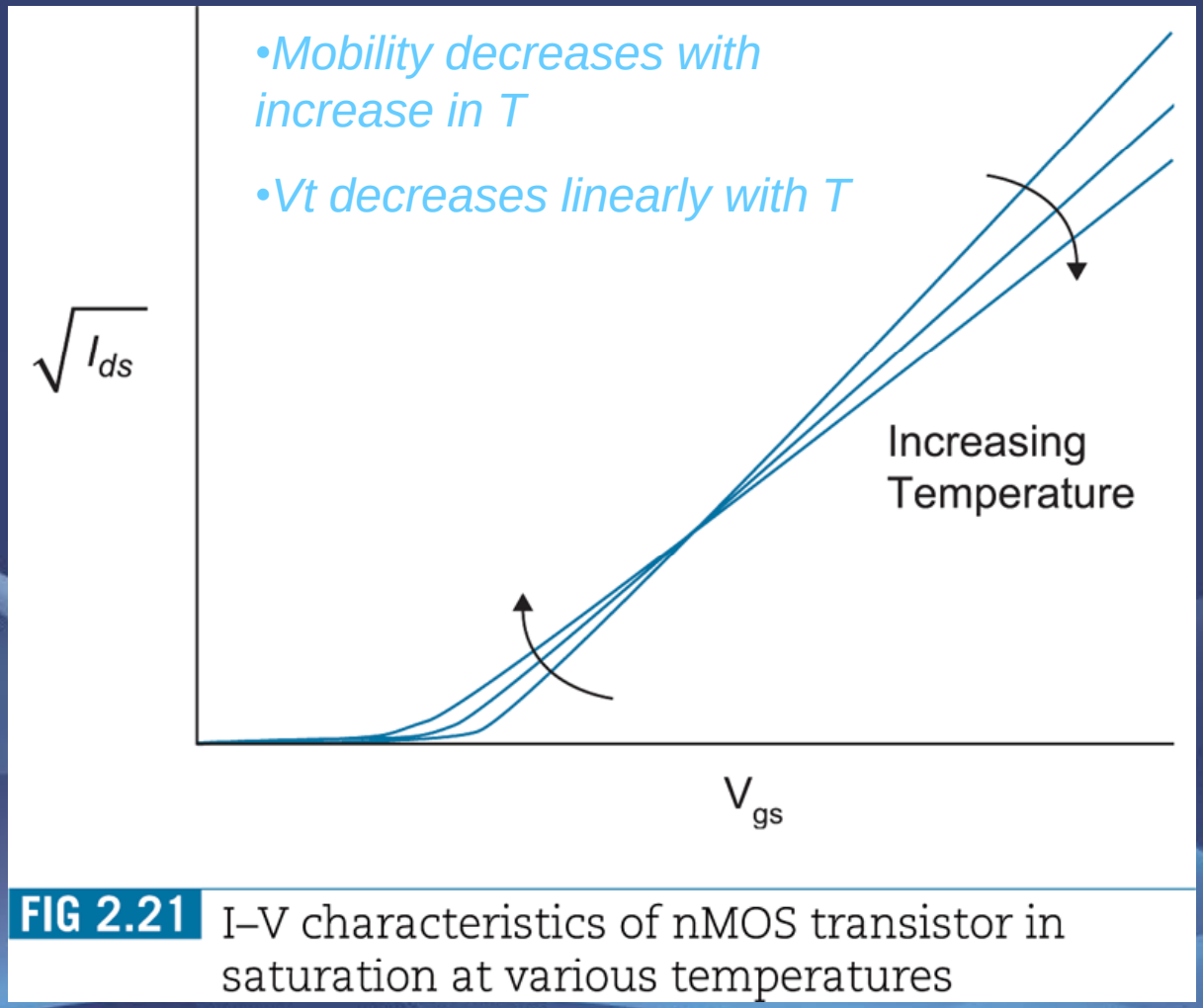


FIG 2.21 I–V characteristics of nMOS transistor in saturation at various temperatures

What happens in ultra low-voltage designs?

See paper by Sakurai…

Temperature Effects

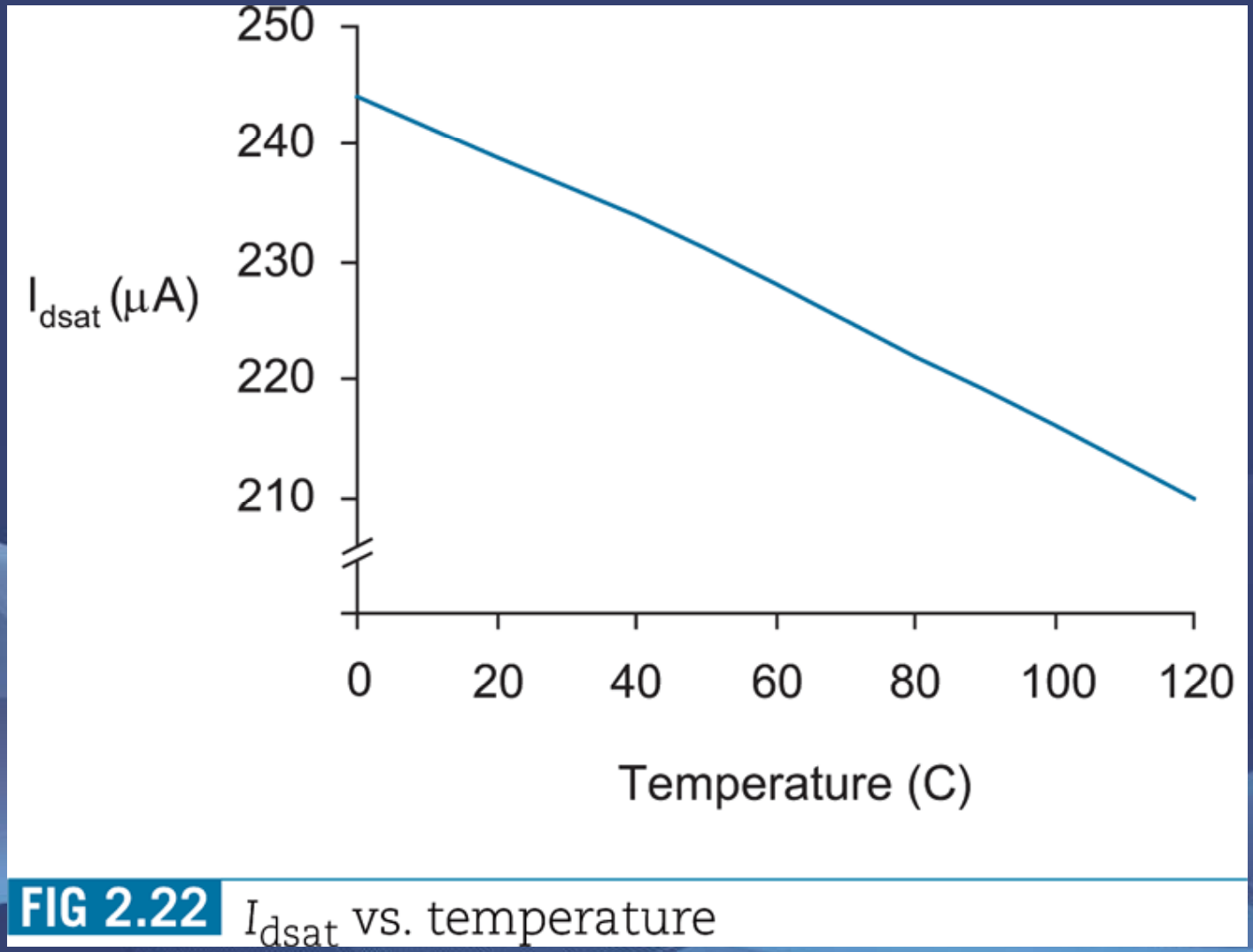


FIG 2.22 I_{dsat} vs. temperature

Hot Carrier Effects

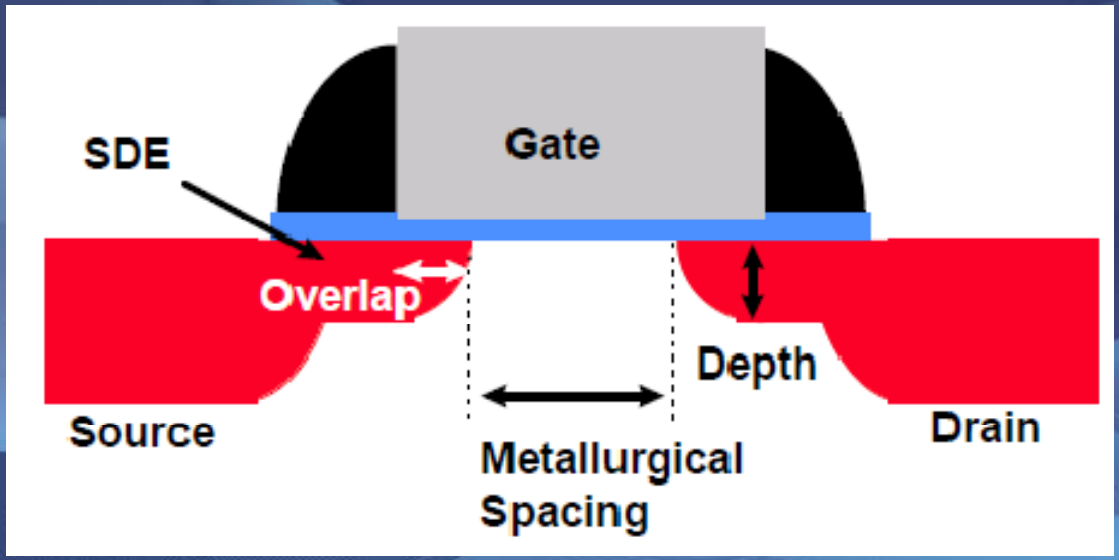
- High-energy electrons can tunnel into gate oxide
- This changes the threshold voltage (increases VT for NMOS)
- Can lead to long-term reliability problems

Avalanche Breakdown

- Due to scaling, high-velocity electrons can impact the drain, dislodging holes---Called impact ionization
- Holes are swept towards grounded substrate → cause substrate current
- Also affects long-term reliability
- This is another factor which limits the process scaling → voltage must scale down as length scales

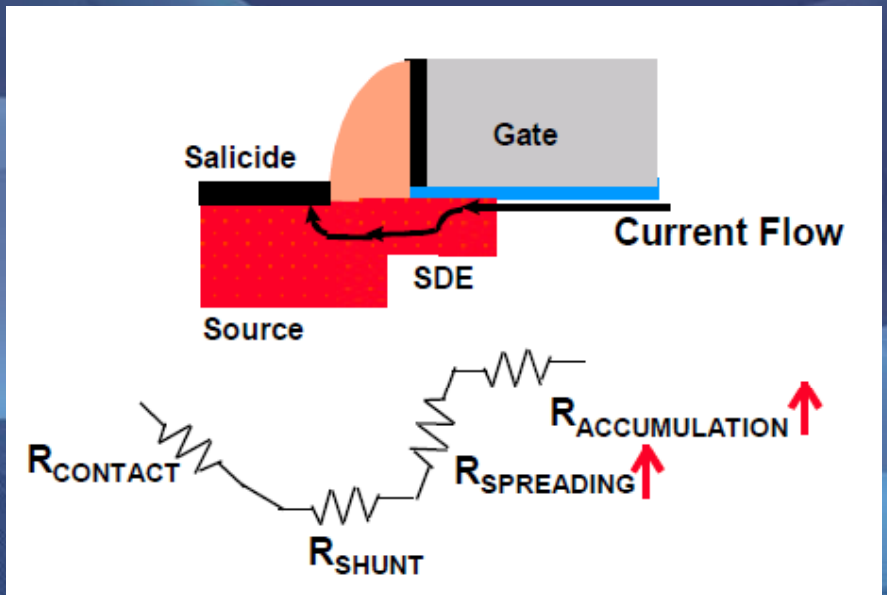
S/D Engineering in the Scaled Regime

- Scaling of S/D extension (SDE) depth and gate overlap is explained
- Junction depth in 0.25 um technology node is 50-100 nm.



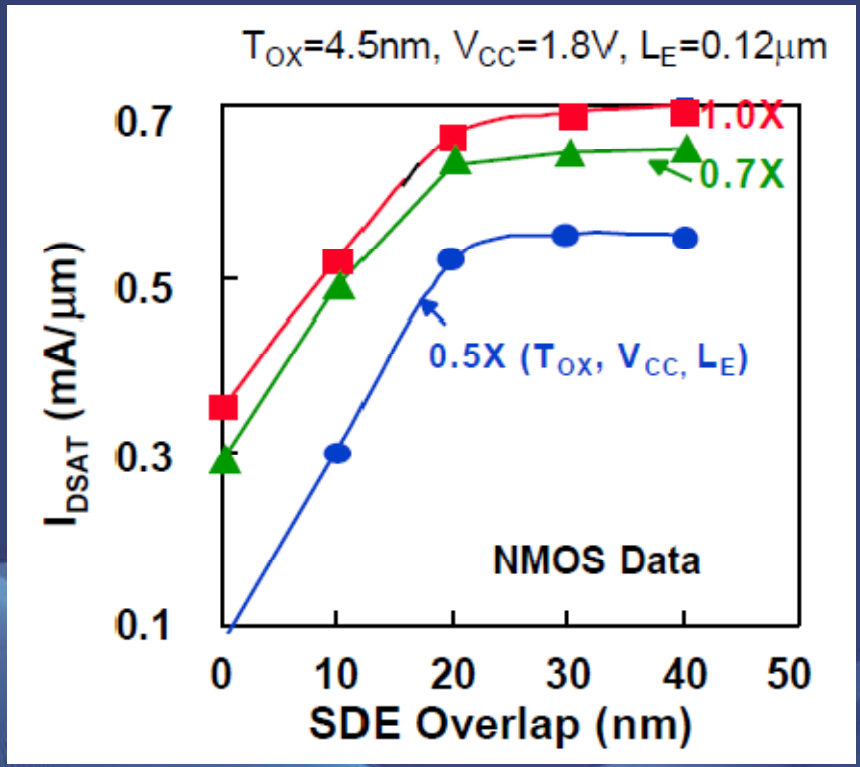
S/D Engineering

- Shallow junctions lead to high external resistance (sheet resistance is higher)
- Shallow junction improves the short channel characteristics by reducing the amount of charge controlled by the drain (note that gate has less control in regions further from the oxide/Si interface)



S/D Engineering

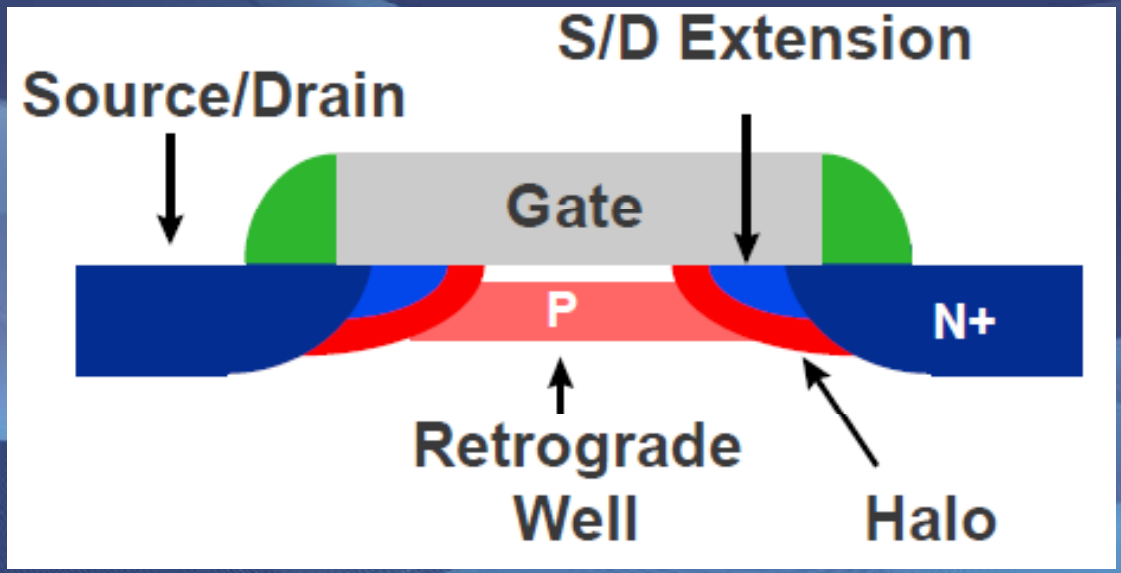
- Reducing SDE-to-gate overlap causes current to spread out into a lower doping location of SDE leading to higher resistance
- By varying the thickness of the offset spacer, the SDE-to-gate overlap and vertical junction depth can be independently varied.



Channel Engineering

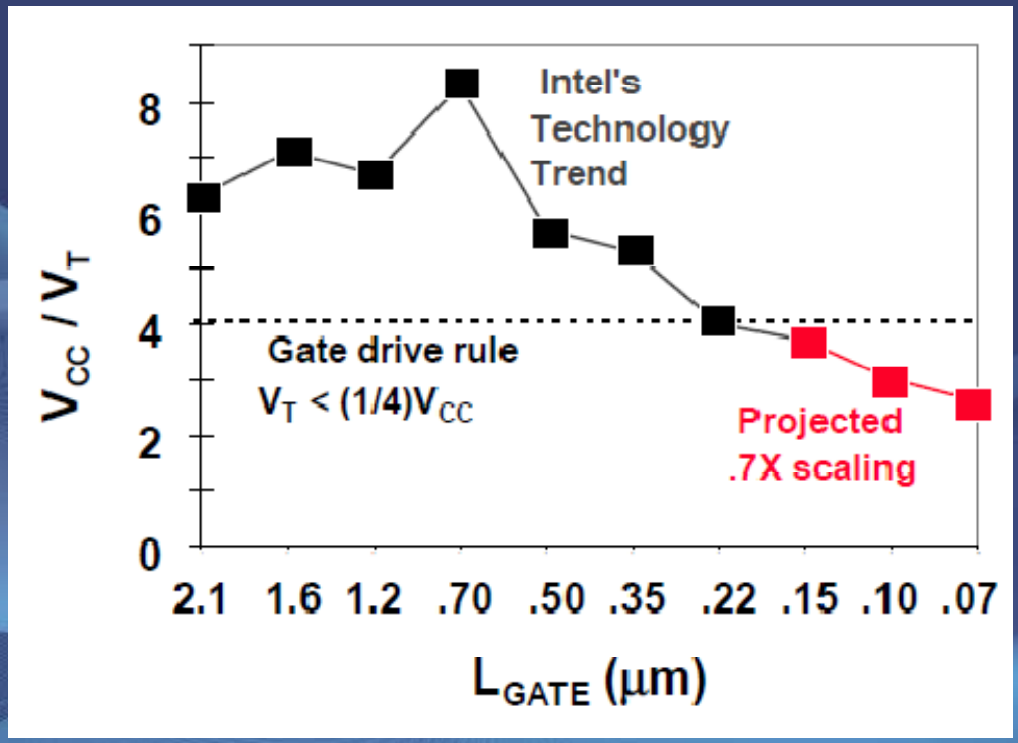
- Modifying doping profile in the channel:
  - Retrograde doping
  - Halo doping

  (Increases junction abruptness)



V_{CC} and V_{th} Scaling

- To keep the gate overdrive (Vcc – Vth) high, the Vth must be scaled
- However lowering Vth at low gate lengths leads to high leakage



Alternative Options in the Ultra-Scaled Regime

- Dual-Vth Architecture
- SOI
- FINFET
- Dynamic-Vth device
- High-k gate oxide
- Strained device
- Steep subthreshold slope devices

Alternative Oxides

OPTION	ISSUES / STATUS
Si_3N_4 /	Small advantage especially with buffer layer
nitride	Close to being ready (G. Lucovsky, T. P. Ma)
Ta_2O_5	Need SiO_2 buffer/ no poly-silicon gate
	Very early stages (S. Kamiyama)
TiO_2	Need SiO_2 buffer/ no poly-silicon gate
	Very early stages (S. A. Campbell)
BST	Deep states/ buffer layer/ no poly-silicon gate
	Early stages FET (large DRAM interest)

Gate Oxide Scaling Issues

- Currently, gate dielectric approaching thickness of a few atoms
  - Problem: Quantum Mechanics
  - Electron tunneling → gate current leakage
- With the number of transistors on a single chip growing exponentially, power dissipation becomes a big problem.

Problem with SiO_2

- SiO_2 layer is too thin.
  - 90nm node has a dielectric thickness of 1.2nm.
- Low relative dielectric constant.
- If there is to be any increase in performance, an alternative must be found.

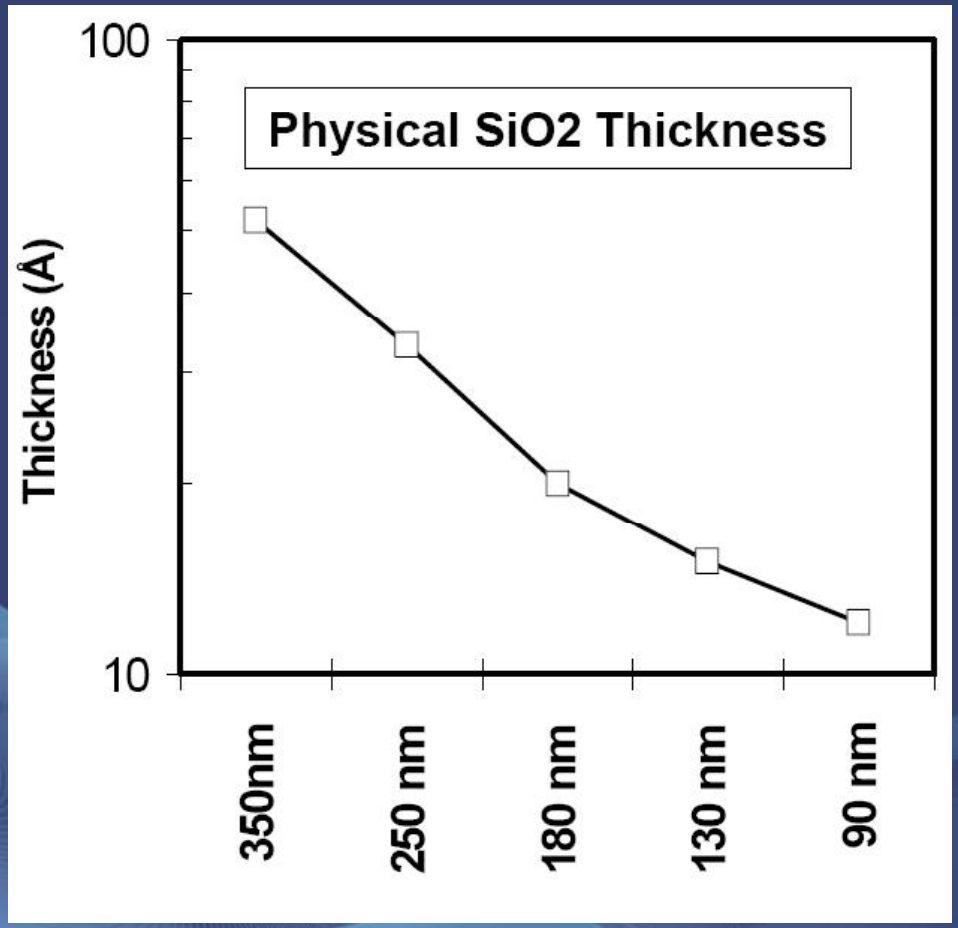


Image courtesy of Intel.

Solution: High-K Dielectric

- Options:
  - Increase dielectric thickness.
  - Increase relative dielectric constant.
- High-k dielectrics are a logical solution.

Solution: High-K Dielectric

- Problems with high-k/poly-si:
  - Increased threshold voltage

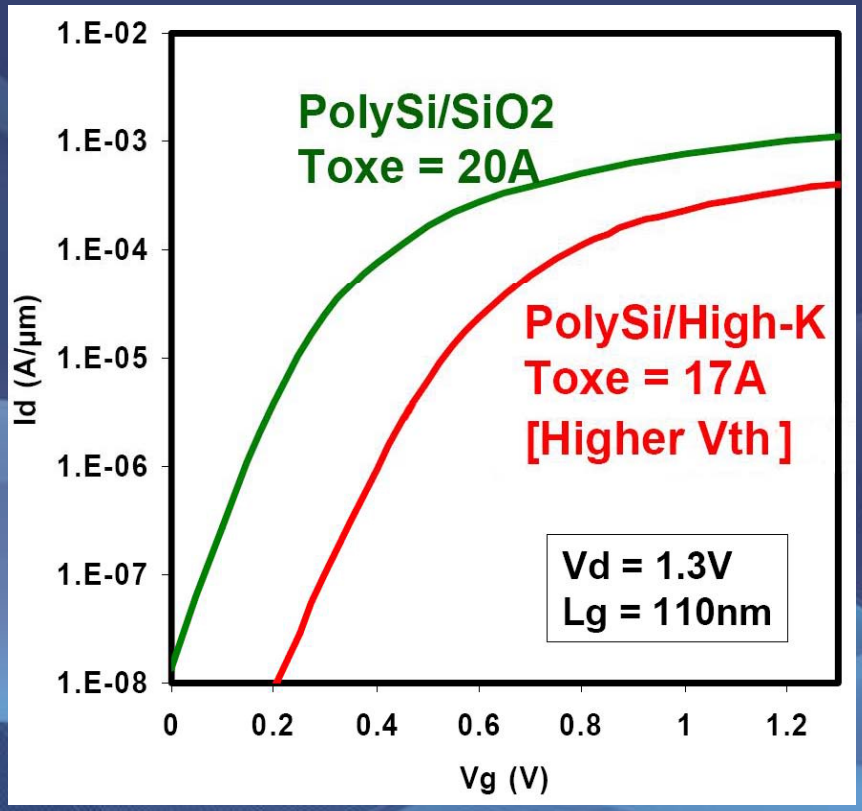


Image courtesy of Intel.

Solution: High-K Dielectric

- Problems with high-k/poly-si:
  - Increased threshold voltage
  - Decreased channel mobility

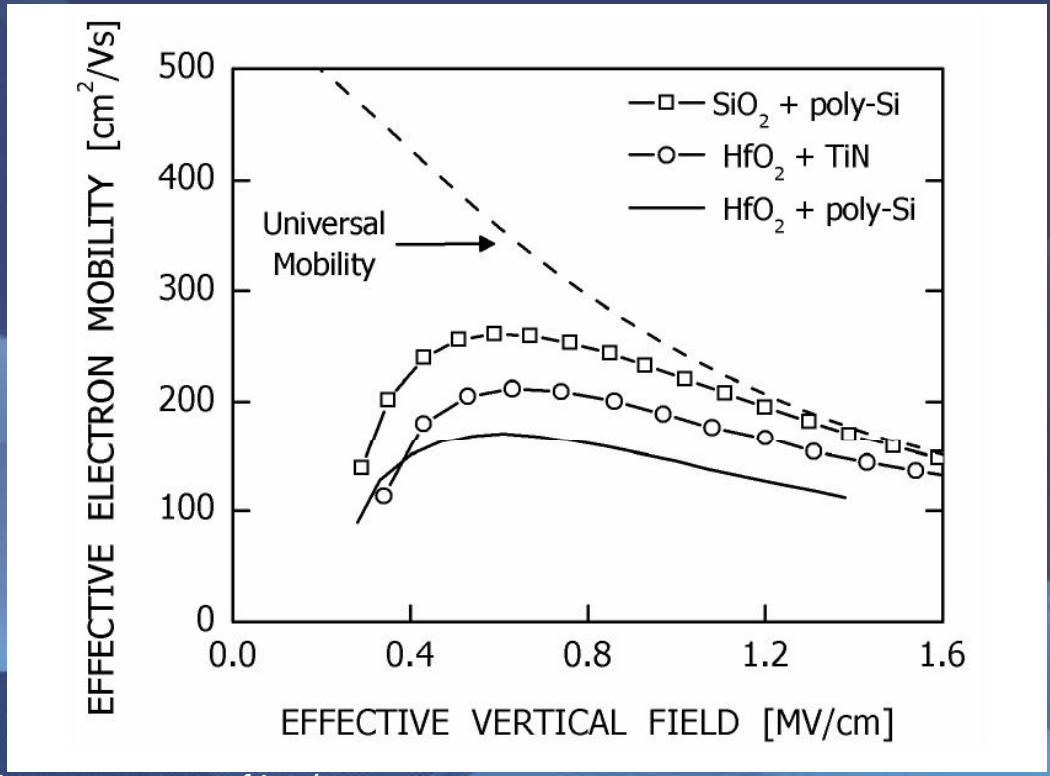


Image courtesy of Intel.

Solution: High-K Dielectric

- Replace poly-si gates with doped, metal gates.
  - Improved mobility.

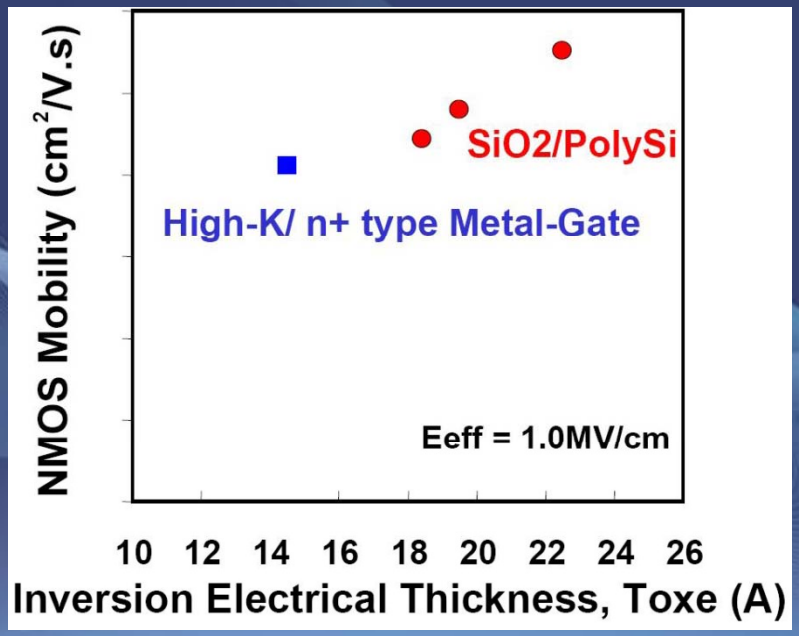


Image courtesy of Intel.

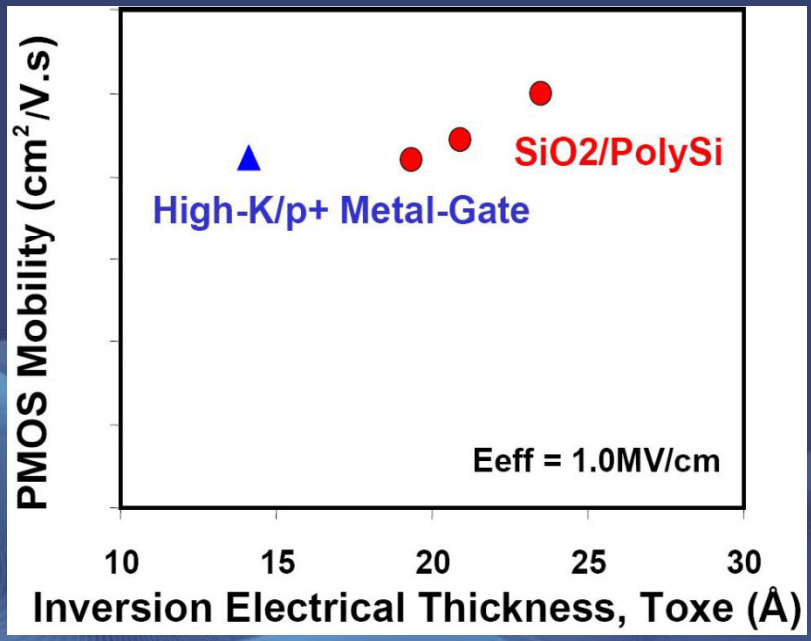
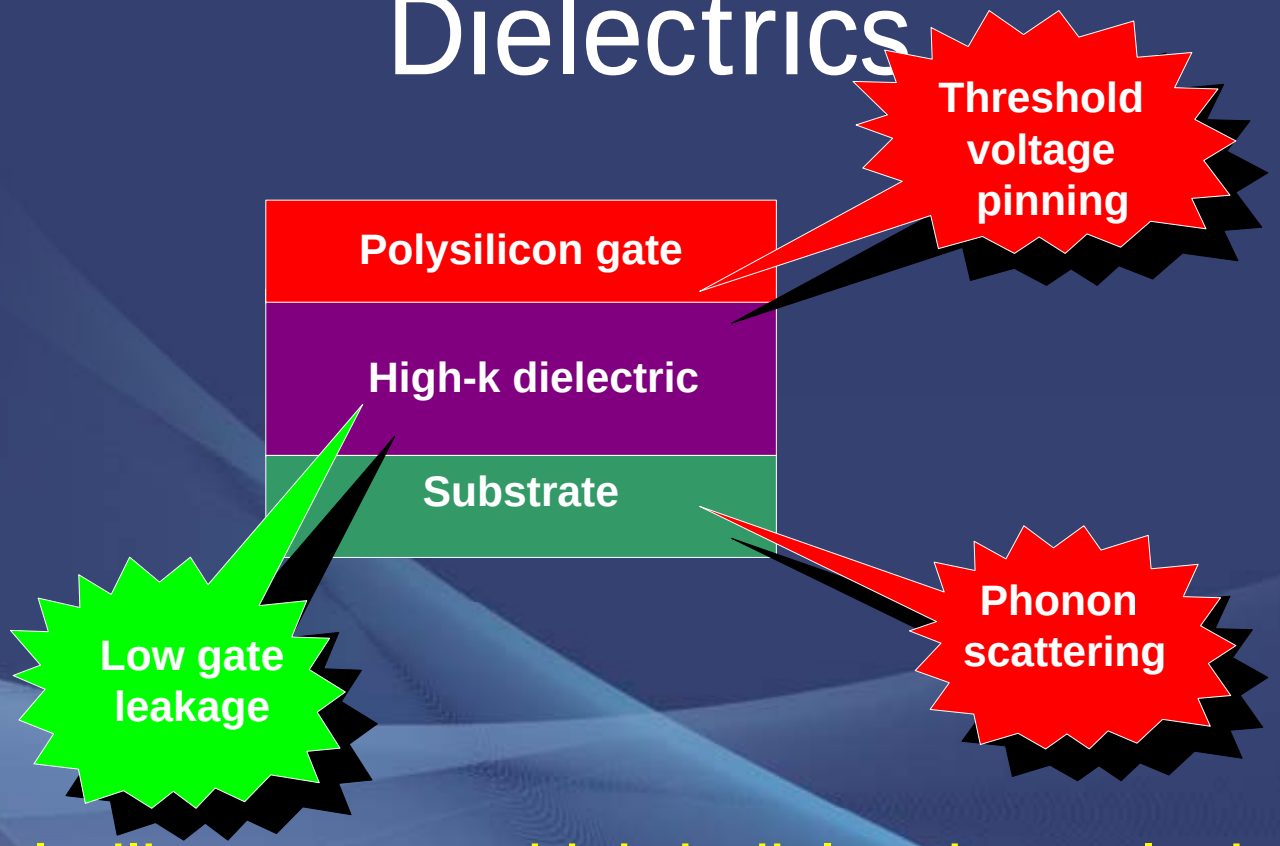


Image courtesy of Intel.

Introduction of High-k Dielectrics



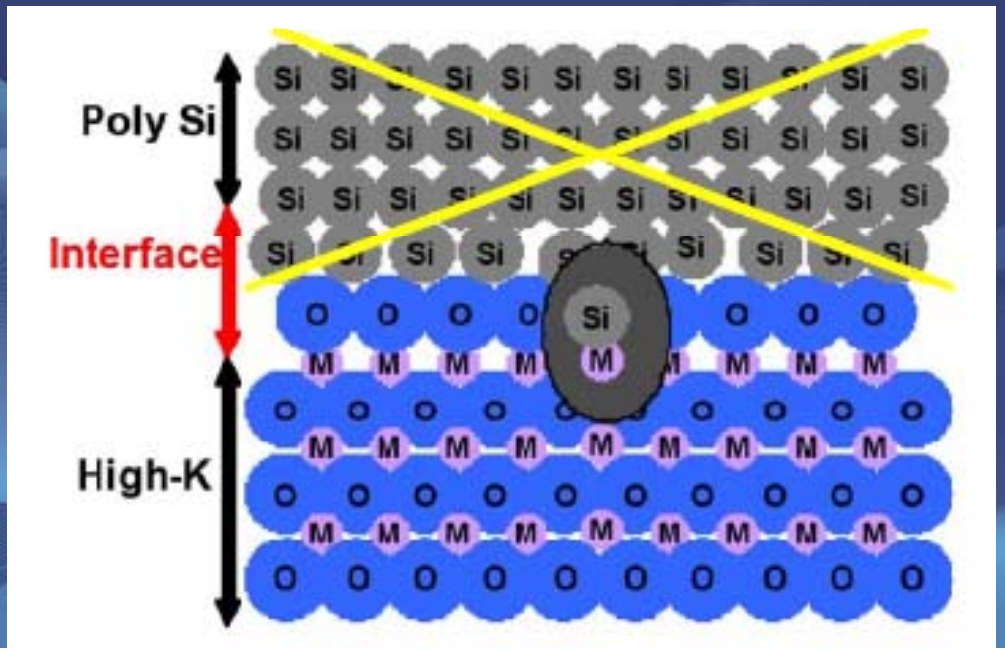
- Polysilicon gate on high-k dielectric results in:

1. Threshold voltage pinning: difficulty in adjusting V_{th}
2. Phonon scattering: reduced carrier mobility

- Solution is to replace polysilicon with metal gate

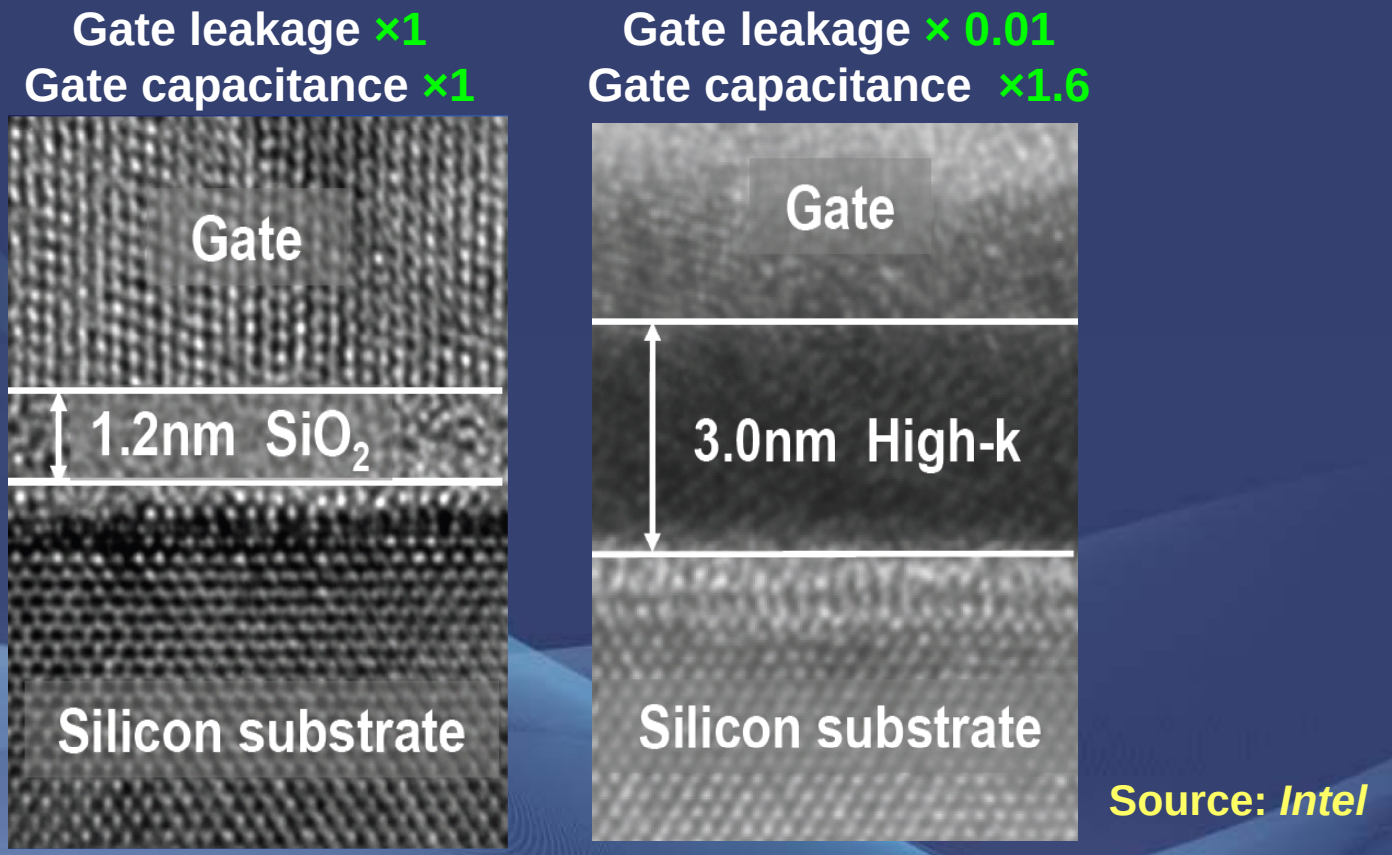
Integrating High K Dielectrics with Metal Gate Electrodes

- Replace poly Si with a metal gate whose work function minimizes Fermi level pinning
- Different metals are required for NMOS and PMOS



R. Chan, AVS5th International Conference on Microelectronics and Interfaces, Santa Clara, California, March 1, 2004.

High-k/Metal Gate Technology



Source: *Intel*

- High-k/metal gate devices offers lower gate leakage with small increase in gate capacitance

High-K Dielectric Performance

- Performance with high-k dielectric and metal gate:

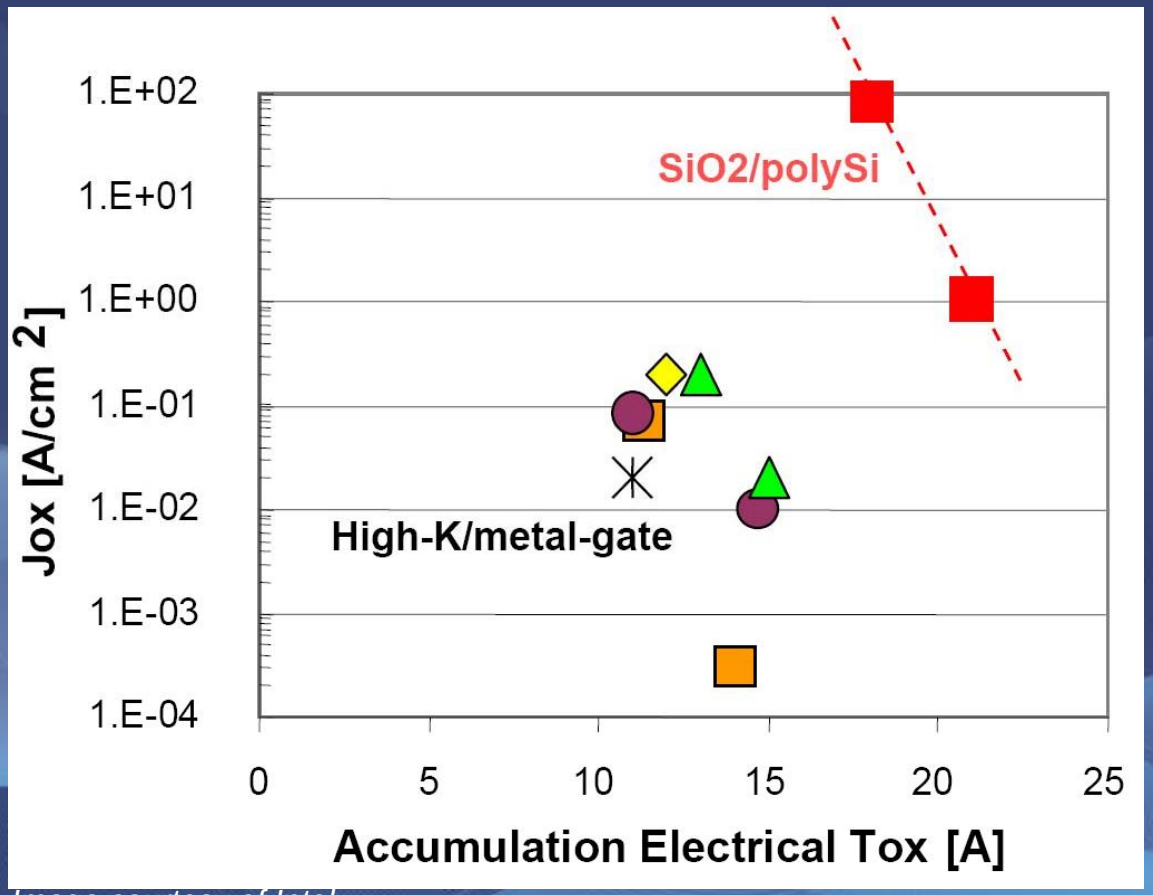


Image courtesy of Intel.

Manufacturing Process

- Several types of high-k dielectric: HfO_2, ZrO_2, TiO_2.
- Chemical vapor deposition:

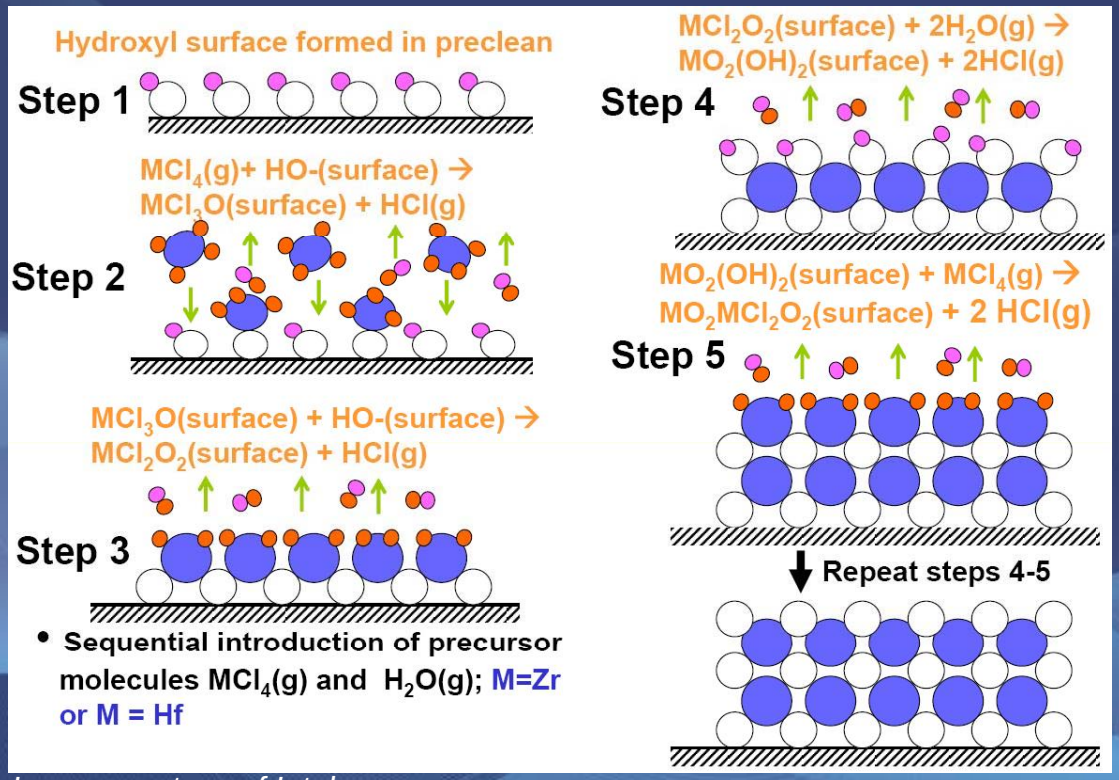
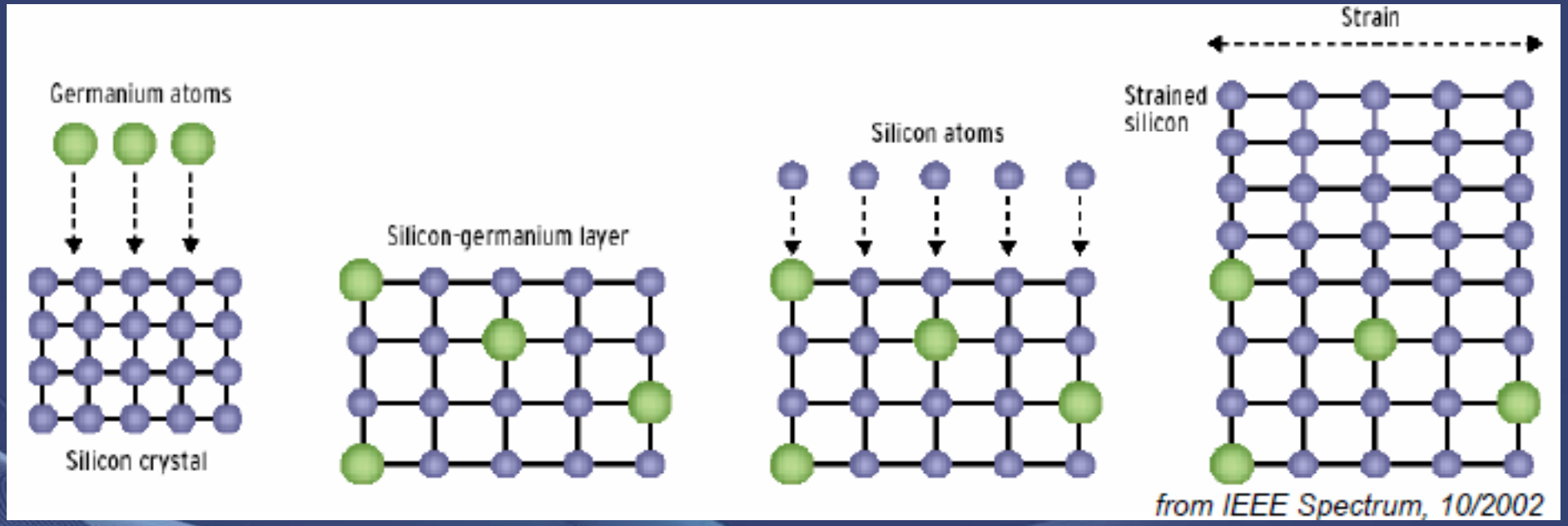


Image courtesy of Intel.

Summary for High-k Gate Oxide

- As transistors shrink in size, an alternative to SiO_2 must be found.
- HfO_2, in conjunction with metal gates, improves leakage current, gate capacitance, and speed.
- By replacing SiO2 with HfO2, transistors will be able to continue to shrink without sacrificing performance.

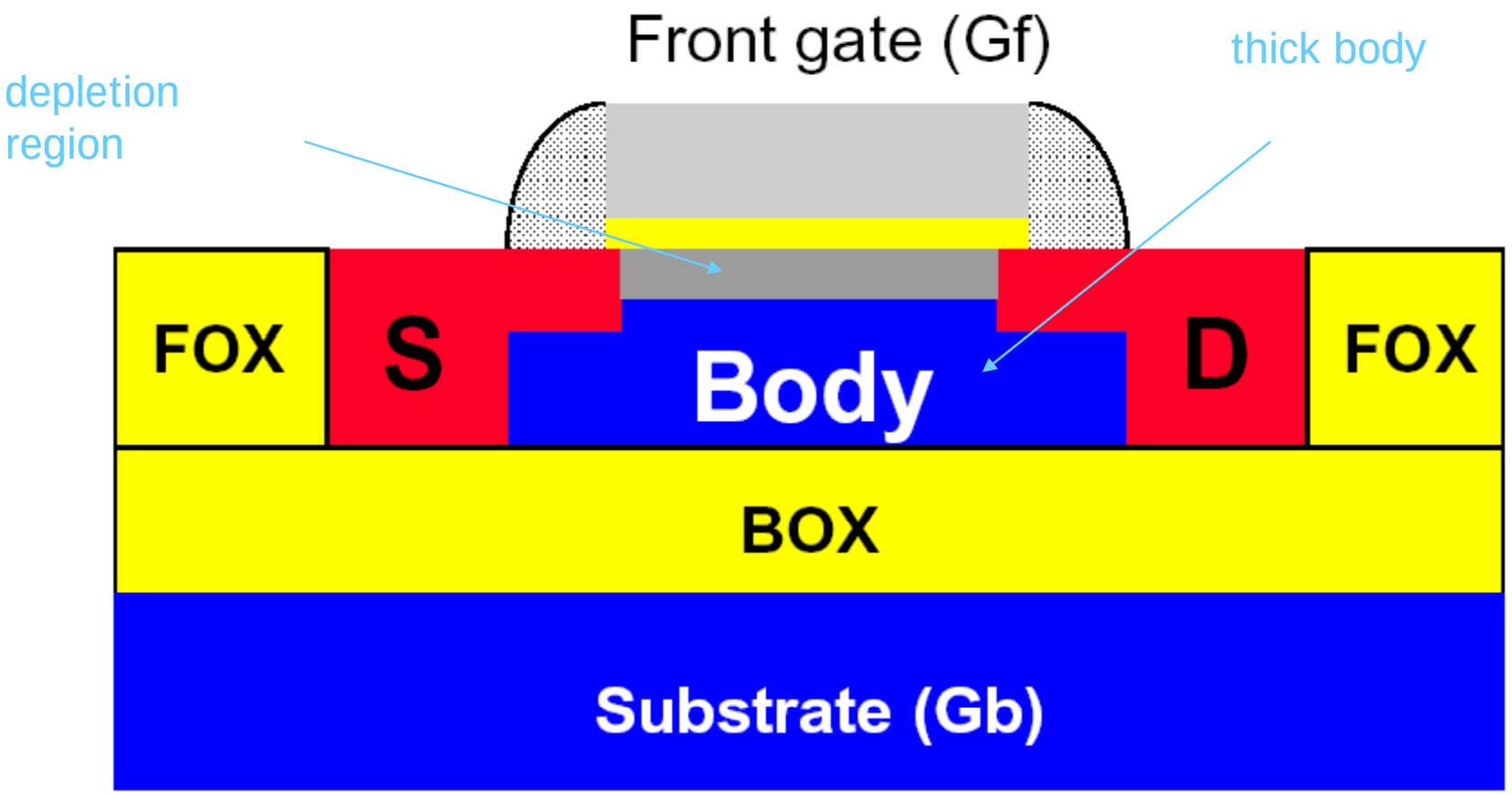
Strained Silicon MOSFET



- Silicon in channel region is strained in two dimensions by placing aSi-Ge layer underneath (or more recently adjacent to) the device layer
- Strained Si results in changes in the energy band structure of conduction and valence band, reducing lattice scattering
- Benefit: increased carrier mobility, increased drive current (drain current)

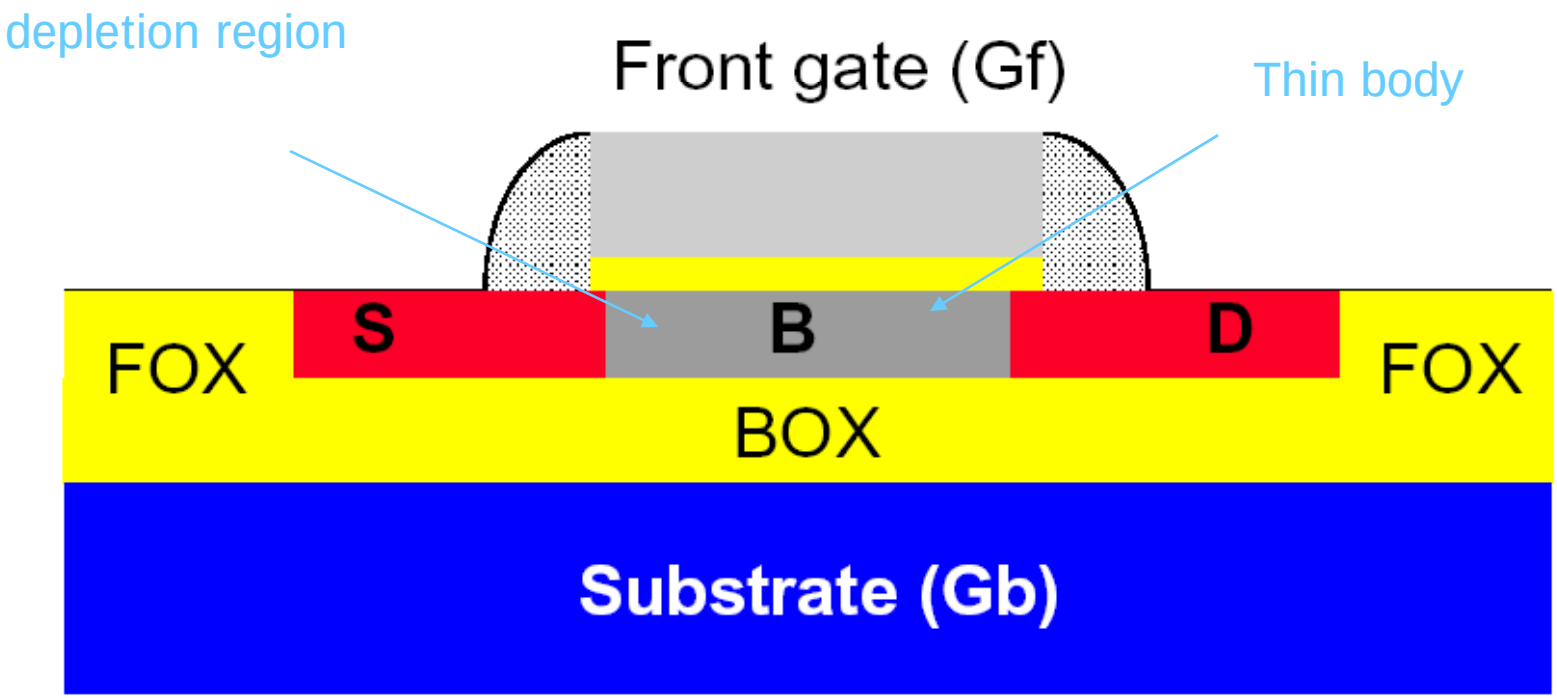
SOI and FINFET Devices

basic structures



Partially depleted (PD) body
(similar to bulk MOSFET but the body **floats**)

basic structures



Fully depleted (FD) body

Partially Depleted vs. Fully-Depleted

- Recall that depletion region empty of free carriers forms in the BULK beneath the gate
- Partially-depleted SOI
  - The body is thicker than the depletion region, so bulk voltage can vary depending on the amount of charge present
  - **This varying charge changes Vt because of the body effect**
- Fully-depleted SOI
  - Body is thin, depletion region spans bulk
  - Body charge is fixed, body voltage does not change

Another View

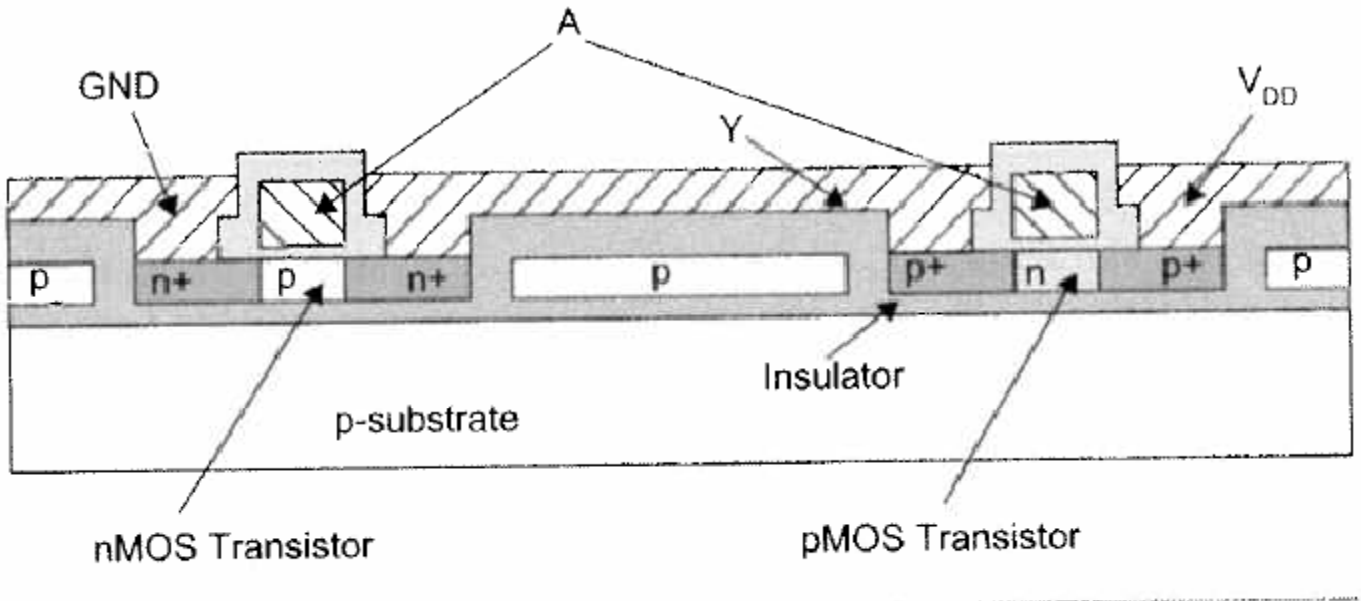


FIG 6.69 SOI inverter cross-sections

Source: Weste/Harris

benefits of SOI

-Simple IC processing (isolation)

-Higher density

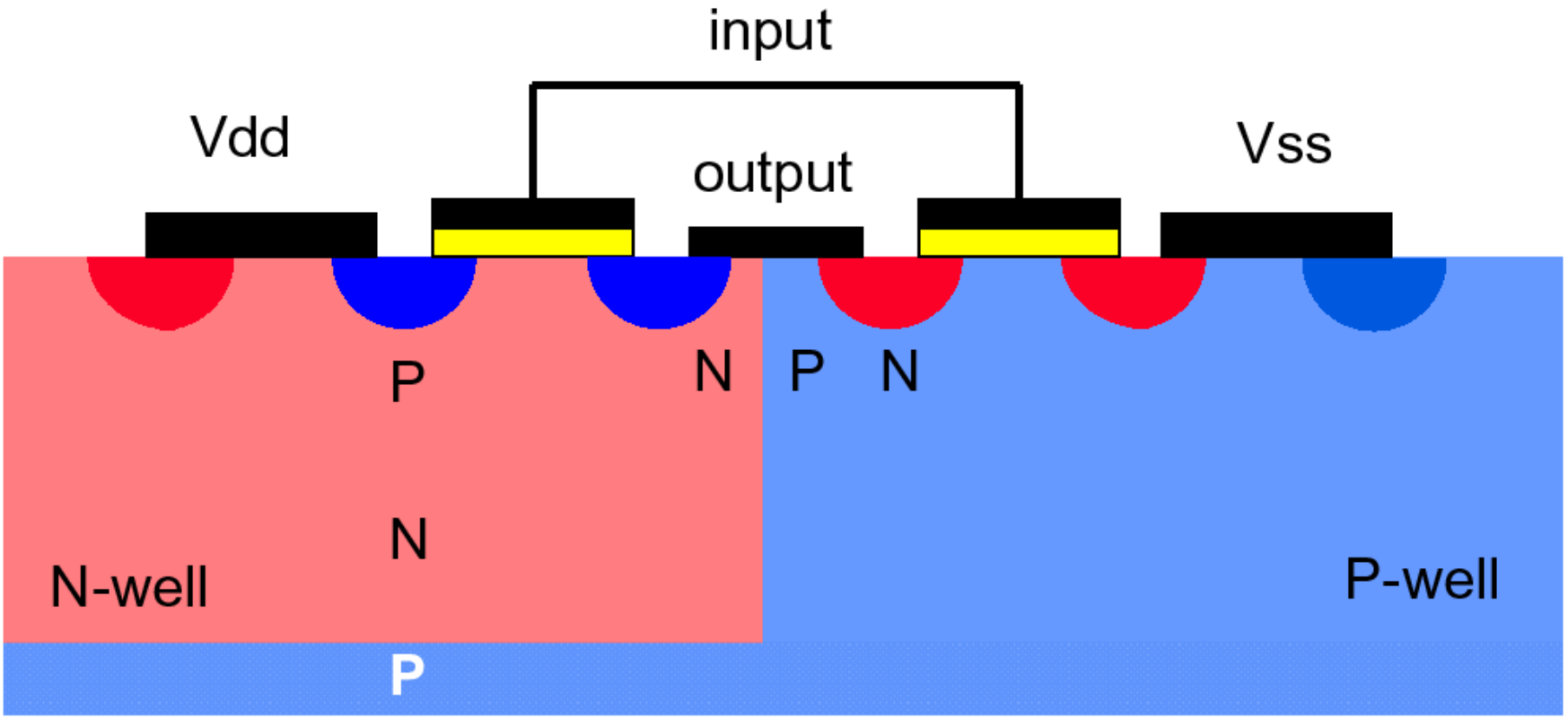
-Reduced S/D junction capacitance (speed/power)

-Low soft-error rate

-No latch-up

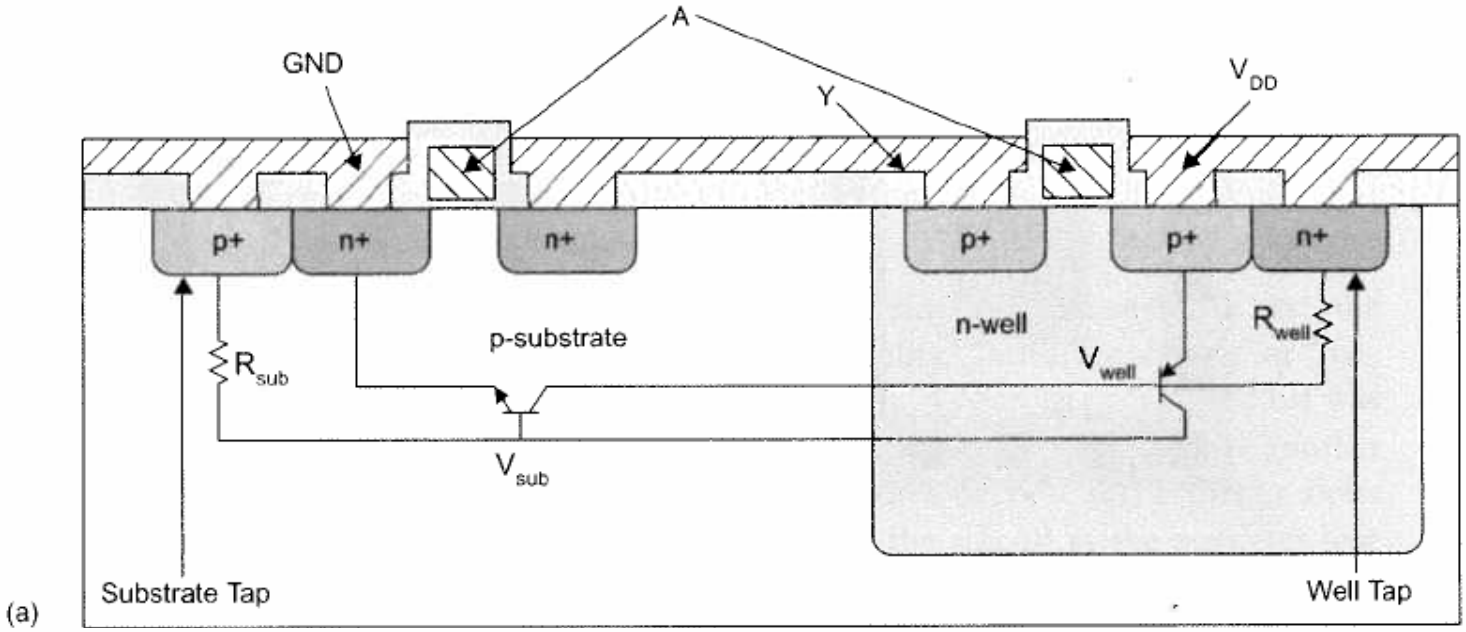
-No (normal) body effect

benefits of SOI



Parasitic bipolar devices → “latchup”

CMOS Latchup



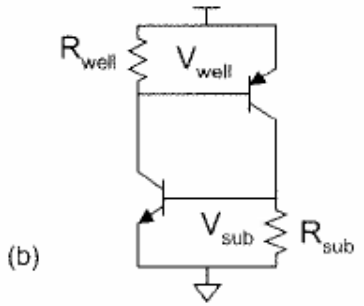


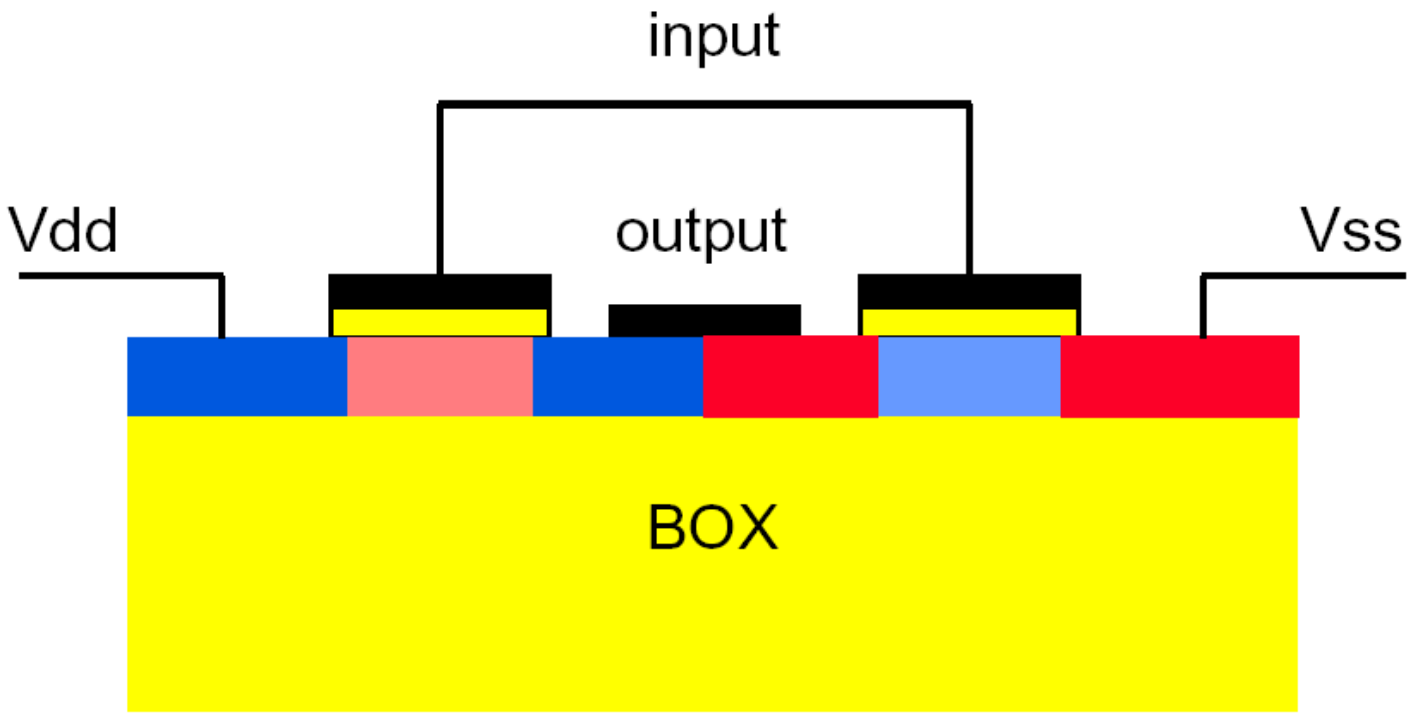
FIG 4.63 Origin and model of CMOS latchup

Source: Weste/Harris

Transient currents flowing in substrate during startup can cause VSUB to rise, turning on Vsub. This will turn on Vwell, which turns on Vsub harder in a positive feedback loop, causing large current to flow between Vdd/GND (destructive current!).

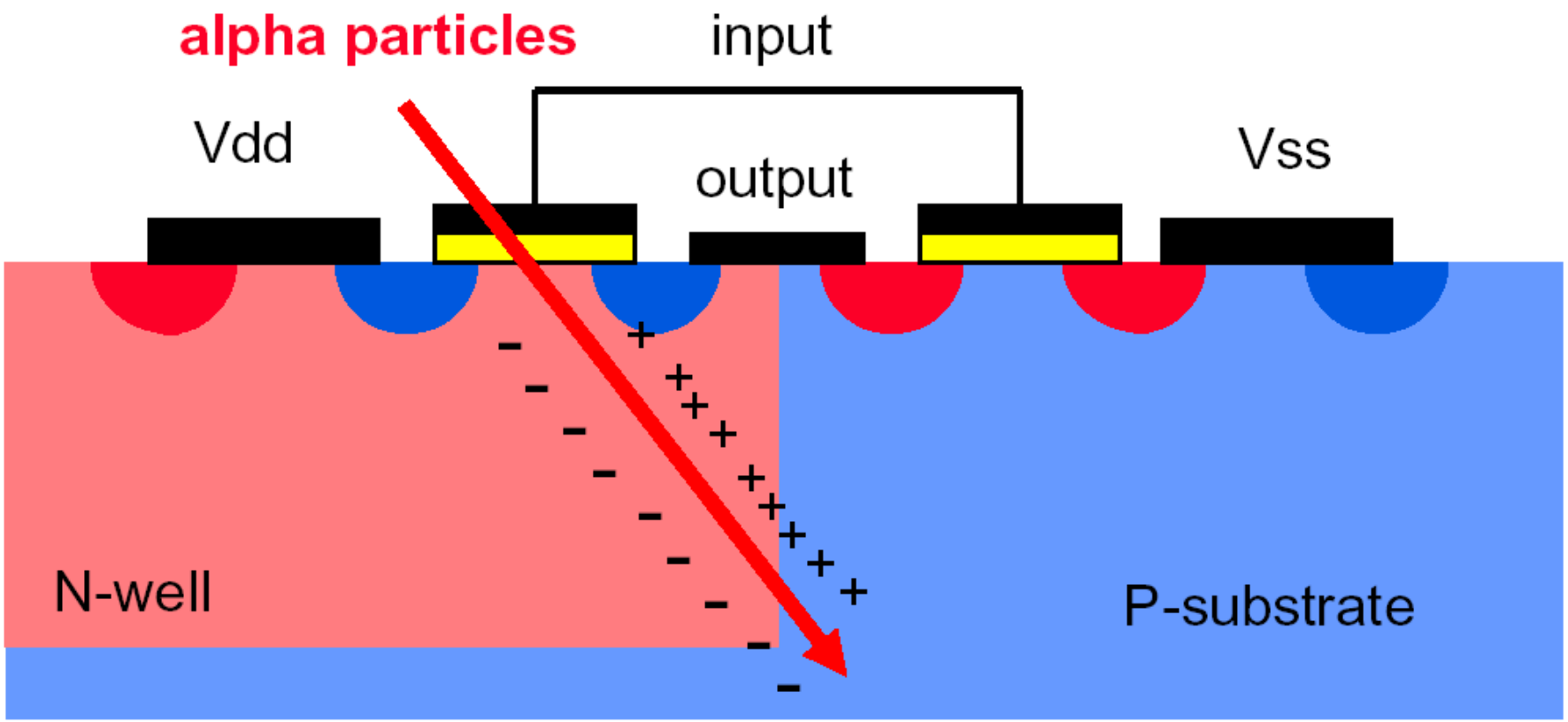
Keep Rwell, Rsub low, also place numerous well taps to collect stray charge

benefits of SOI (ii)



No parasitic bipolar devices ➡ no latchup

soft errors in bulk CMOS

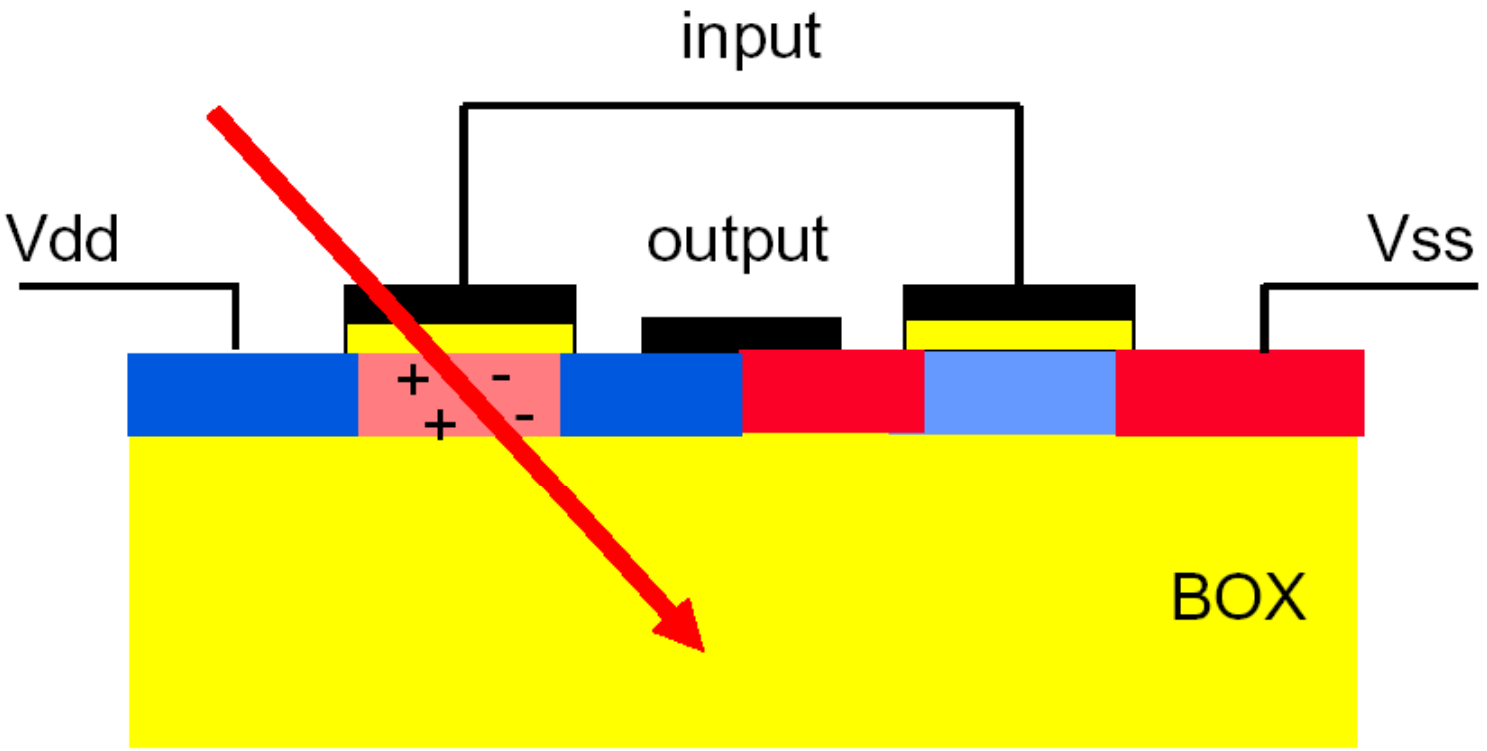


Alpha particles → "soft" errors

Alpha Particles

- Sources
  - Cosmic Rays (aircraft electronics vulnerable)
  - Decaying uranium and thorium impurities in integrated circuit interconnect
- Generates electron-hole pairs in substrate
  - Excess carriers collected by diffusion terminals of transistors
  - Can cause upset of state nodes – floating nodes, DRAM cells most vulnerable

soft errors in SOI

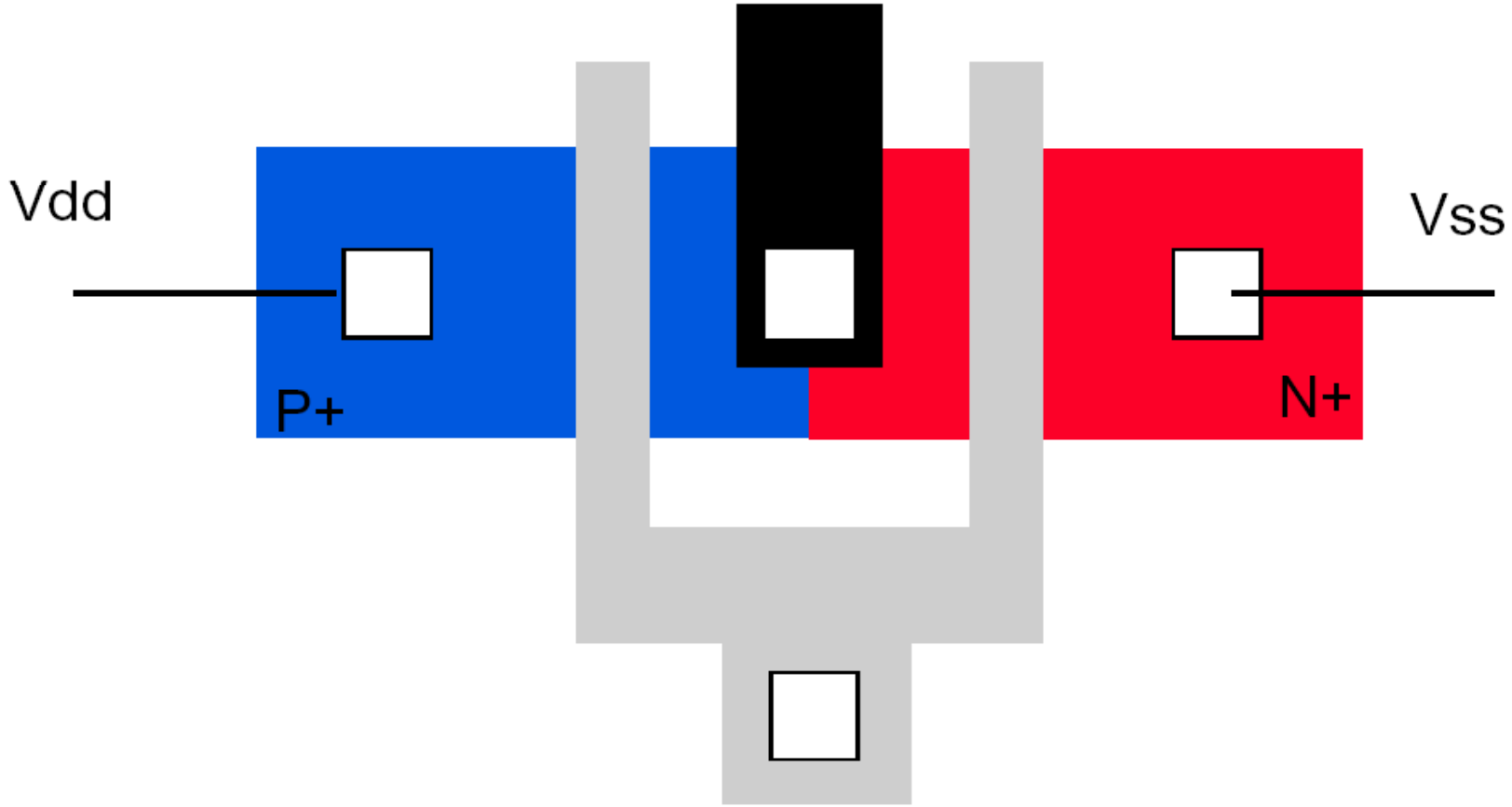


Not as much substrate to generate charge in!

Low soft error rate

layout for bulk CMOS

layout for SOI



Simpler isolation → simpler process → smaller layout

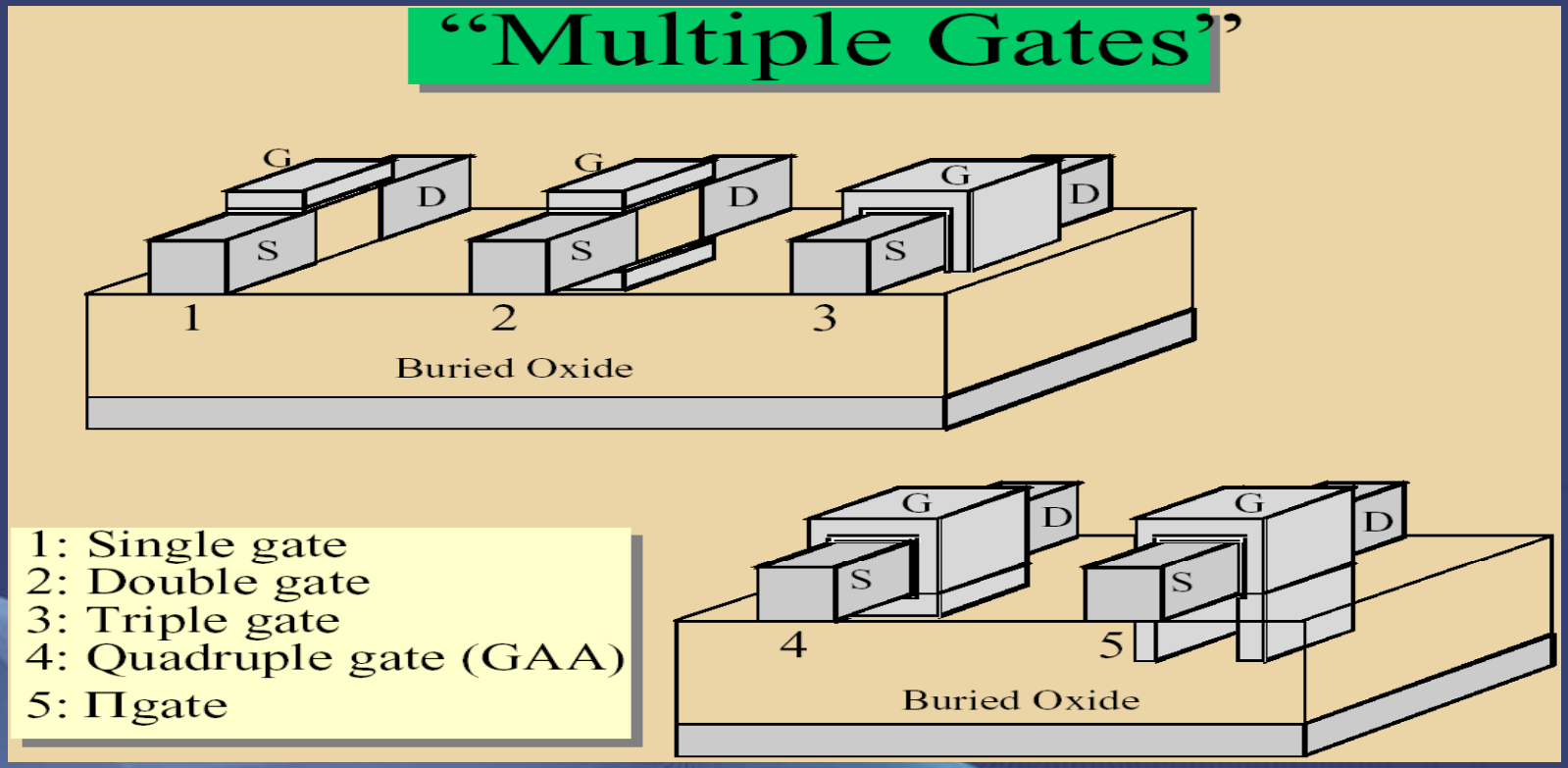
Another subtle advantage: Lower Vt

- In bulk-CMOS, Vt varies with channel length
  - variations in polysilicon etching shows up as variations in threshold voltages
  - Vt must be high enough in the worst case (lowest Vt) to limit subthreshold leakage, so nominal threshold must b higher
- SOI has lower Vt variations than bulk-CMOS
  - So nominal Vt can be lower, resulting in faster circuits, esp. for lower VDD

SOI Disadvantages

- Floating body causes the ***History Effect***
  - Body voltage depends on if device has been idle or switching
  - This changes Vt, which changes the delay of the circuit
  - Circuit delay changes with its “history” of switching activity!
  - Matches matching transistors for analog designs difficult because even if transistors are next to each other, can have different characteristics because of changing VT
- Self-heating
  - The oxide is good thermal insulator as well as electrical insulator
  - Heat accumulates in switching transistors rather than spreading throughout the substrate, slow them down.
  - A problem for large transistors that switch fast, i.e, clock buffer transistors.

Why Multi-Gate SOI MOSFETs ?



- Higher current drive => better performance
- Prophesized to show higher tolerance to scaling
- Better integration feasibility, raised source-drain structure, ease in integration
- Larger number of parameters to tailor device performance

What does FinFet look like

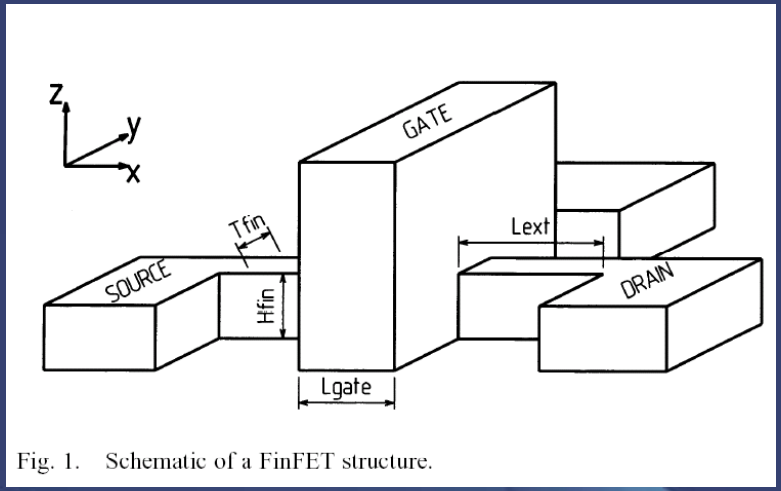
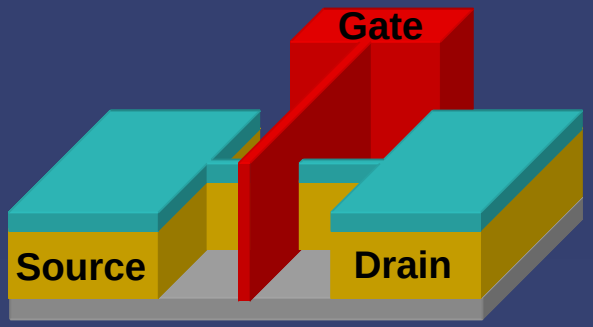
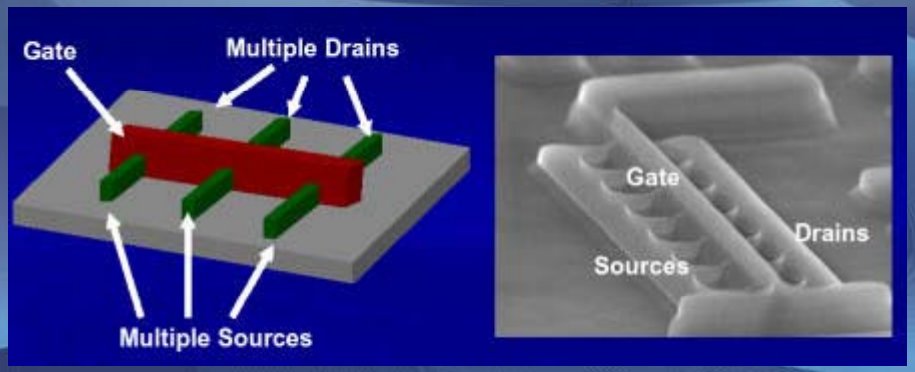


Fig. 1. Schematic of a FinFET structure.

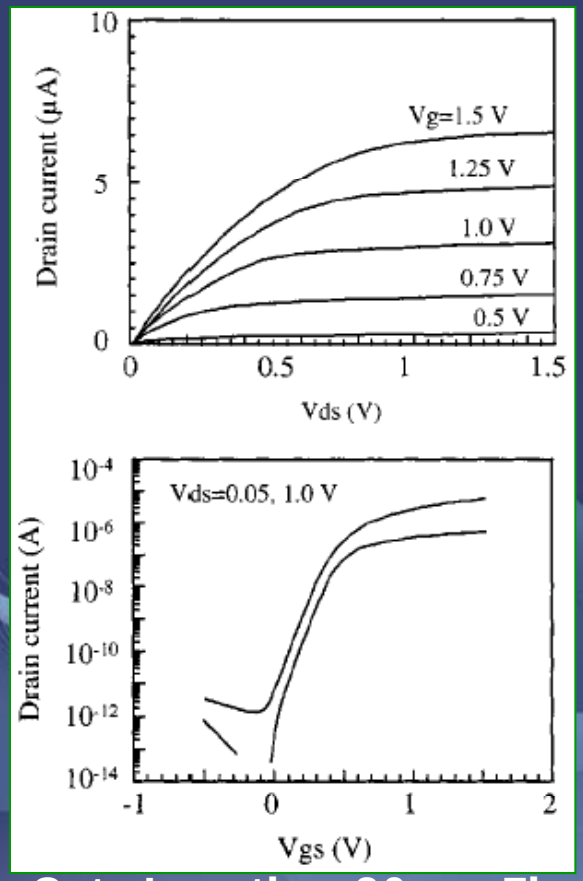


3D view of FinFET

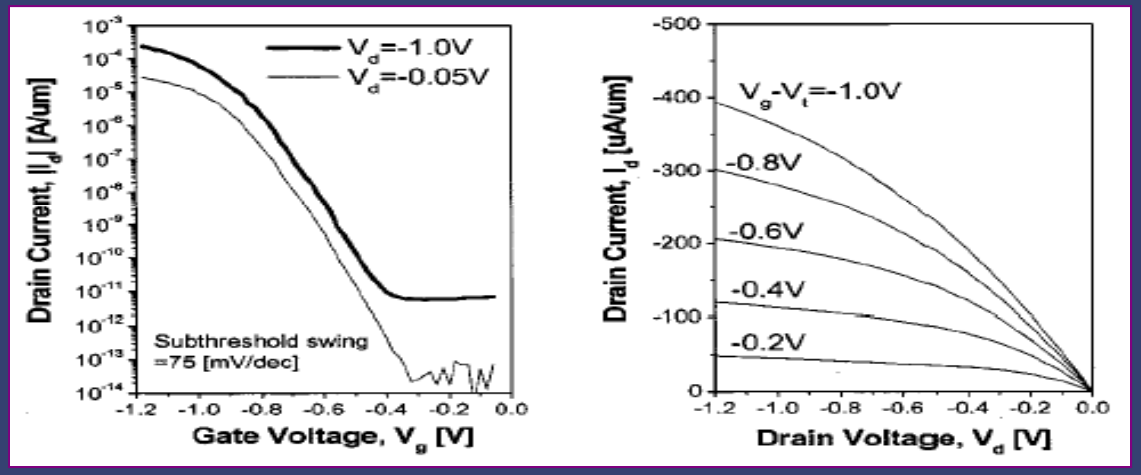


3D view of multi-fin FinFET

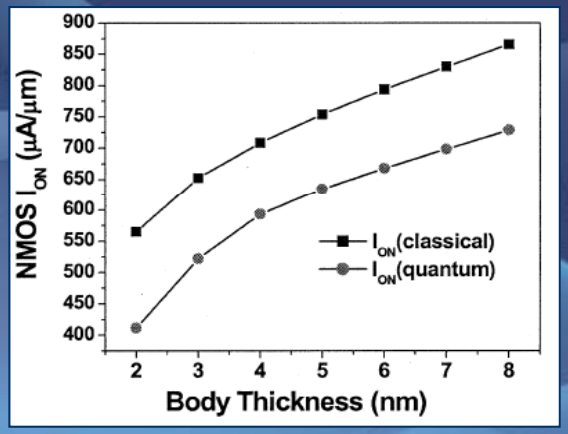
UC Berkeley Results – FinFET/ Double Gate (2000-04)

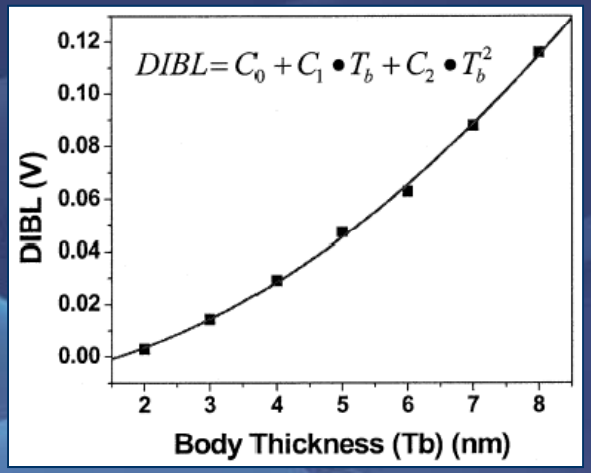


Gate Length = 30nm, Fin Width =20nm



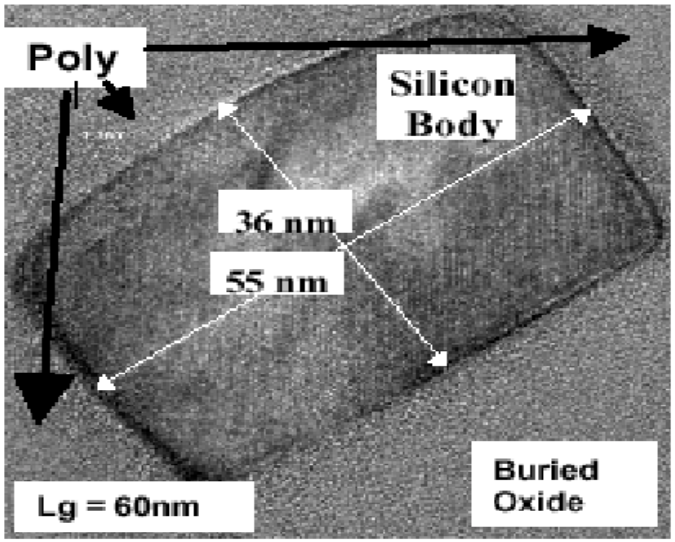
Gate Length = 30nm, Oxide thickness =2.1nm

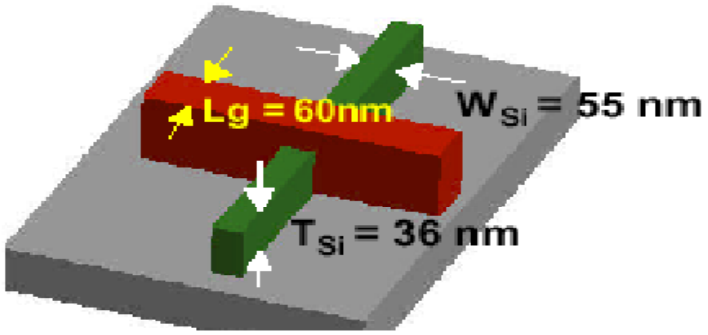




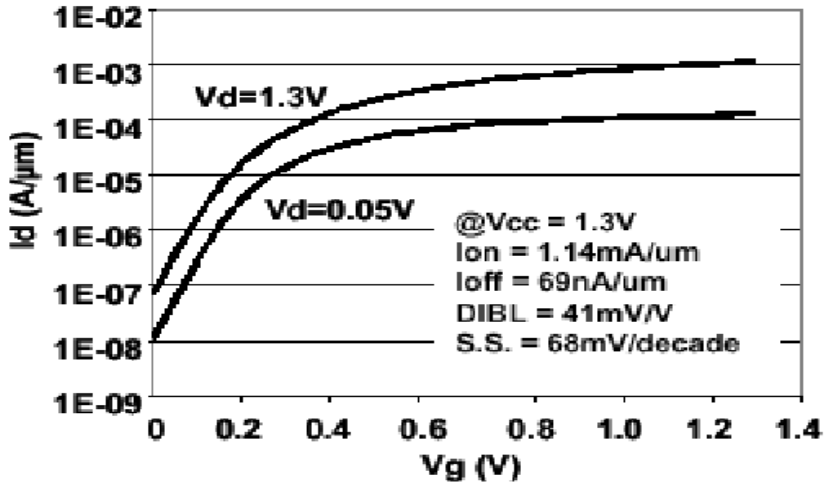
Gate Length = 20nm

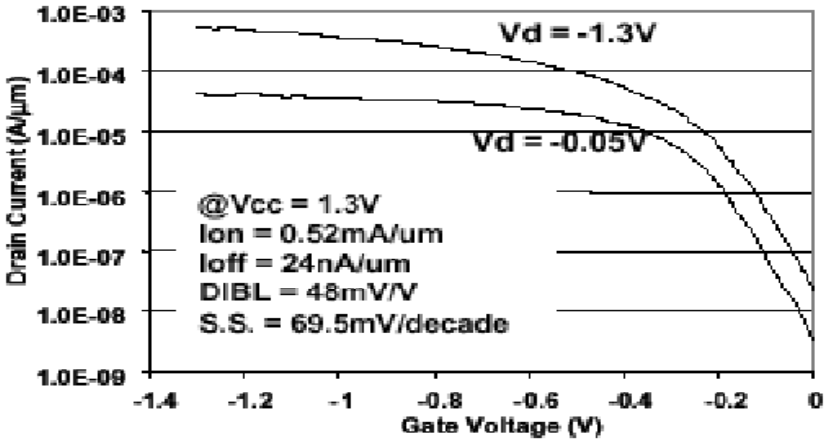
INTEL's TriGate SOI (SSDM 2002)





Current per unit width = $I_d/(2*T_{Si}+W_{Si})$

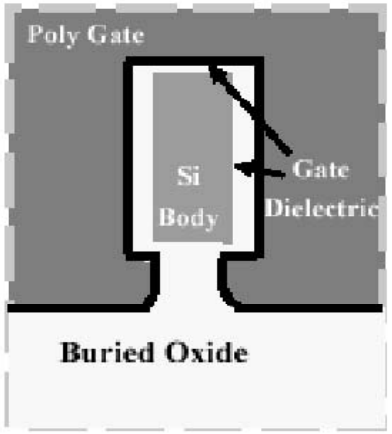


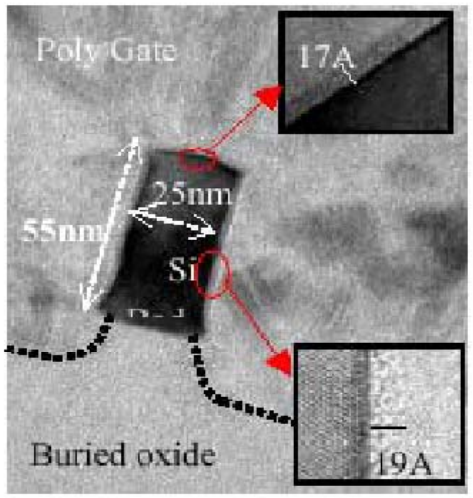


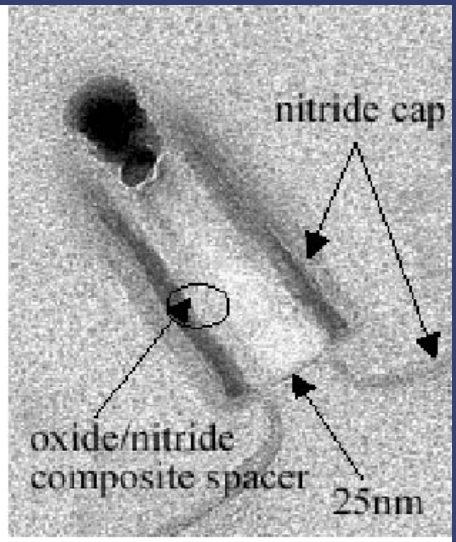
Highest ever performance reported for NMOS and PMOS devices on a single substrate !!

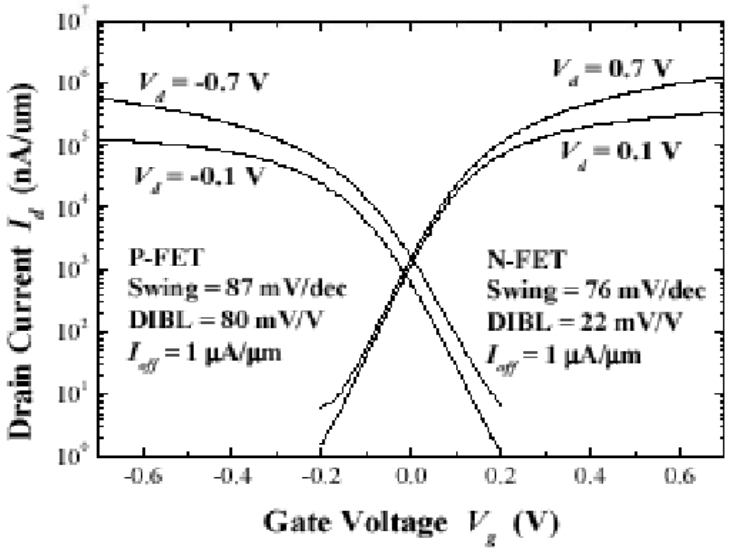
TSMC's Ω-gate Device (SSDM-2002)

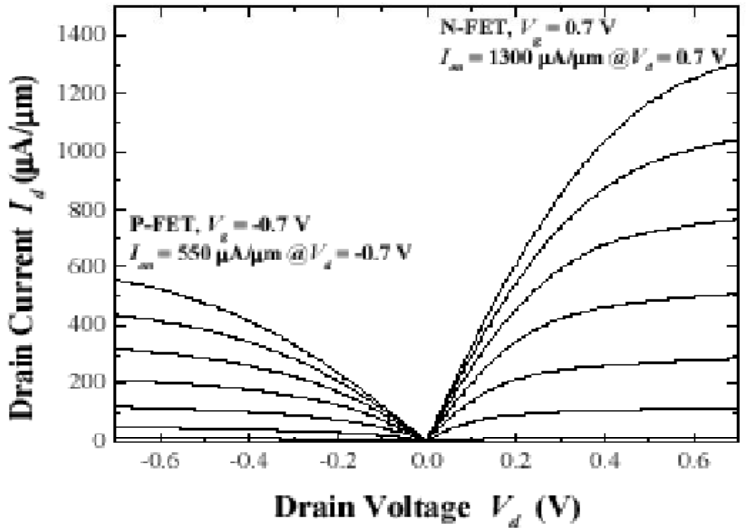
TSMC's Ω-gate (IEDM'02)



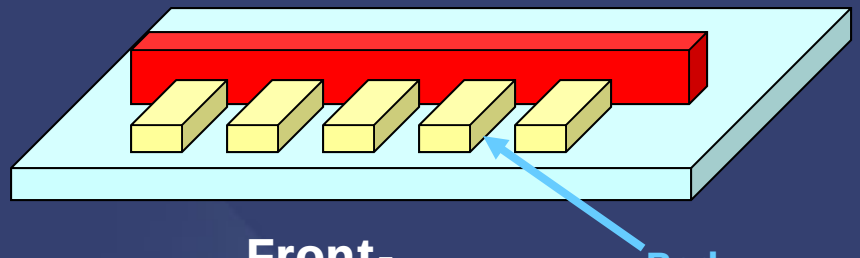




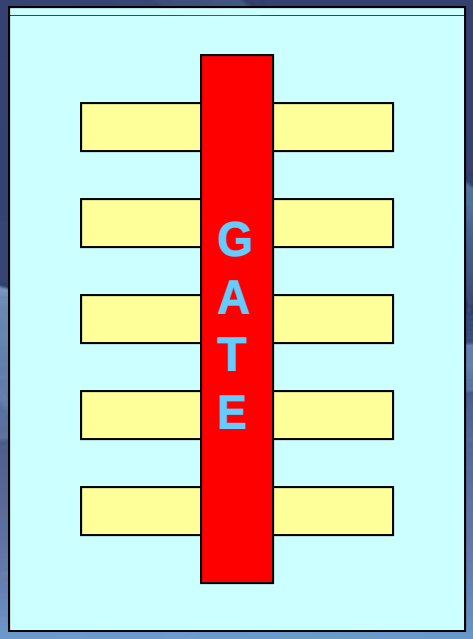




Multi-Body Single-Gate Devices



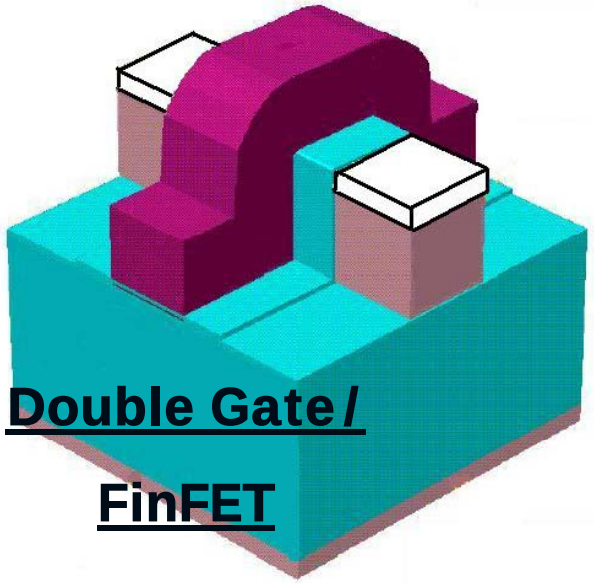
Front-View



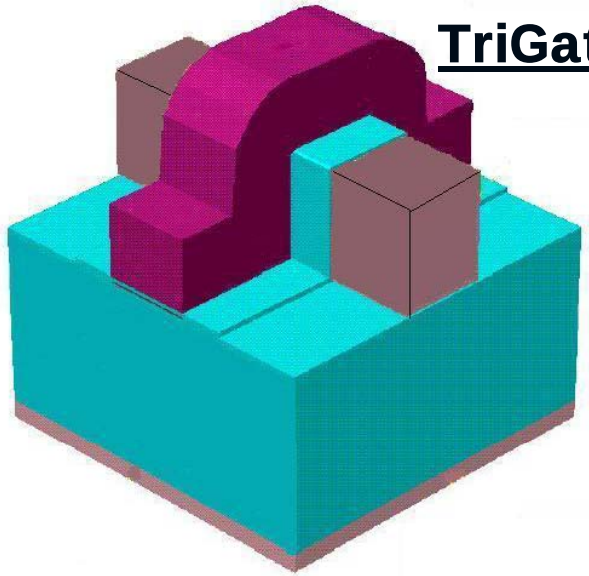
Top-View

- Multi-Body Single gate devices an attractive option.
- Increased current drive using a single gate.
- Total current nearly equals the current thru one body multiplied by the number of body regions.
- Fabrication feasibility.
- Feasible for the Dual-Gate, Tri-Gate and Ω-gate devices.

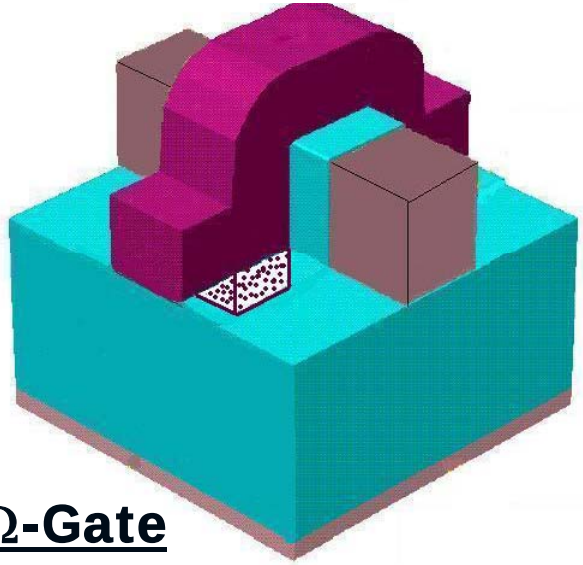
Multi-Gate SOI MOSFETs (3-D Views)



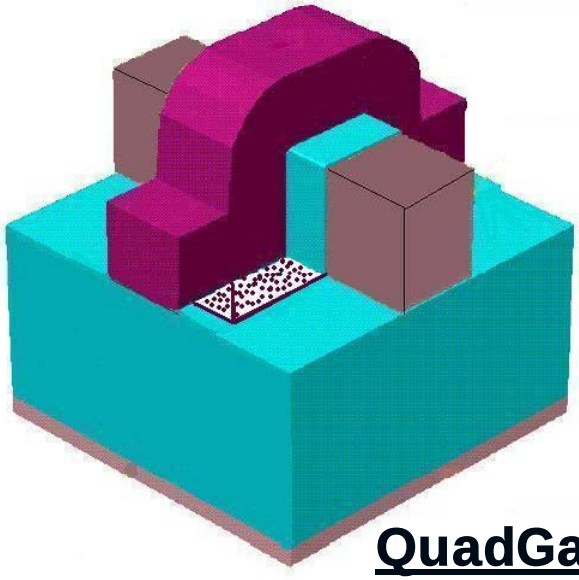
Double Gate / FinFET



TriGate



Ω-Gate



QuadGate