ECE 225
High-Speed Digital IC Design
Lecture 12

Steep Subthreshold Slope Devices:
Tunneling Field-Effect-Transistors

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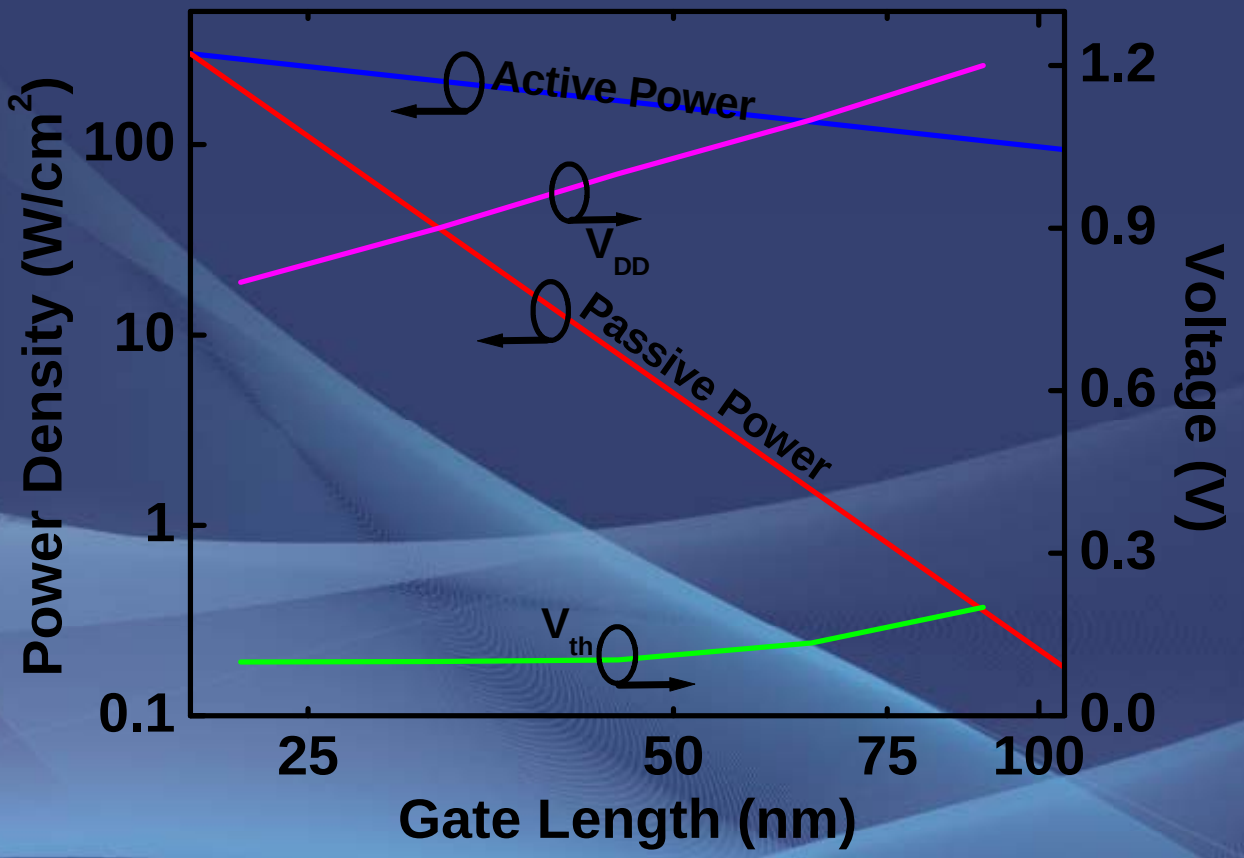
Gate Length Scaling Trends

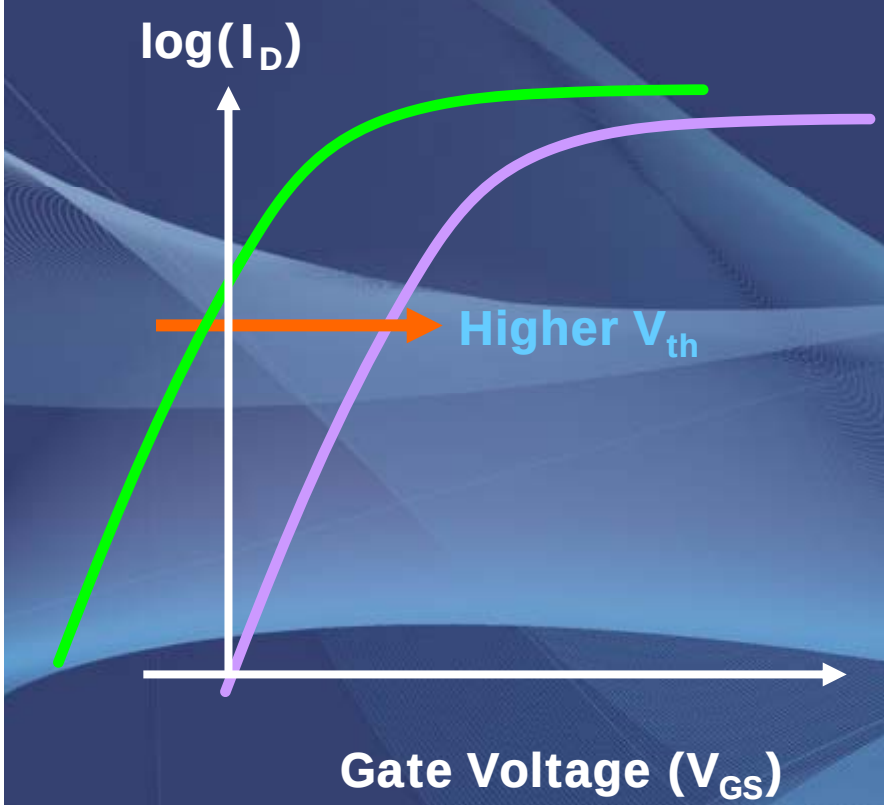


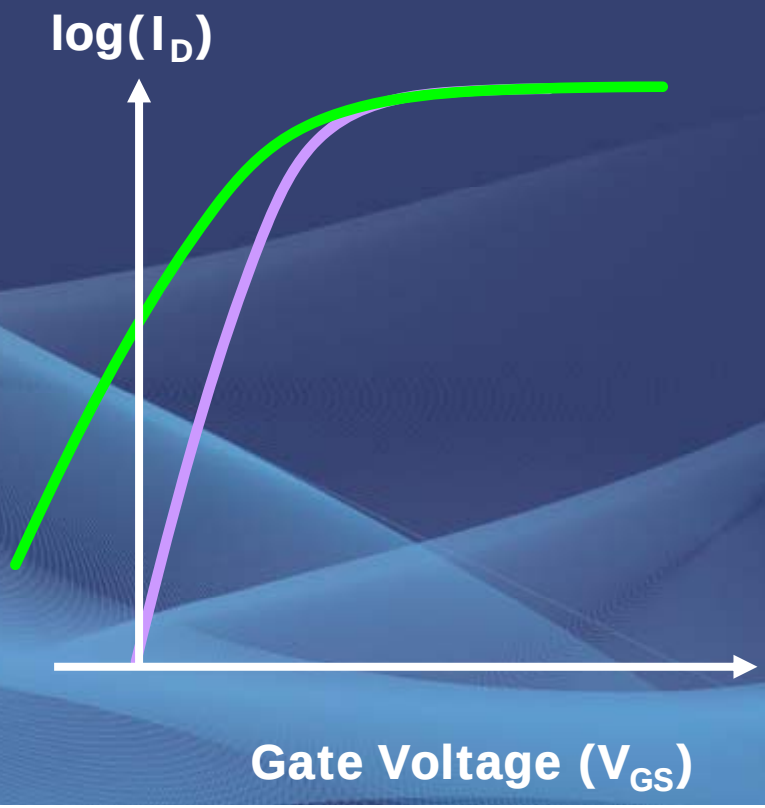
Puri *et. al., Nano Lett.*, 2003

Off-State Leakage Current

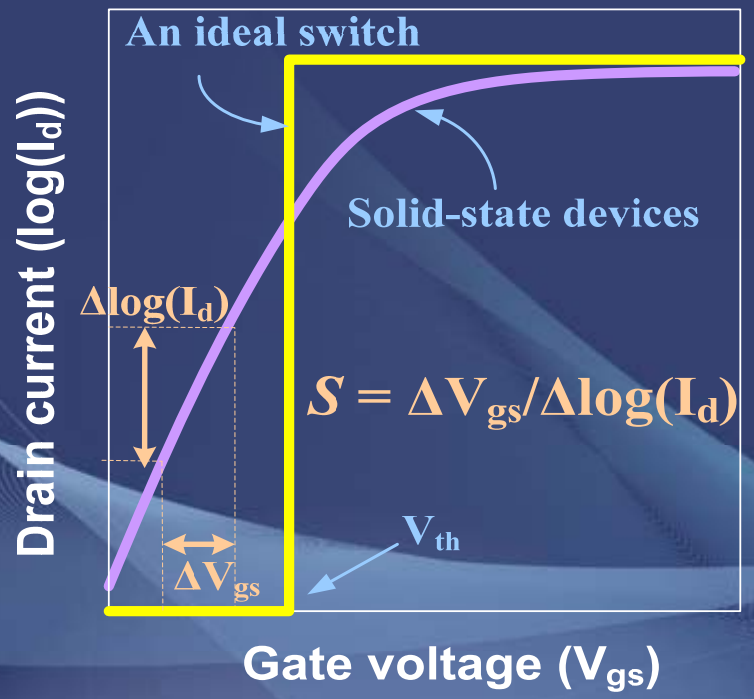
- Generally high V_{th} is needed to reduce leakage current.
- High V_{th} reduces ON current

- V_{th} remains constant by reducing the subthreshold swing in tunnel FETs
- Off current can be reduced by several orders





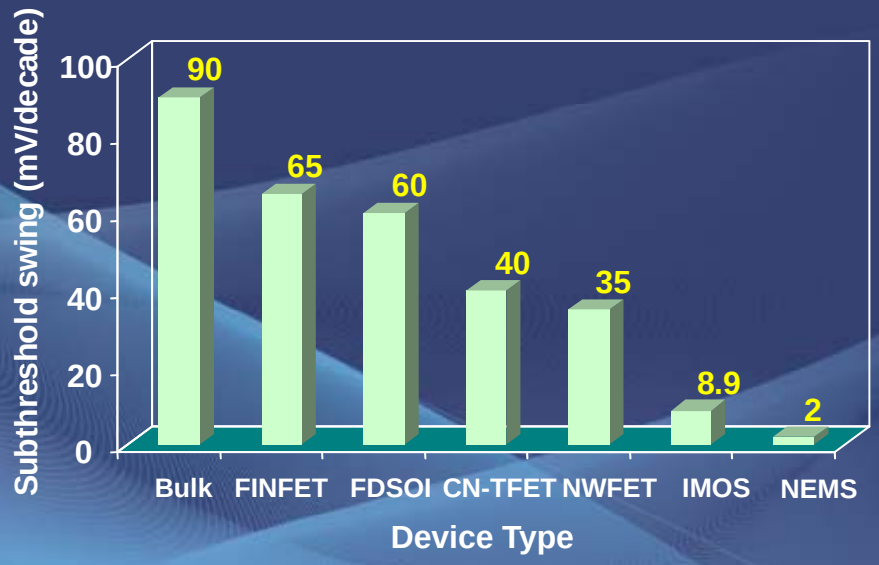
Sub-threshold Slope Engineering



$$S = \left(\frac{d[\log I_d]}{dV_g} \right)^{-1} = \left(1 + \frac{C_{dm}}{C_{ox}} \right) \frac{kT}{q} \ln 10$$

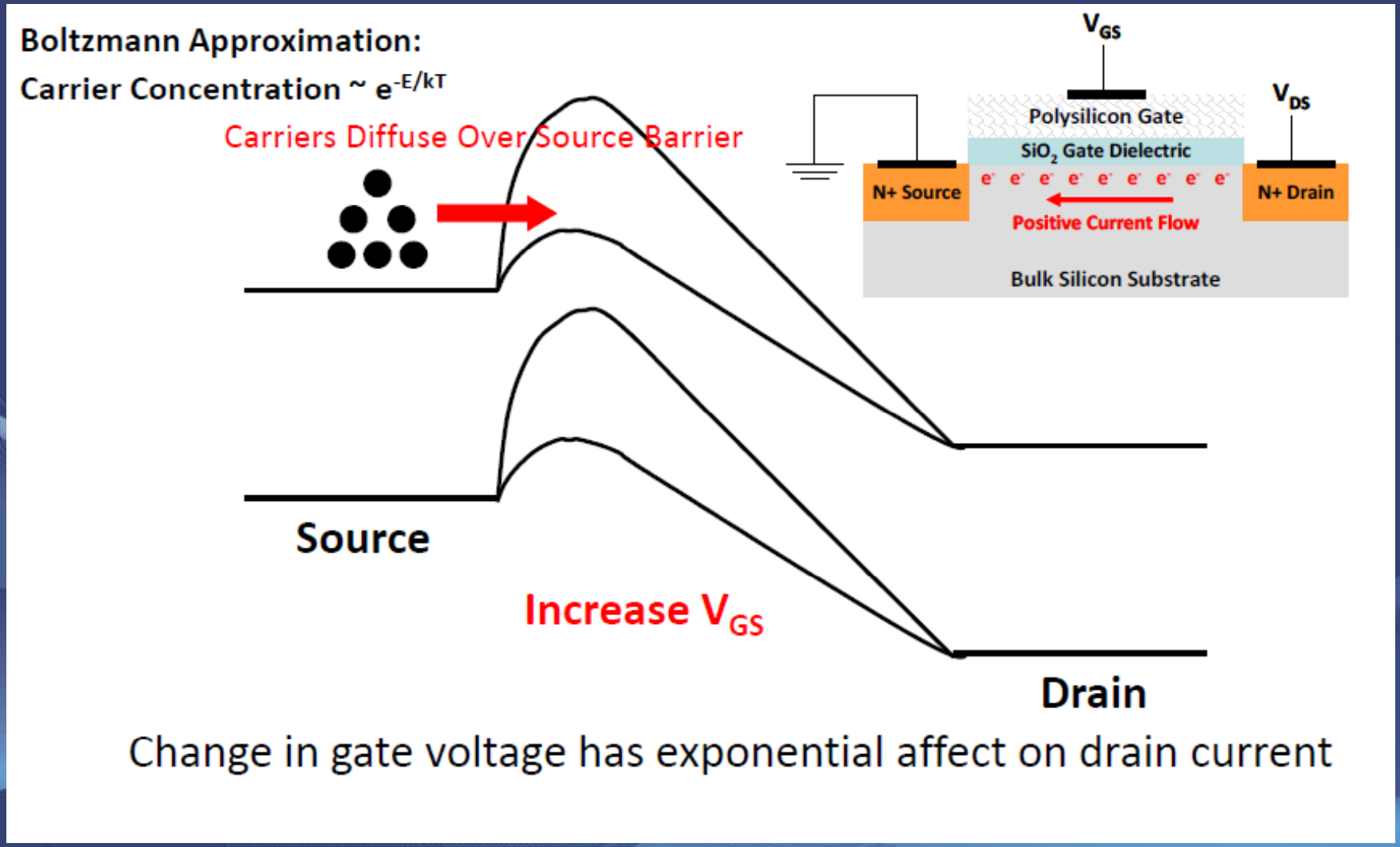
NEM-FET, NWFET, Fe-FET

TFET, IMOS



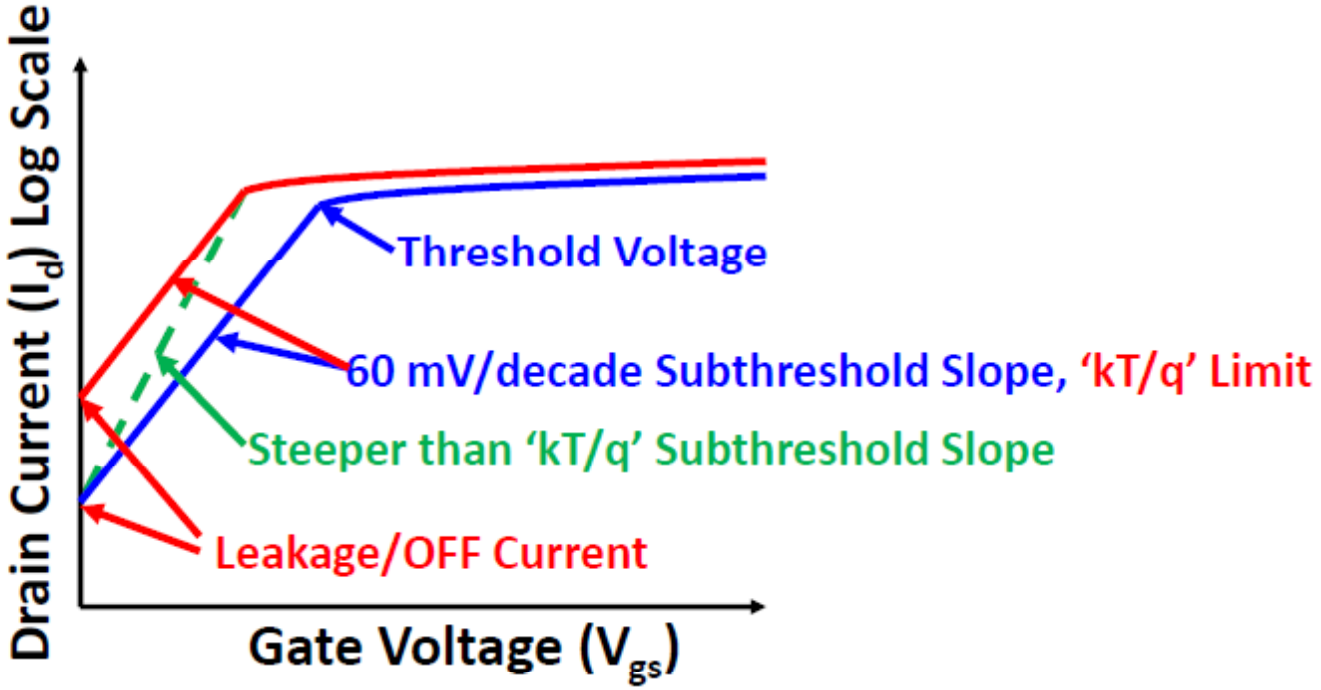
Dadgour et al., *DAC 2007*

MOSFET Carrier Transport



Change in gate voltage has exponential affect on drain current

MOSFET Subthreshold Slope



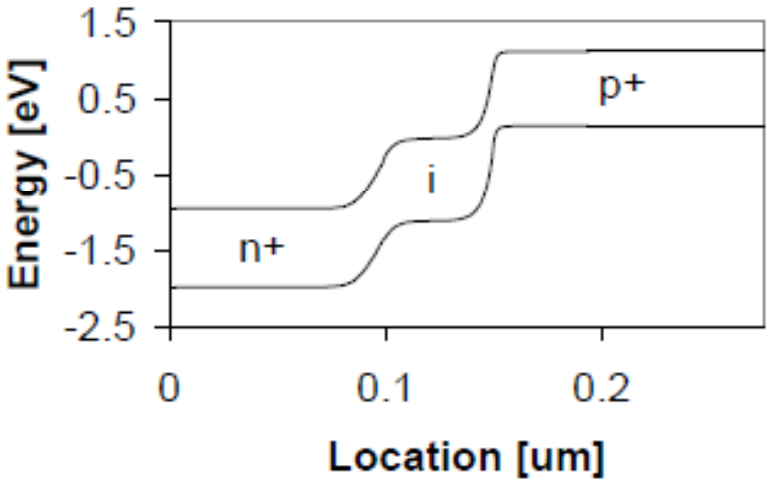
$$S = \left(\frac{d \log I_D}{dV_G} \right)^{-1} = \left(1 + \frac{C_{dm}}{C_{ox}} \right) \frac{kT}{q} \ln(10) \geq \ln(10) \frac{kT}{q}$$

Leakage current increases ***exponentially*** as device is scaled

Tunnel FET Operation

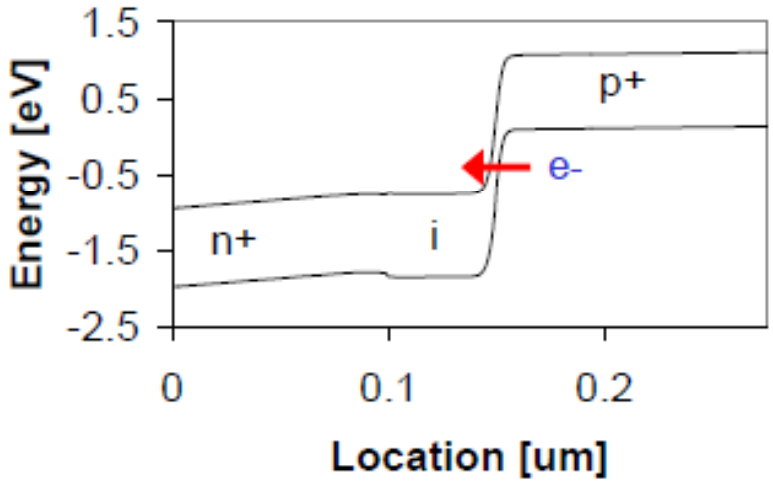
OFF-state

- V_d = positive
- V_g = 0
- no current flows

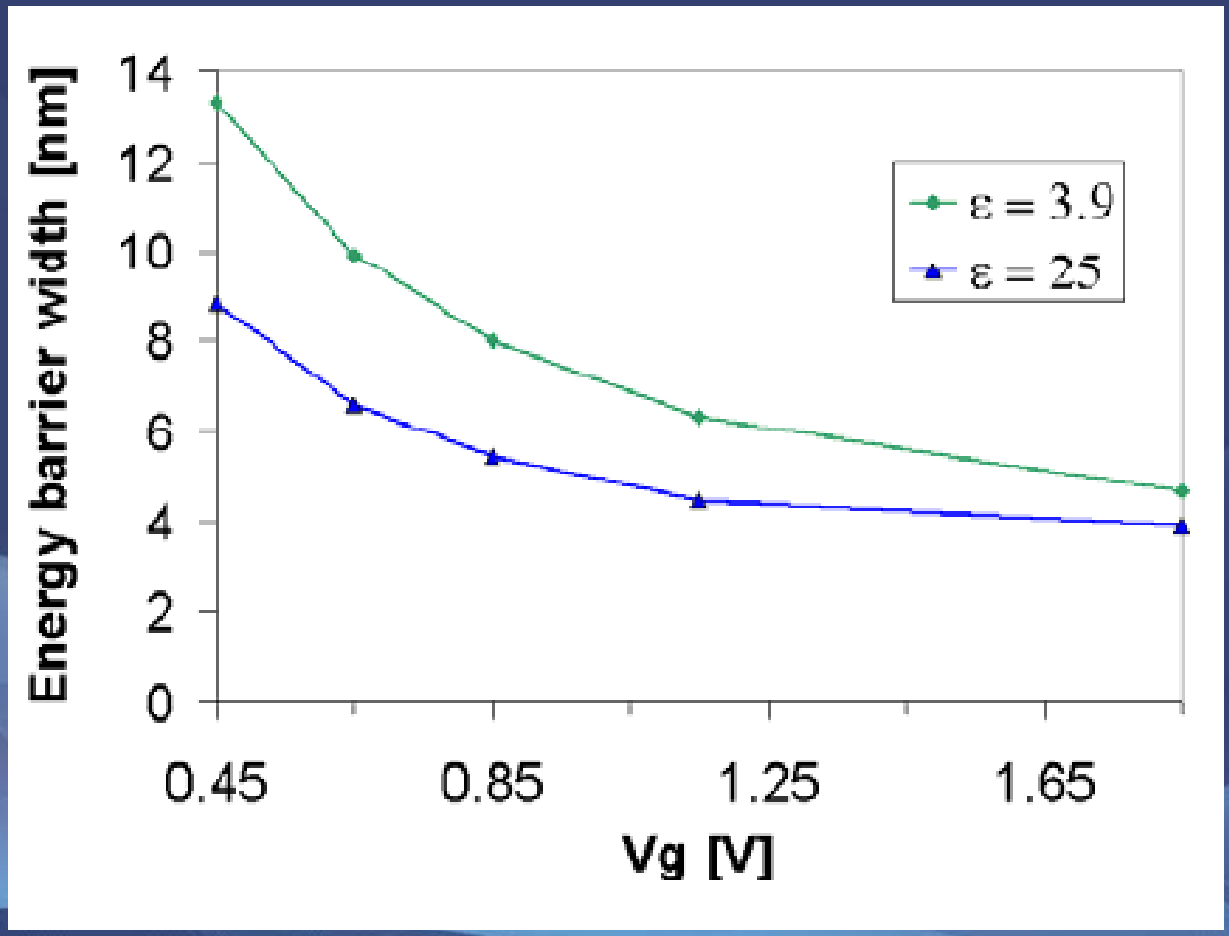


ON-state

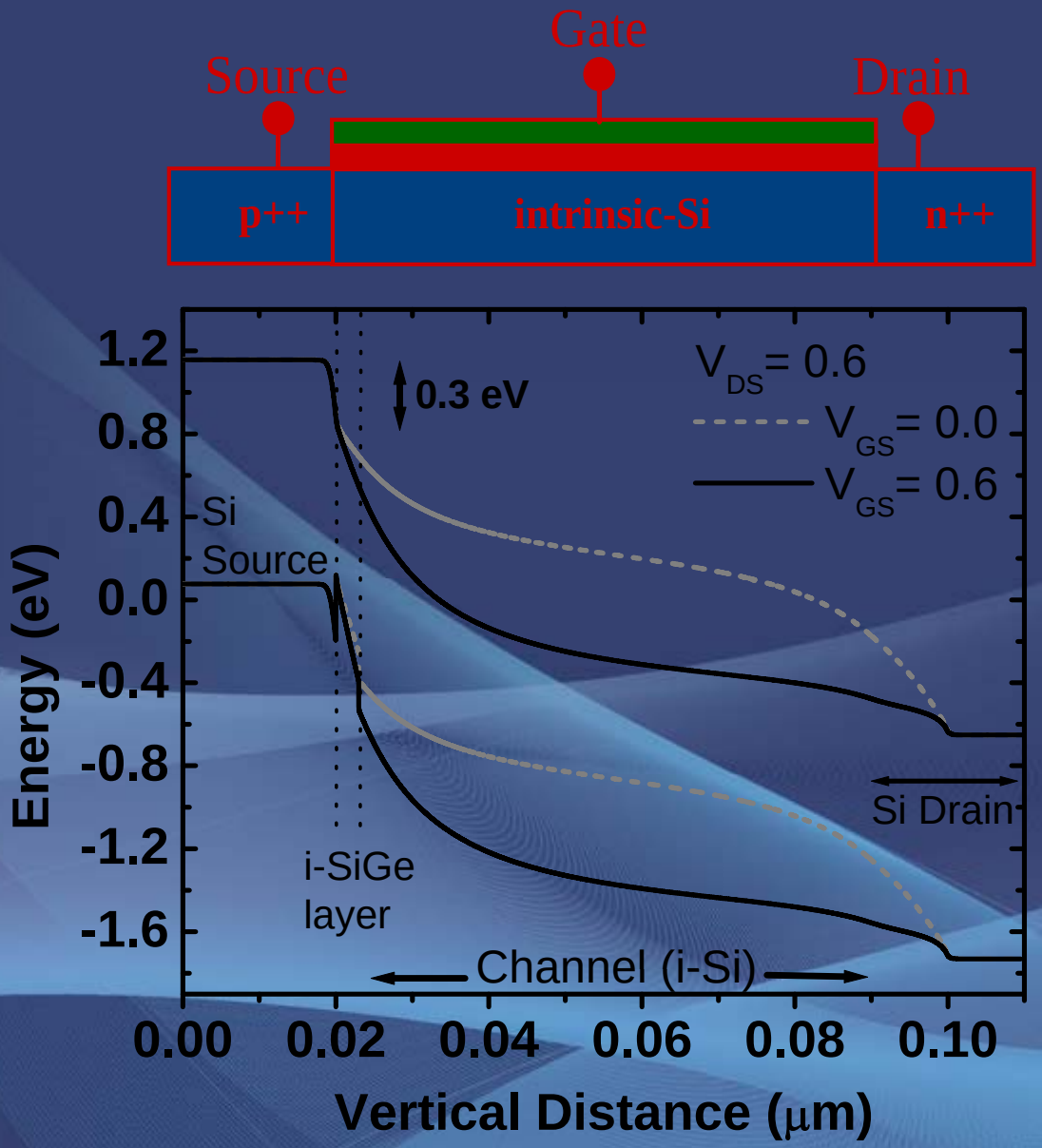
- V_d = positive
- V_g = positive
- barrier thin, current flows



Tunneling Barrier Width



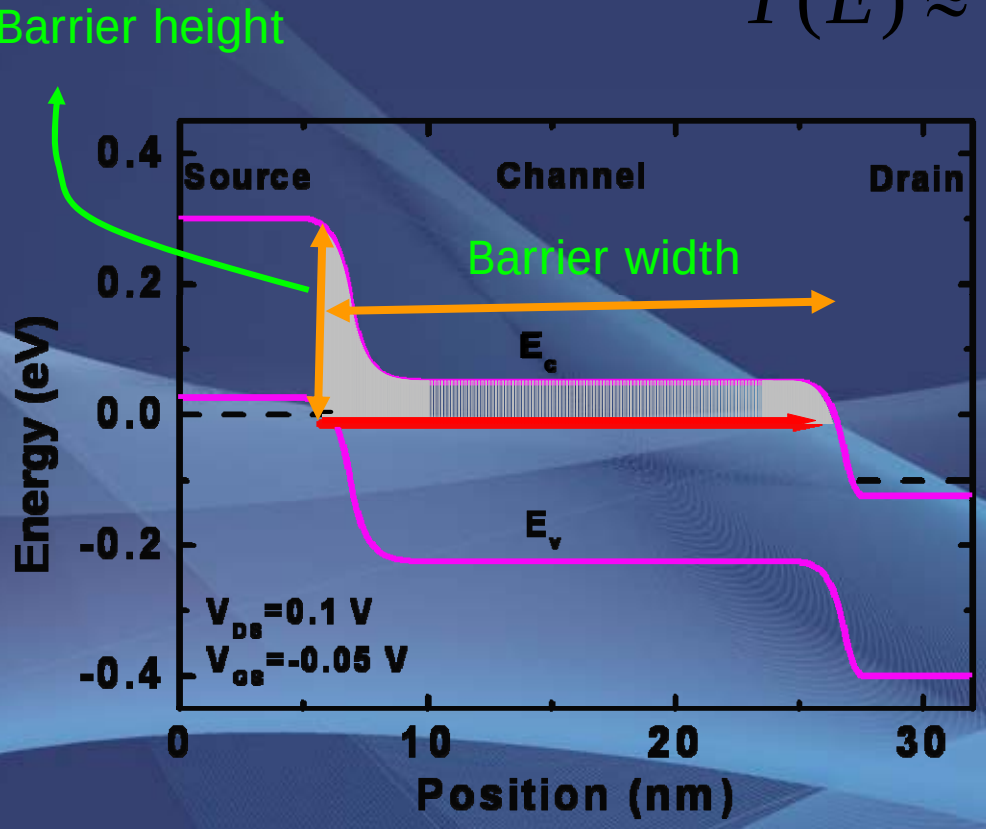
Working Principle



Improving Performance

- T-FET Limitation: Low ON current

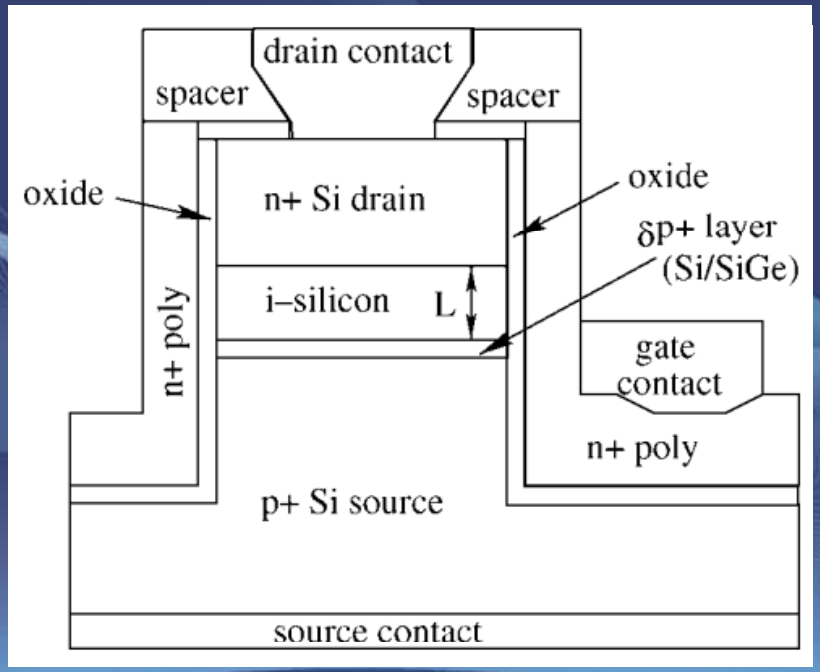
$$T(E) \approx \exp\left(-\frac{4\Lambda\sqrt{2m^*}E_g^{3/2}}{3|e|\hbar(\Delta\phi + E_g)}\right)$$



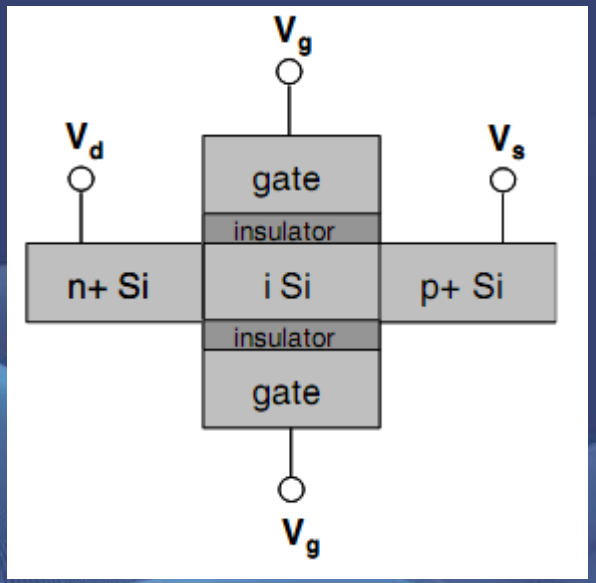
Literature Review

Bhuwalka et. al. 2004

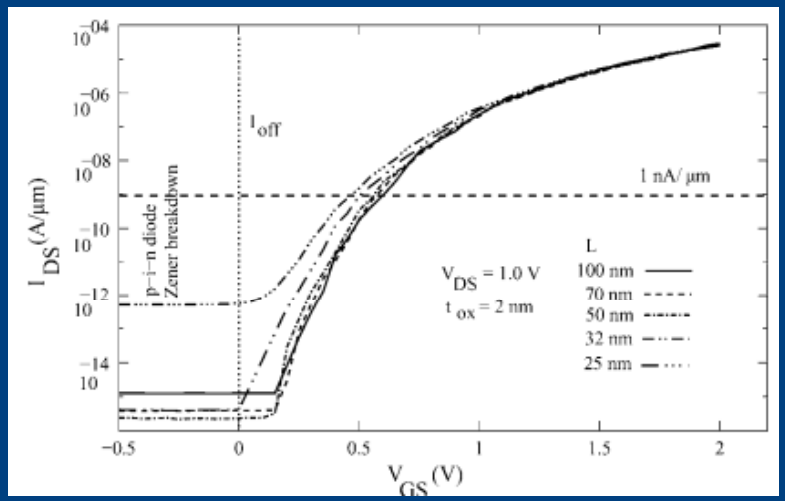
S~50 mV/dec

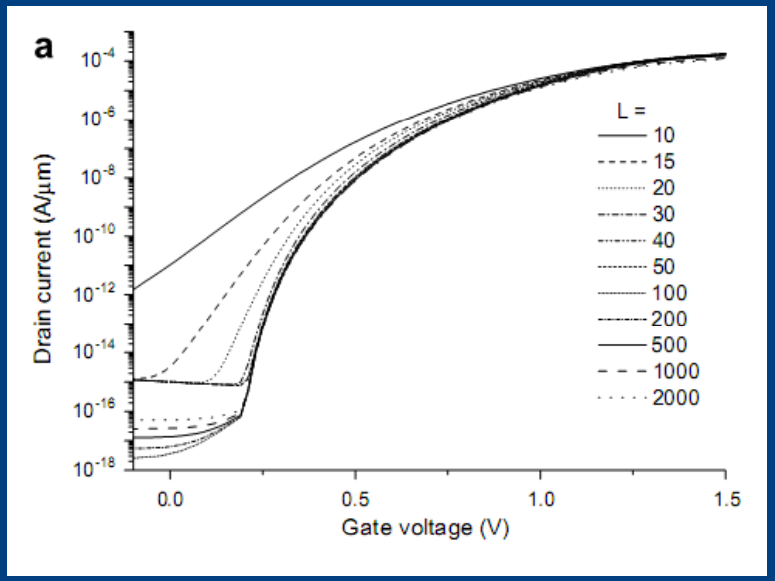


Boucart et. al. 2007



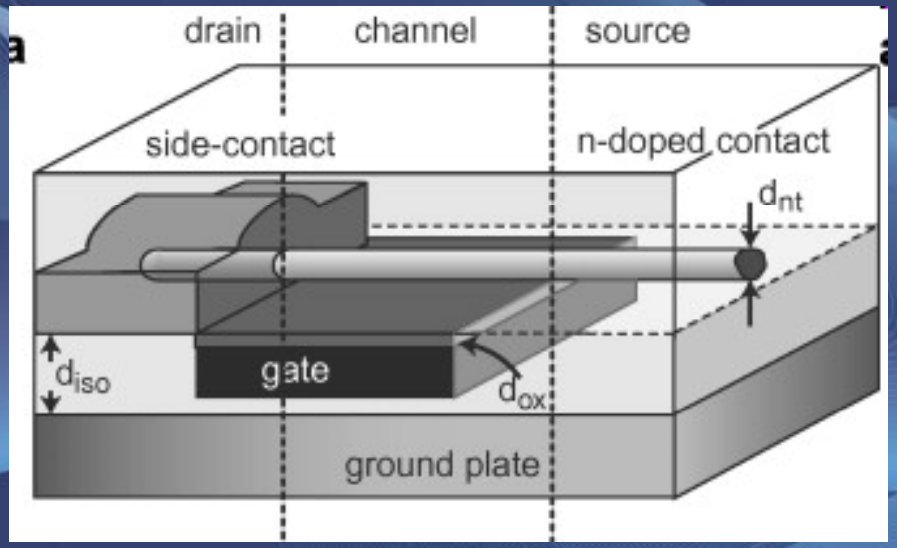
Literature Review

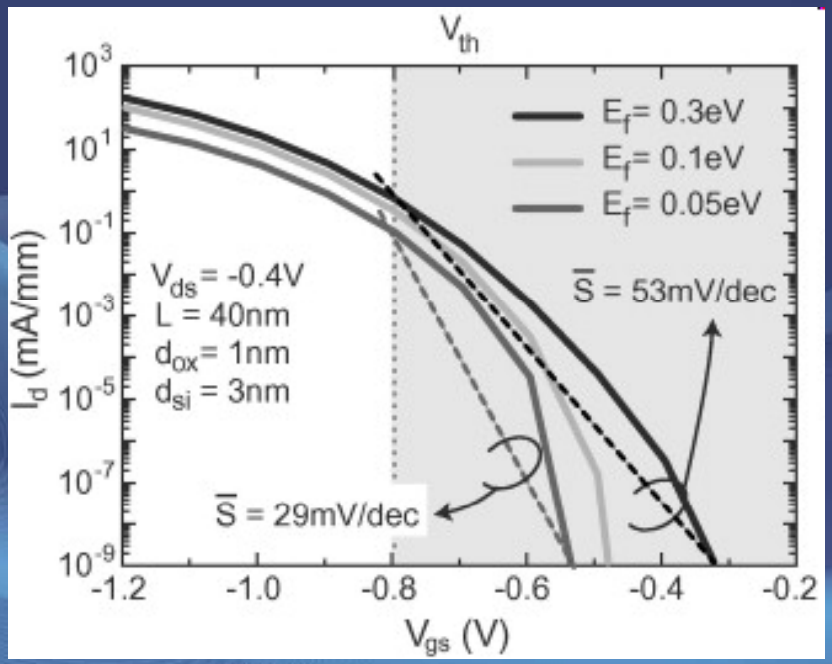




Literature Review

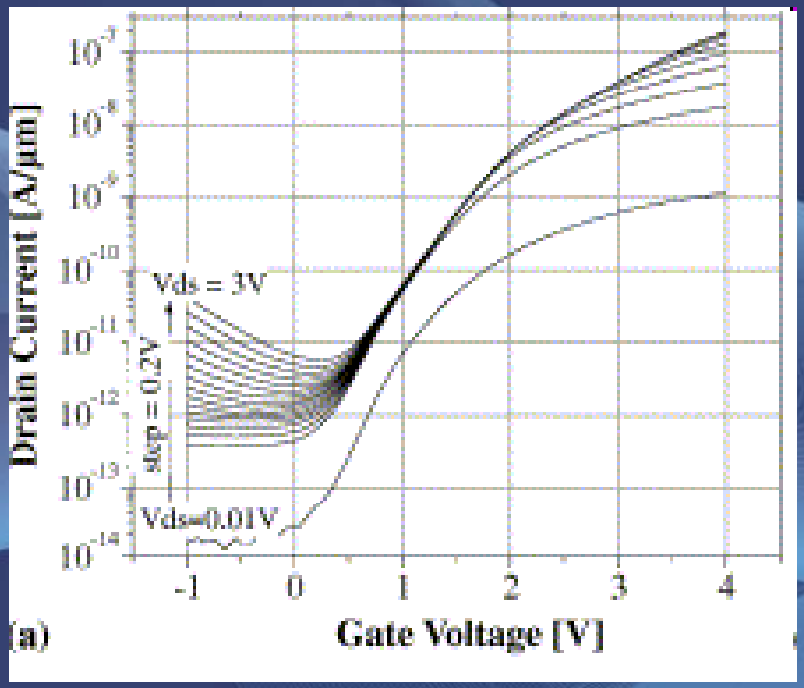
- CNT based T-FET
- Knoch et. al. 2007
- S=13 mV/dec

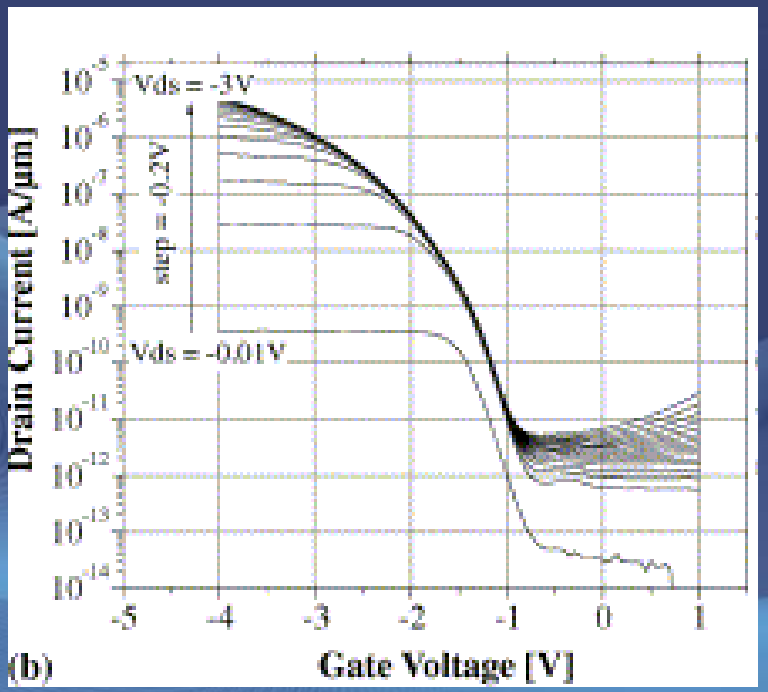




Literature Review

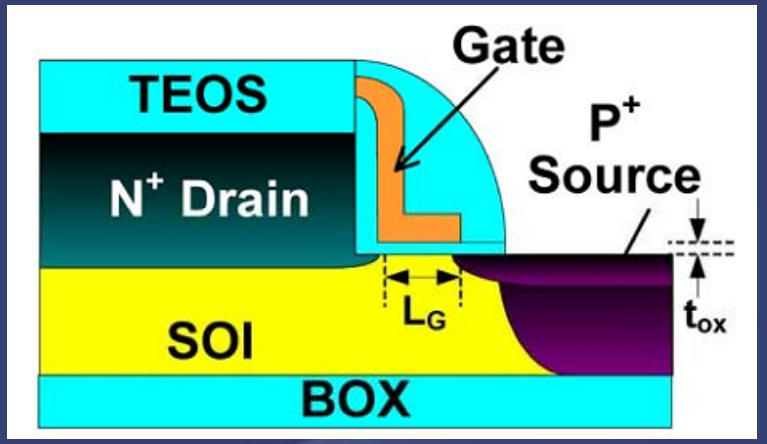
- Complementary T-FET
- Wang et. al. 2004
- High voltage requirement

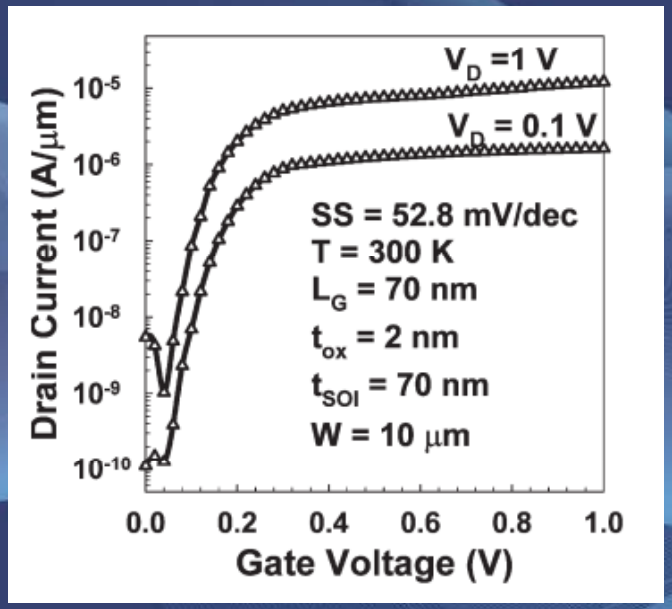


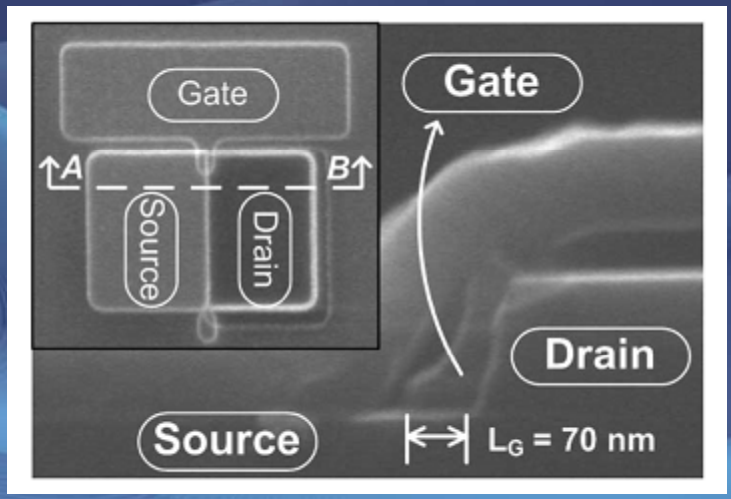


Literature Review

- First experimental work
- Choi et. al. 2007 (UC Berkeley)
- High voltage requirement

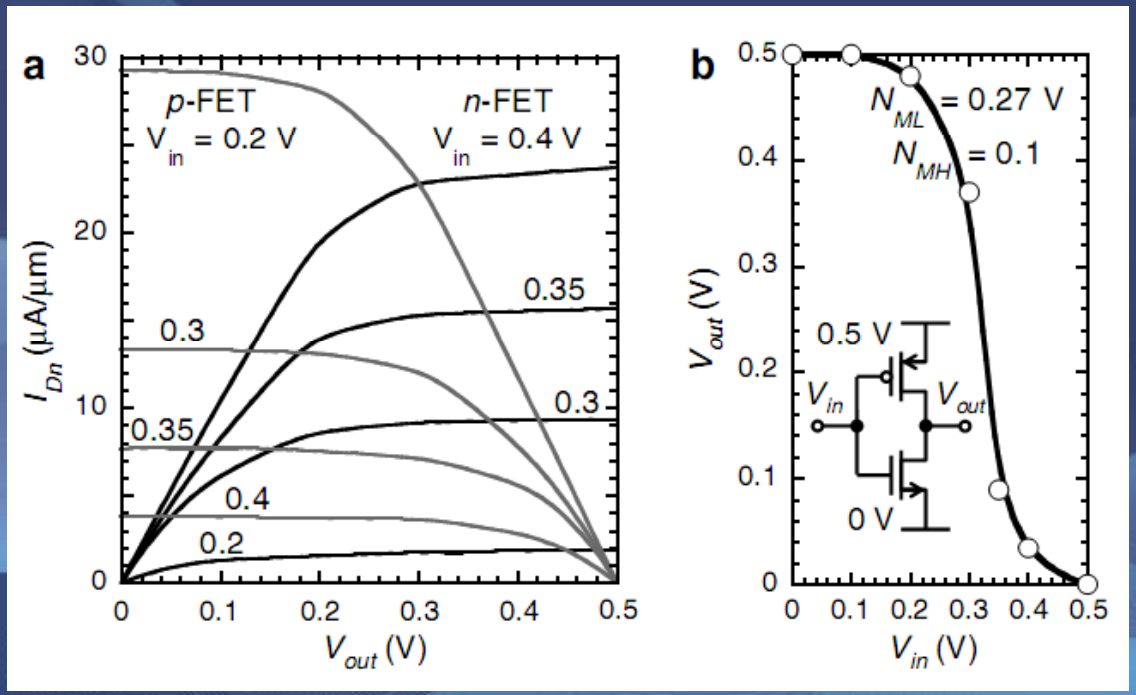






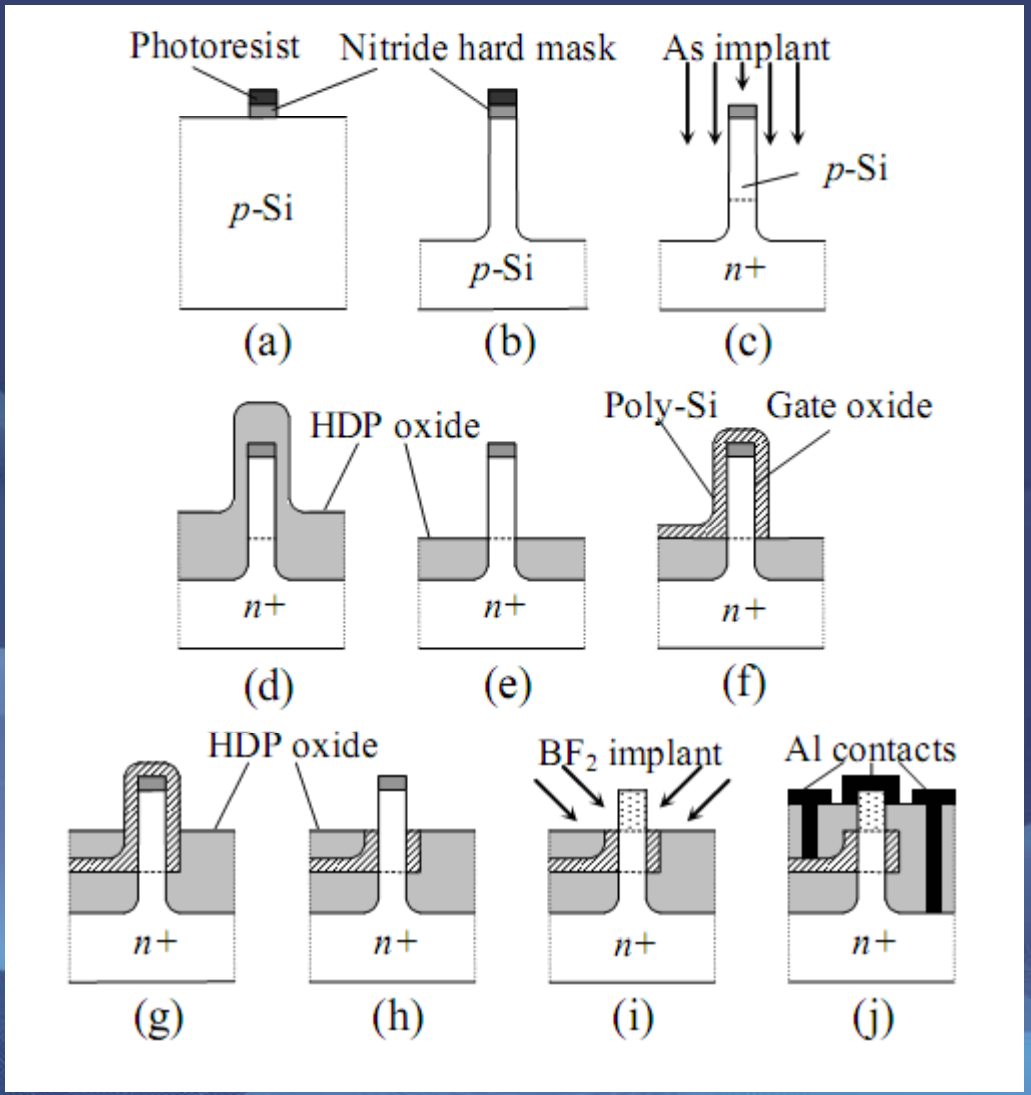
Literature Review

- Ge tunneling transistor
- Zhang et. al. 2008
- Low voltage, 2nm body thickness
- Claims to be faster than CMOS at VDS=0.5 V



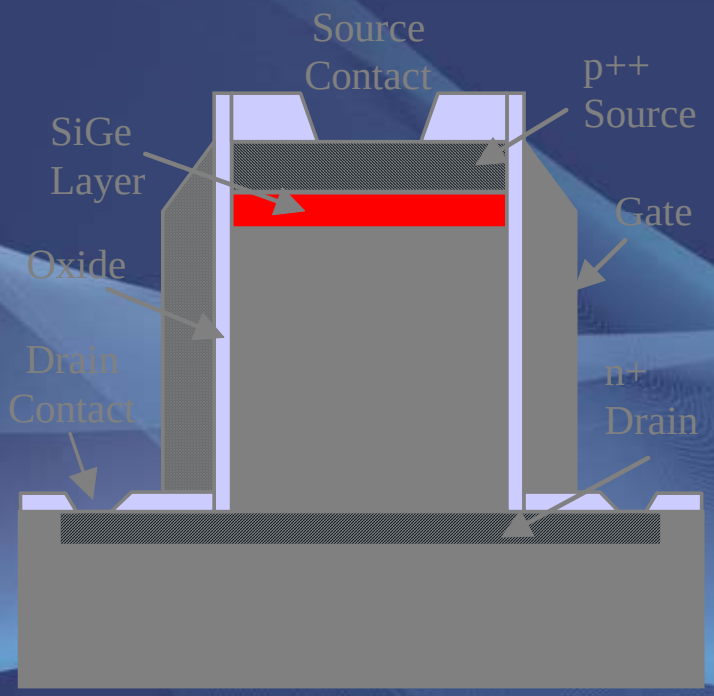
Fabrication

Chen et. al. 2009
IME-Singapore

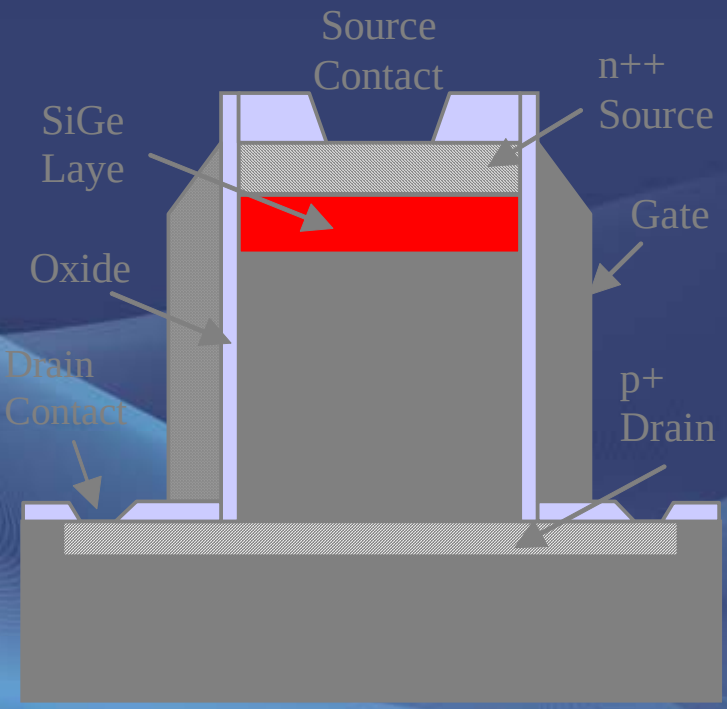


i-SiGe based T-FET

n-T-FET

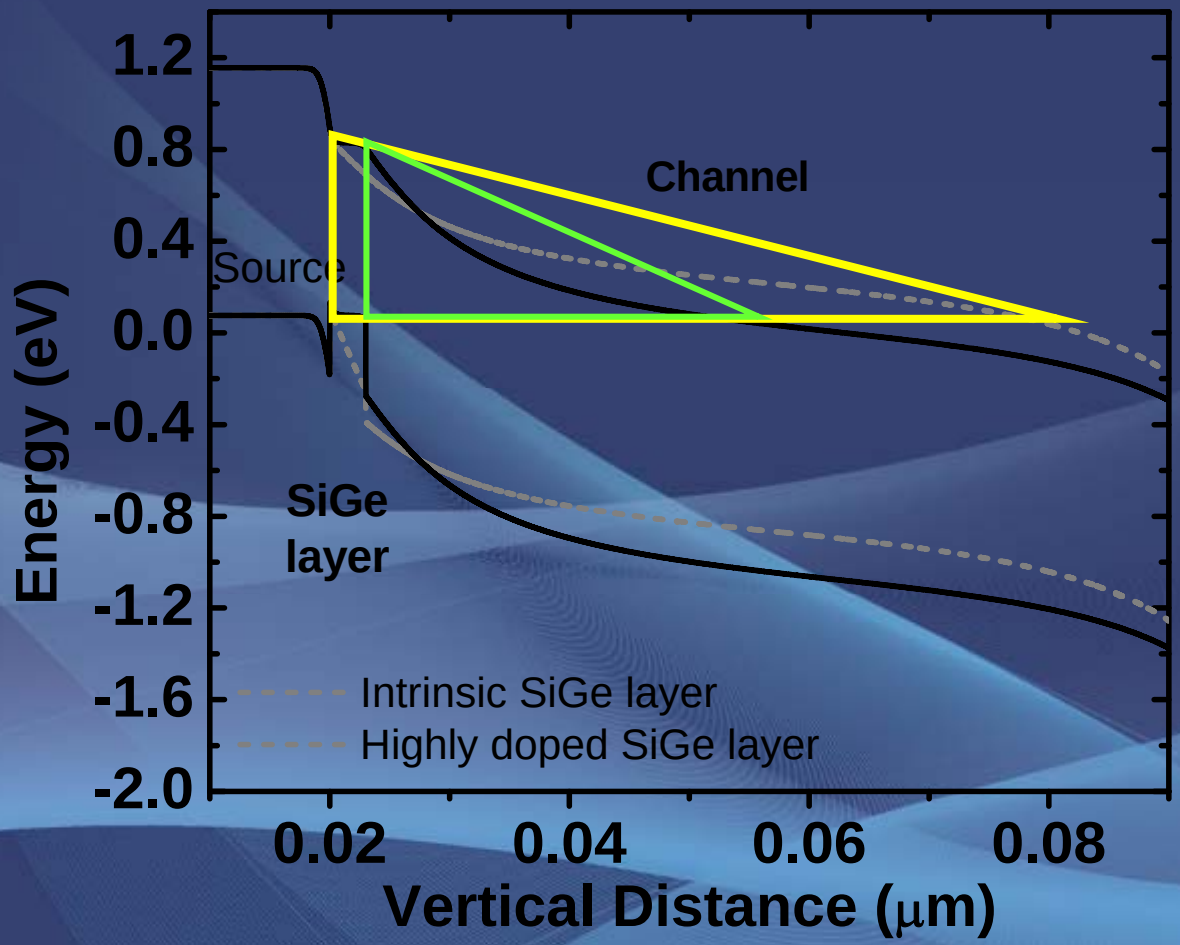


p-T-FET

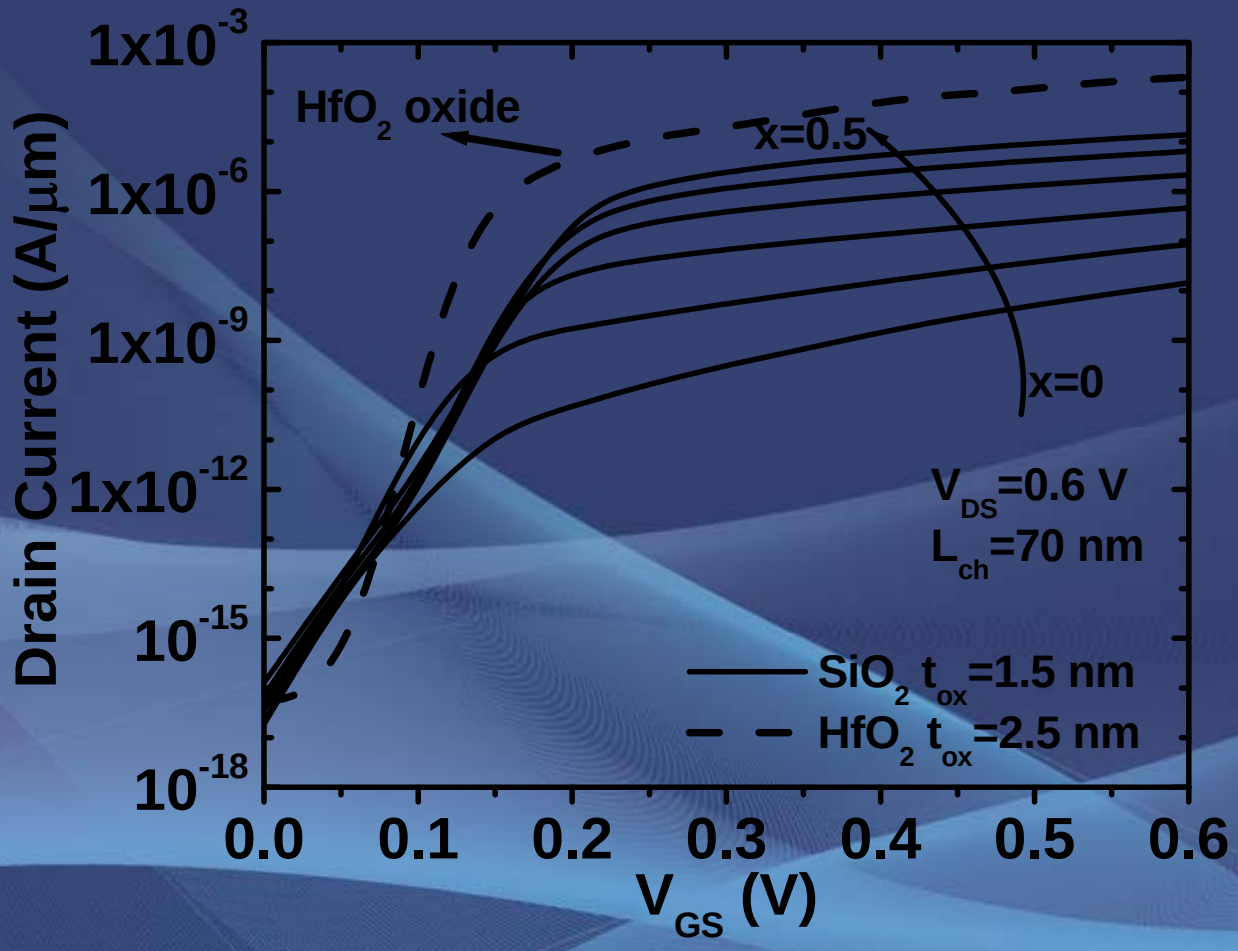


Khatami and Banerjee, (UCSB) 2009

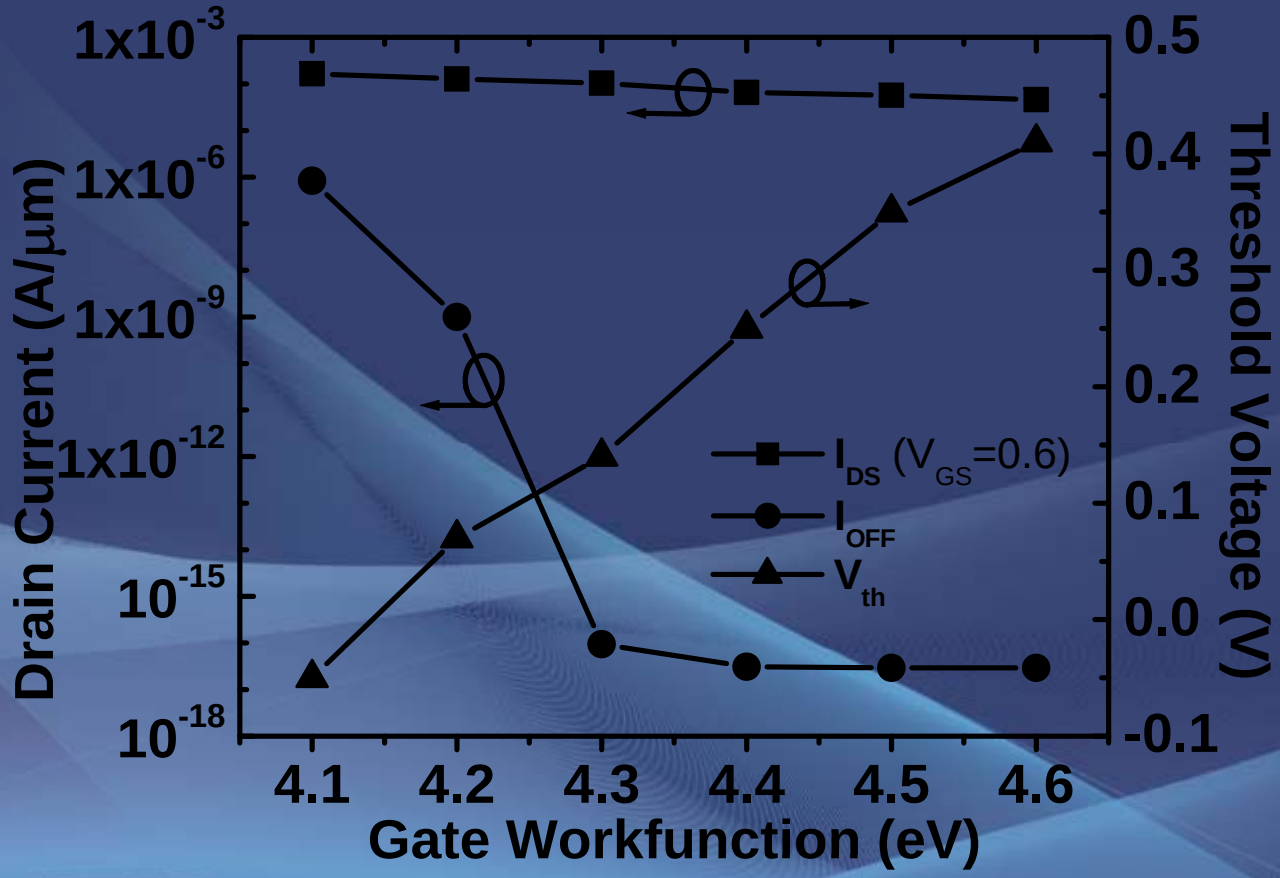
Comparison of i-SiGe and Heavily Doped SiGe Devices



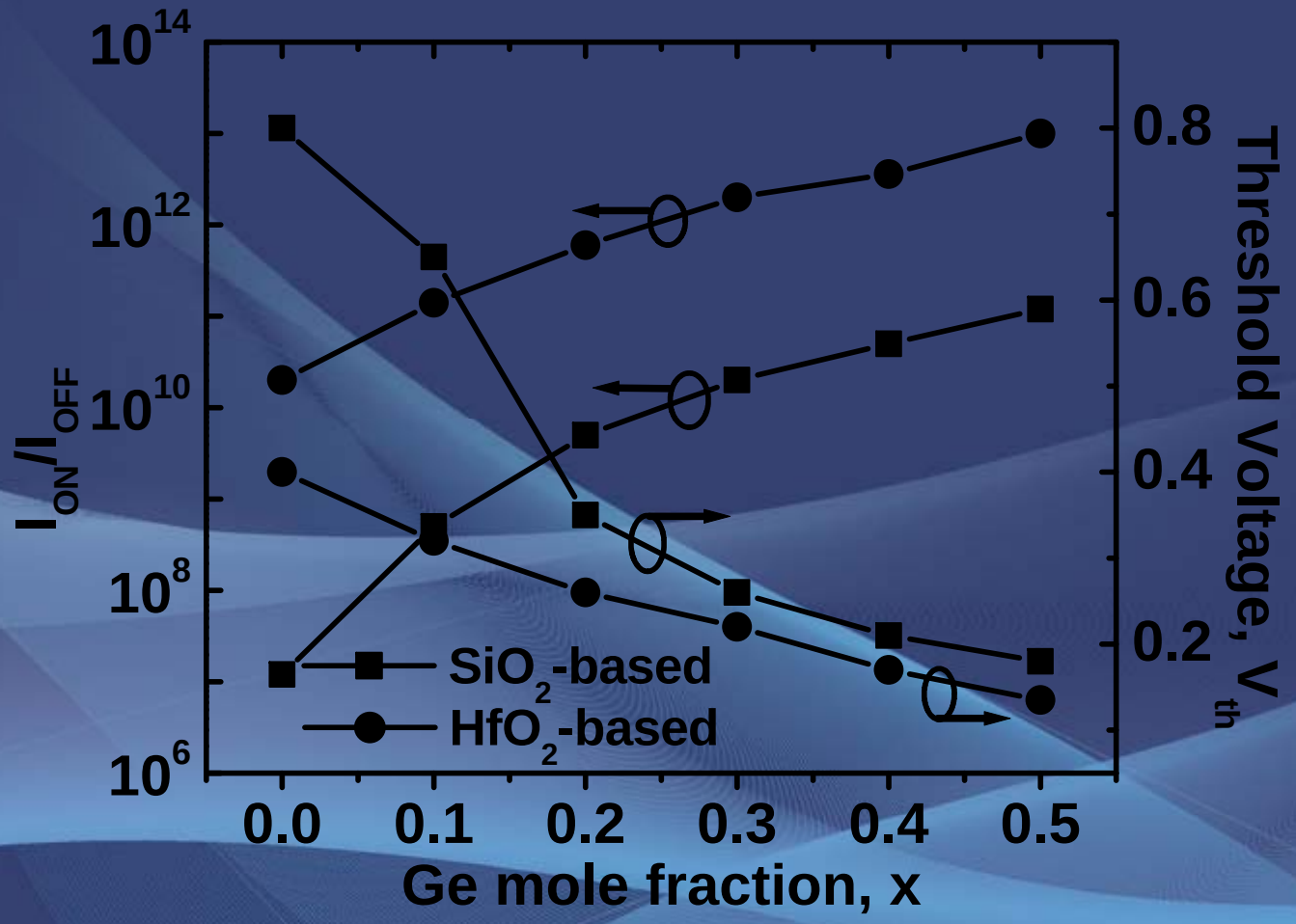
Input Characteristics



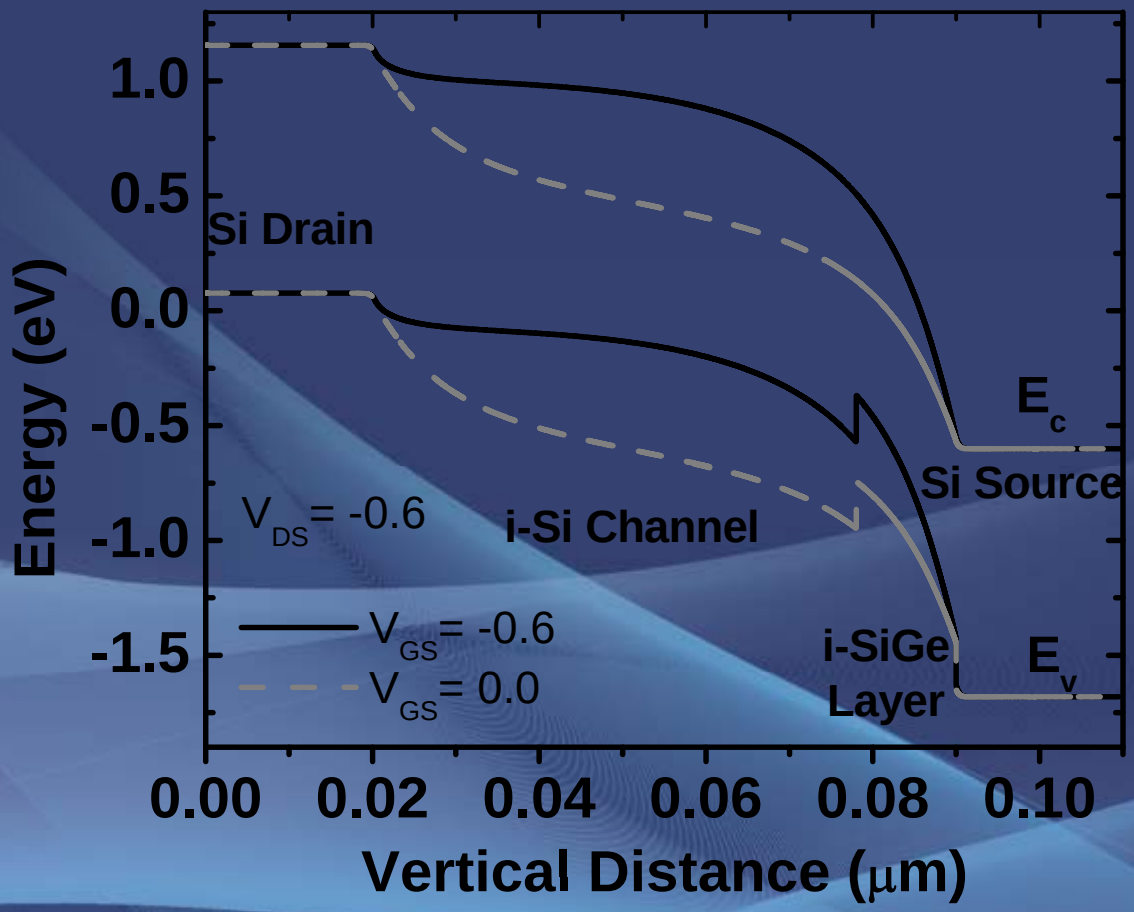
Performance Optimization



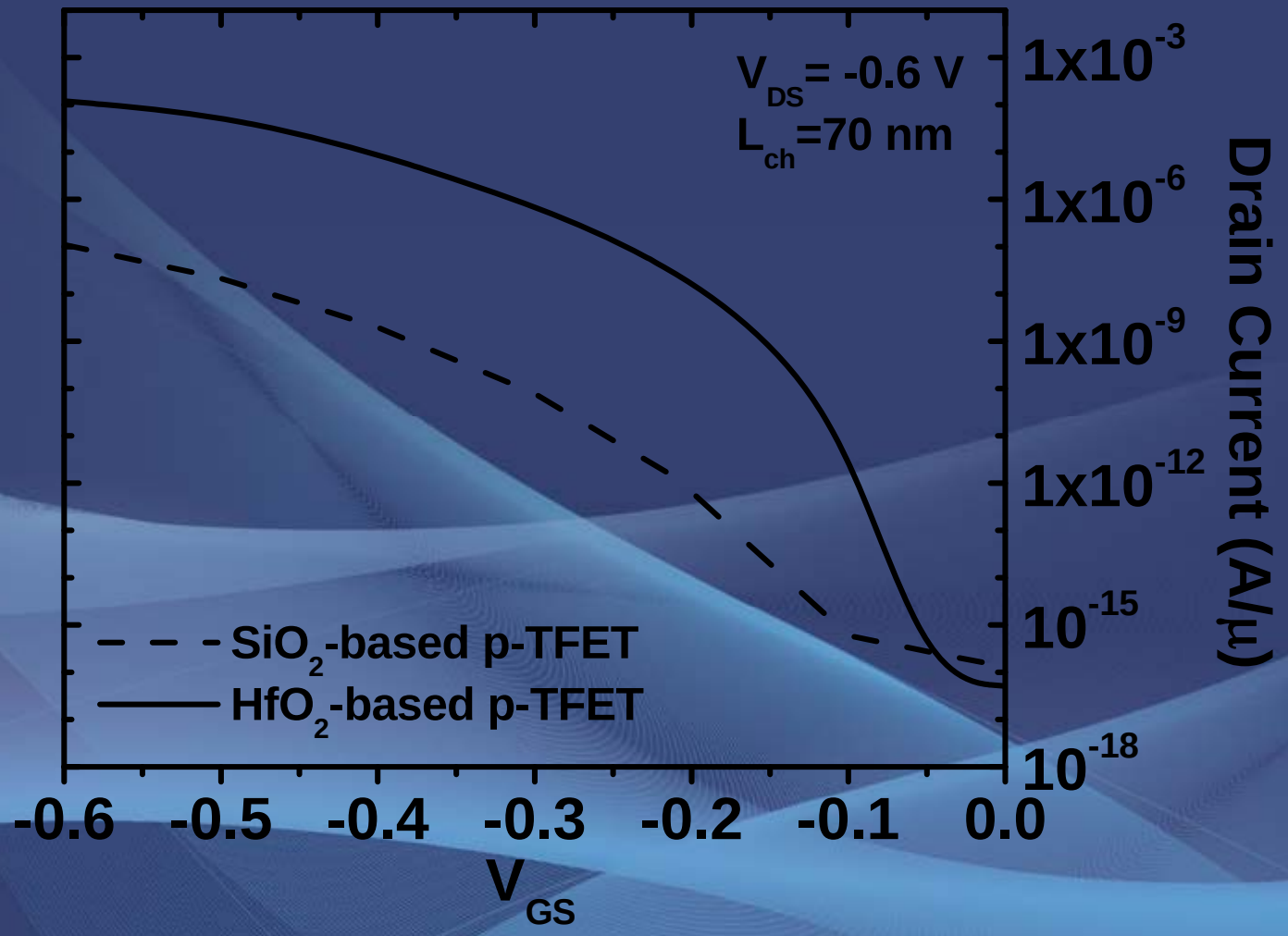
Performance Optimization



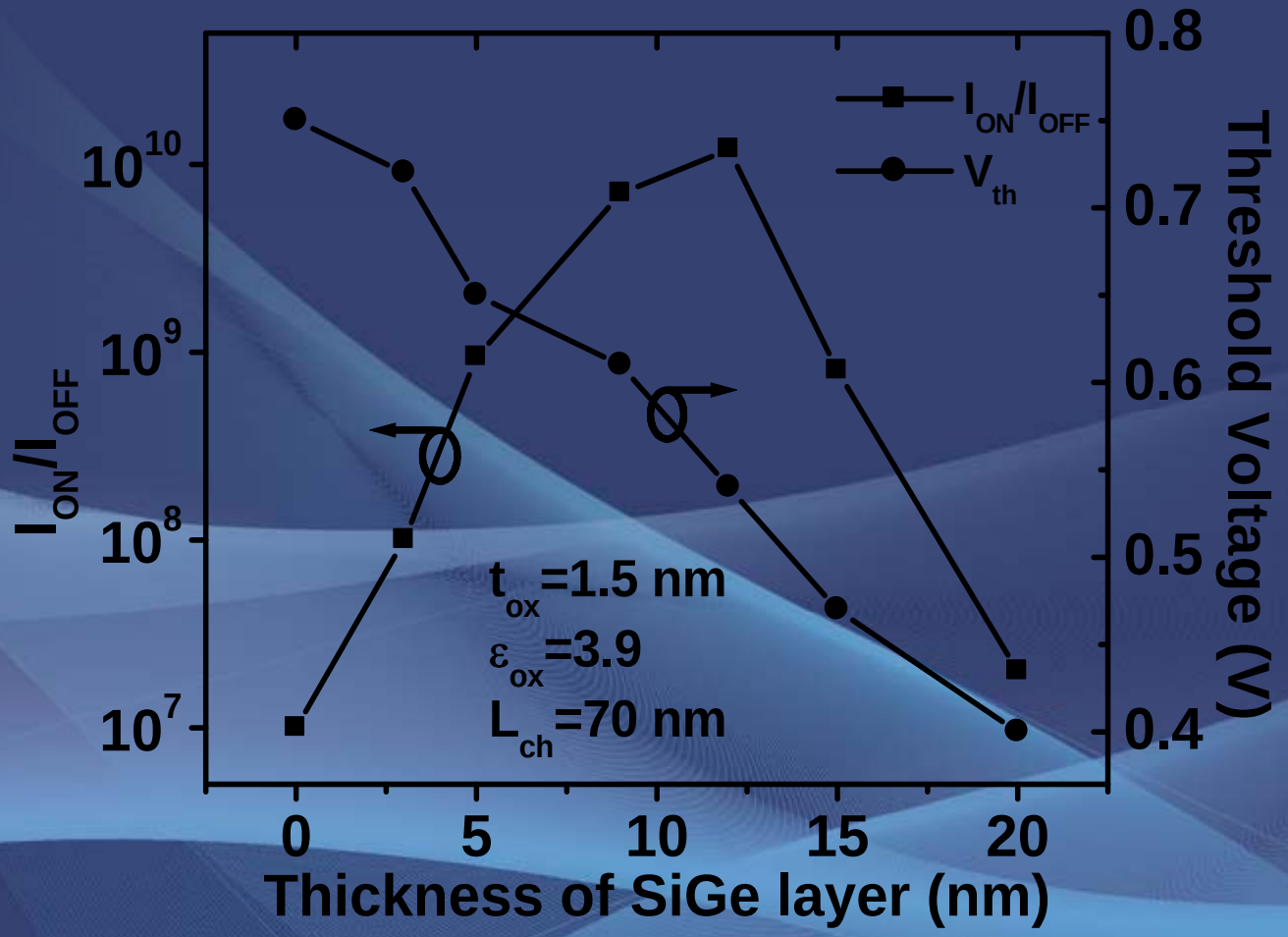
p-T-FET


1.0
0.5
0.0
-0.5
-1.0
-1.5
Energy (eV)
0.00
0.02
0.04
0.06
0.08
0.10
Vertical Distance (μm)
Si Drain
Si Source
i-Si Channel
i-SiGe Layer
E_c
E_v
V_DS = -0.6
V_GS = -0.6
V_GS = 0.0

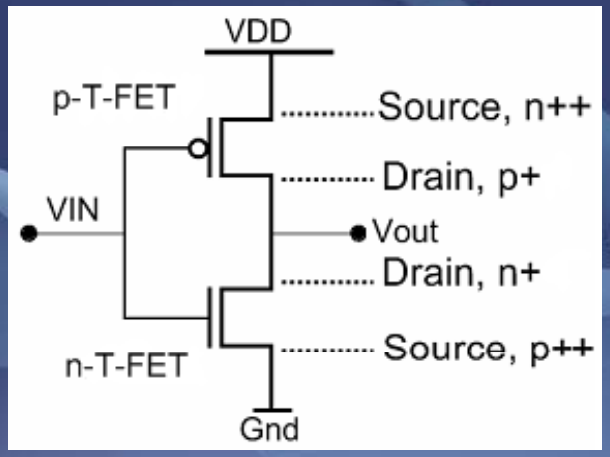
Input Characteristics p-T-FET

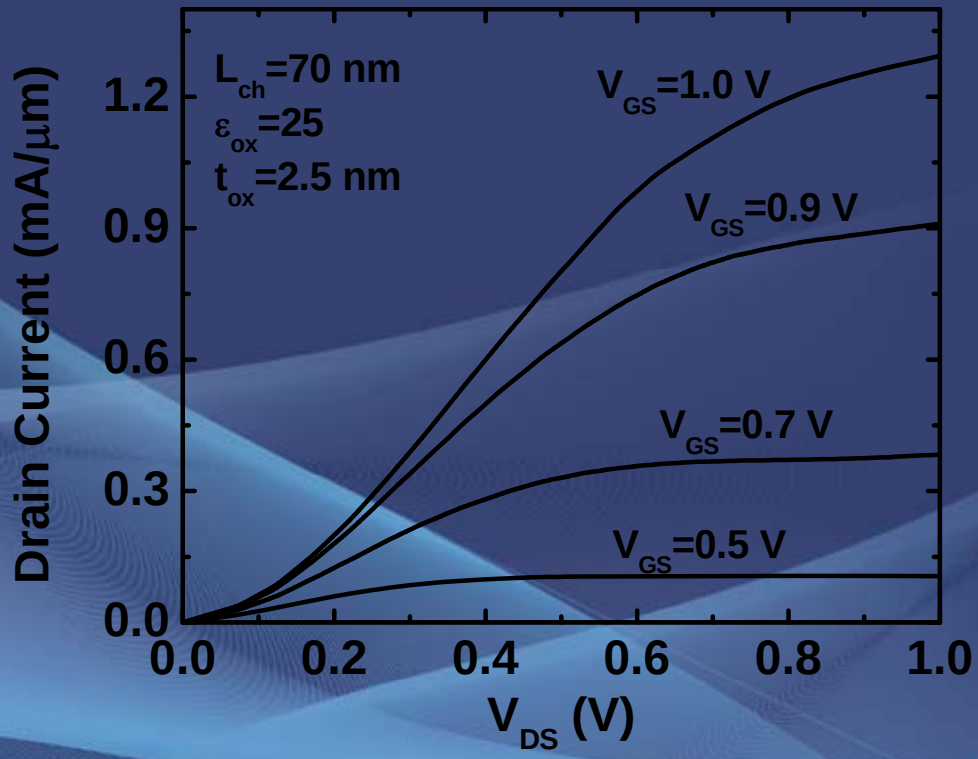


Performance Optimization

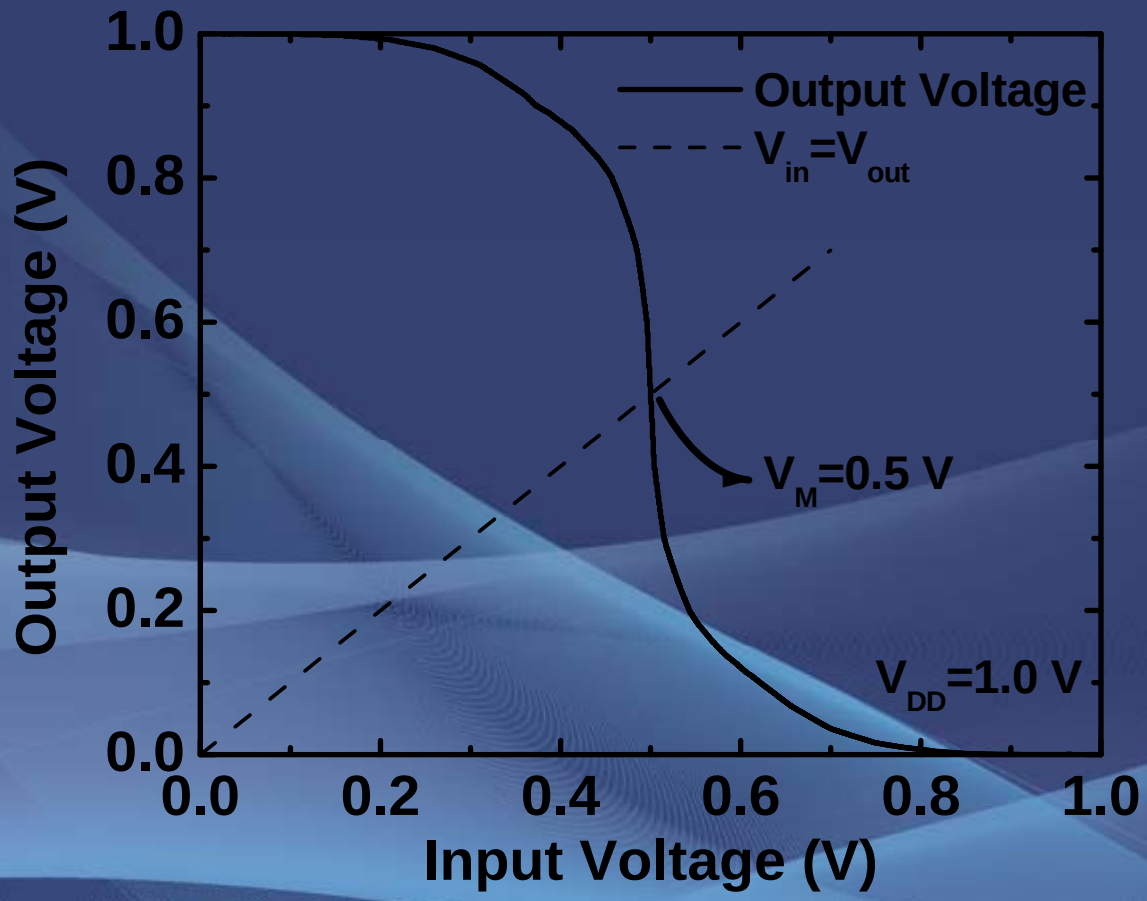


Circuit Analysis

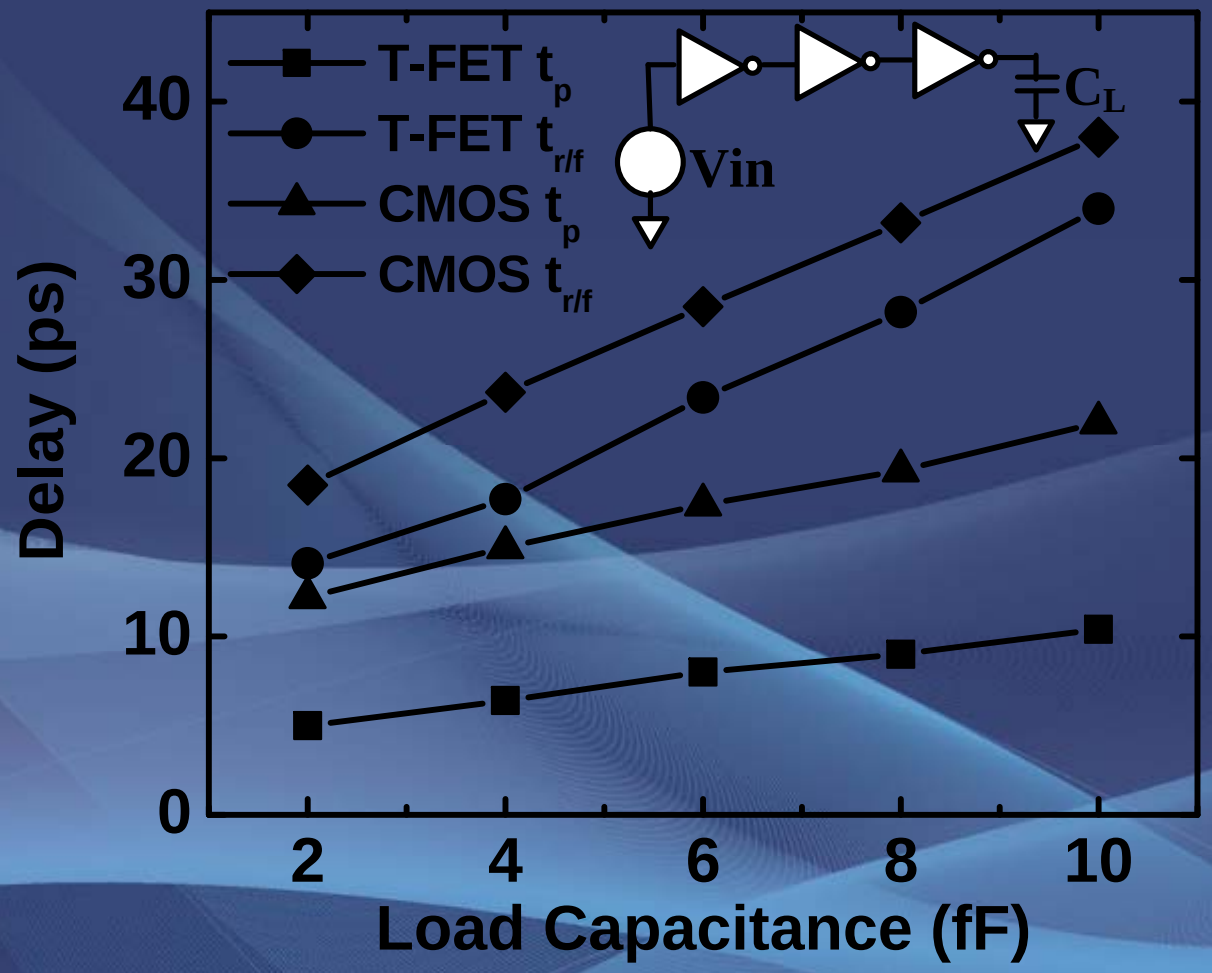




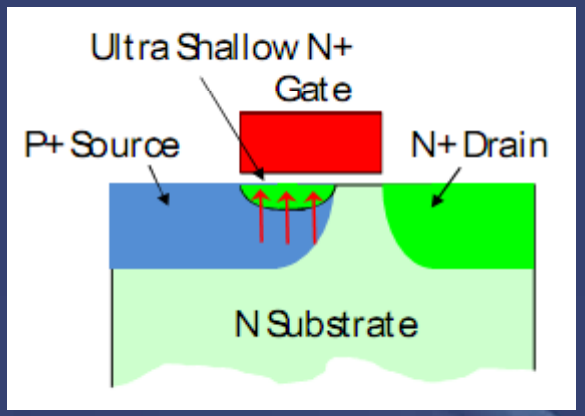
Inverter VTC

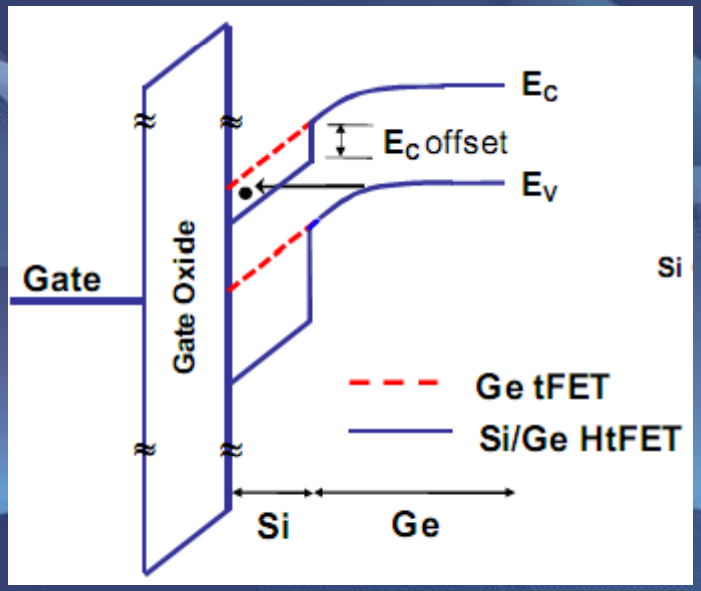


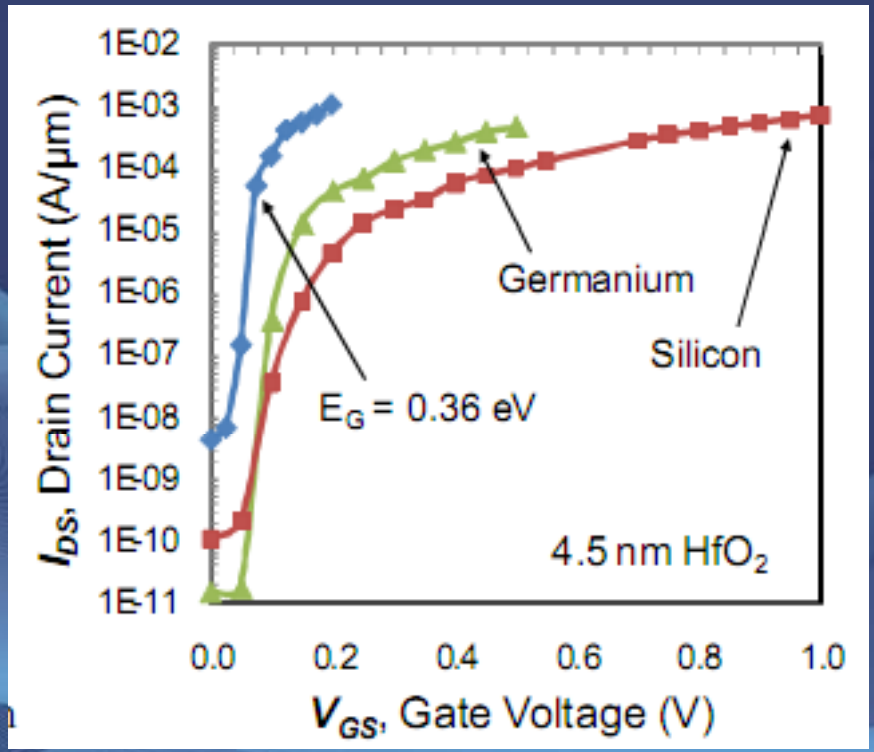
Circuit Analysis



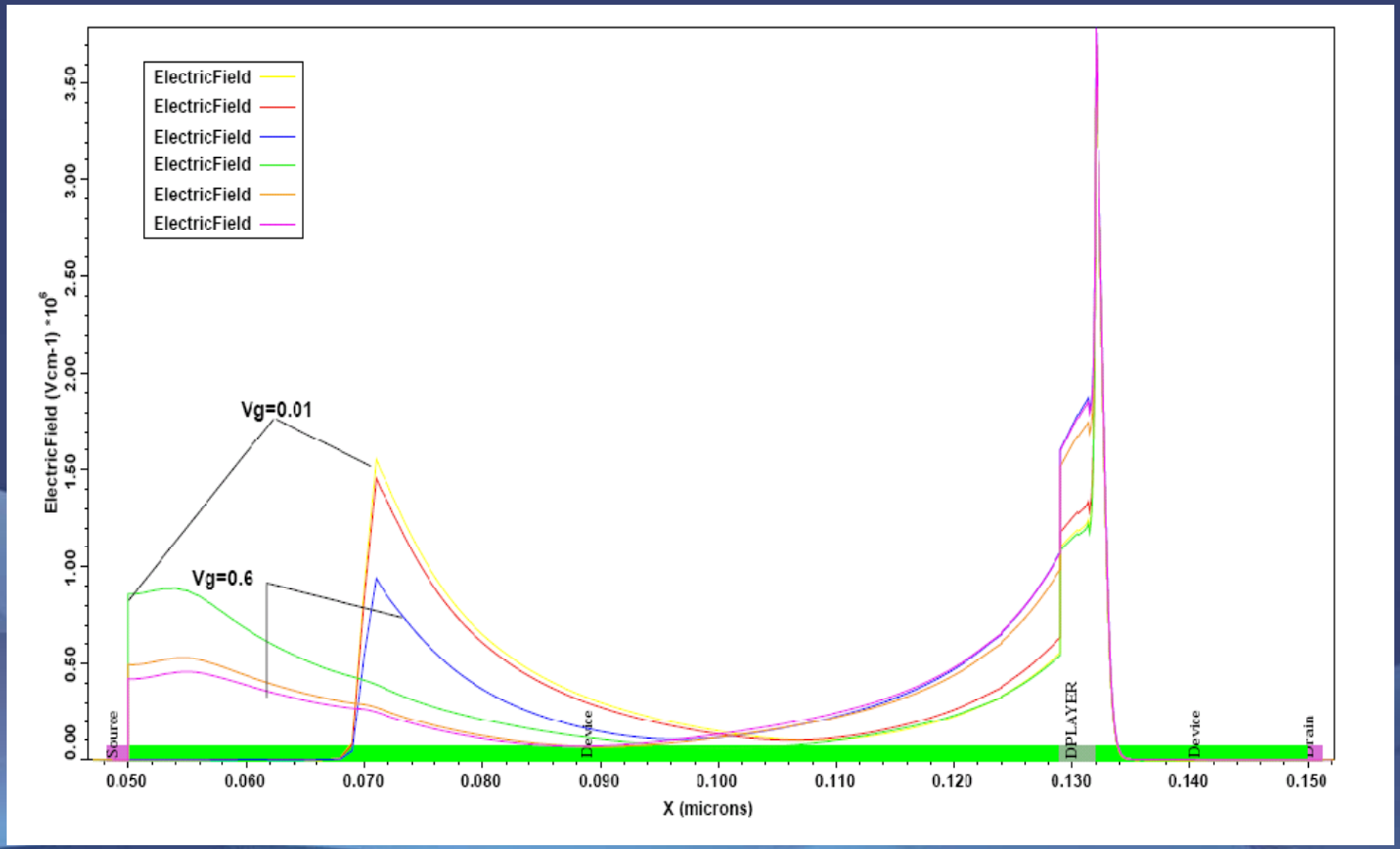
Green FET (Berkeley)





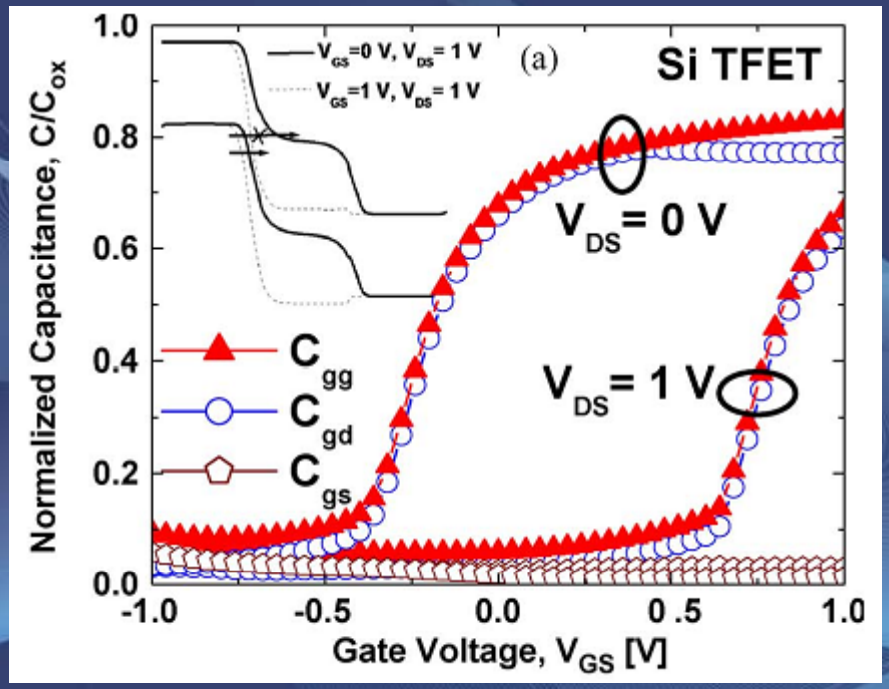


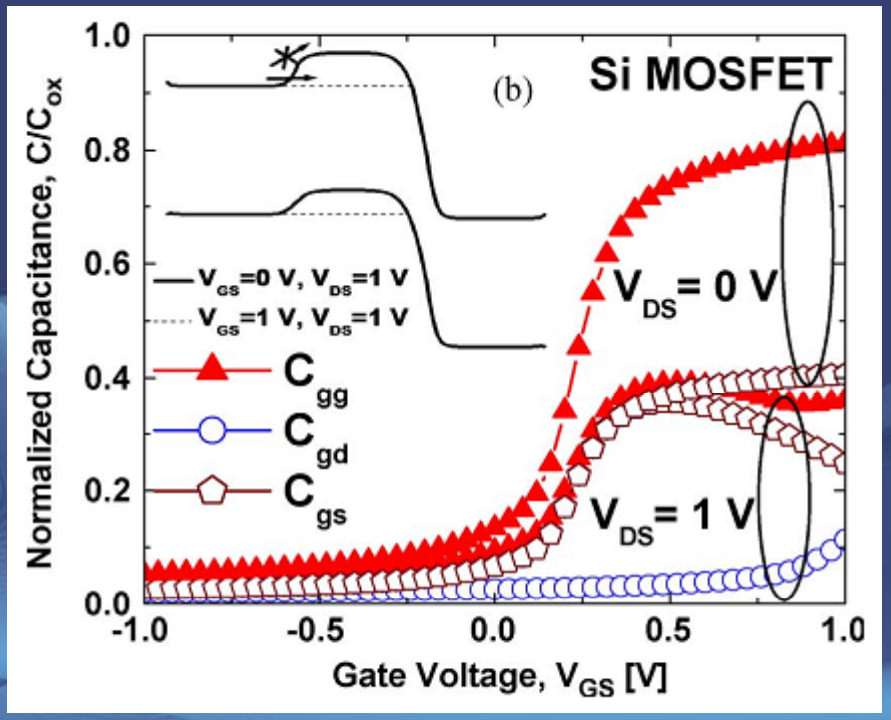
I_{OFF} Reduction



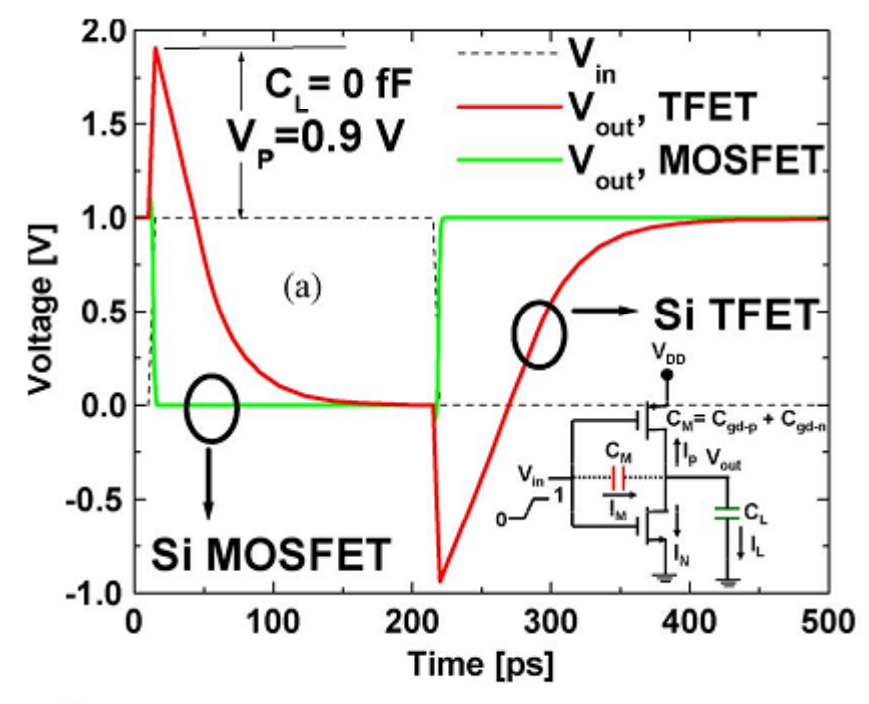
Parasitics in T-FET

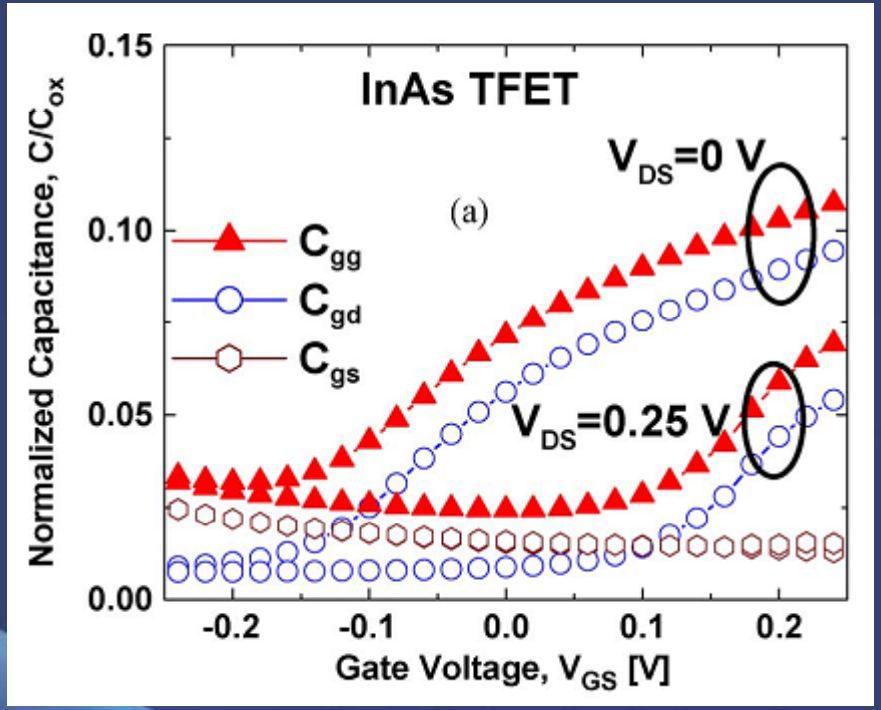
- Mookerja et. al. 2009
- Cgd dominant in T-FET





Parasitics in T-FET





MILLER CAPACITANCE $C_M = C_{gd,n} + C_{gd,p}$ FOR Si TFET/MOSFET INVERTER FOR VARIOUS POINTS ALONG THE DC TRANSFER CHARACTERISTICS, AS SHOWN IN FIG. 3(b). HERE, $C_{gg} = 0.8\ C_{ox}$

	A	B	C	D	E
MOSFET	$0.5C_{gg} + 0.03C_{gg}$ (p-lin, n-cutoff)	$0.5C_{gg} + 0.04C_{gg}$ (p-lin, n-sat)	$0.2C_{gg}$ (p-sat, n-sat)	$0.5C_{gg} + 0.04C_{gg}$ (p-sat, n-lin)	$0.5C_{gg} + 0.03C_{gg}$ (p-cutoff, n-lin)
TFET	$C_{gg} + 0.05C_{gg}$ (p-lin, n-cutoff)	$C_{gg} + 0.08C_{gg}$ (p-lin, n-sat)	$1.1C_{gg}$ (p-sat, n-sat)	$C_{gg} + 0.08C_{gg}$ (p-sat, n-lin)	$C_{gg} + 0.05C_{gg}$ (p-cutoff, n-lin)