ECE 225
High-Speed Digital IC Design
Lecture 13

Steep Subthreshold Slope Devices:
Nanoelectromechanical (NEM) FETs

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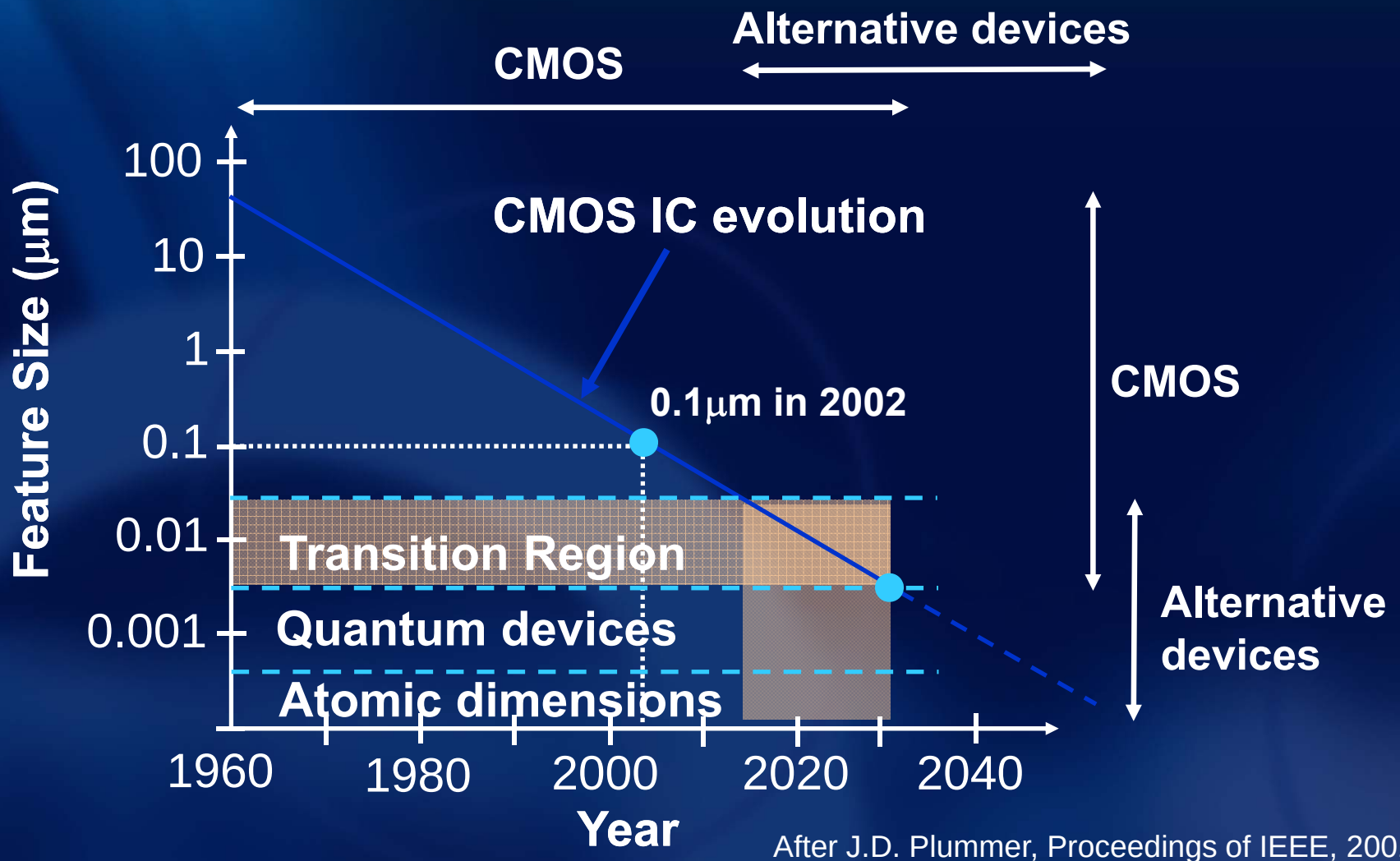
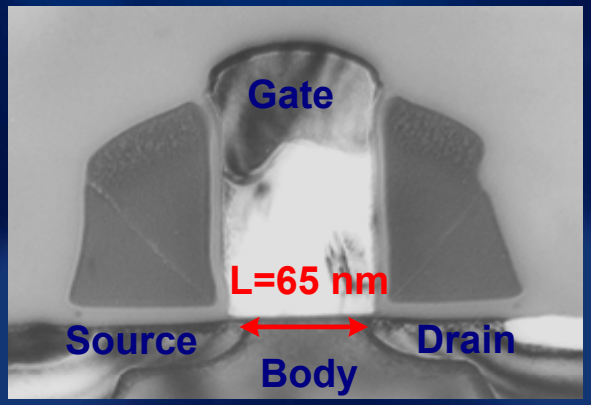
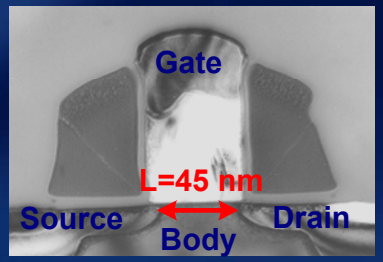
CMOS Scaling: History and future…



After J.D. Plummer, Proceedings of IEEE, 2001.

Scaling: Size Does Matter!

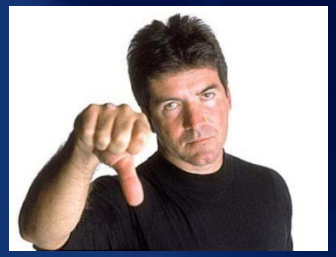




Source: Intel Inc.

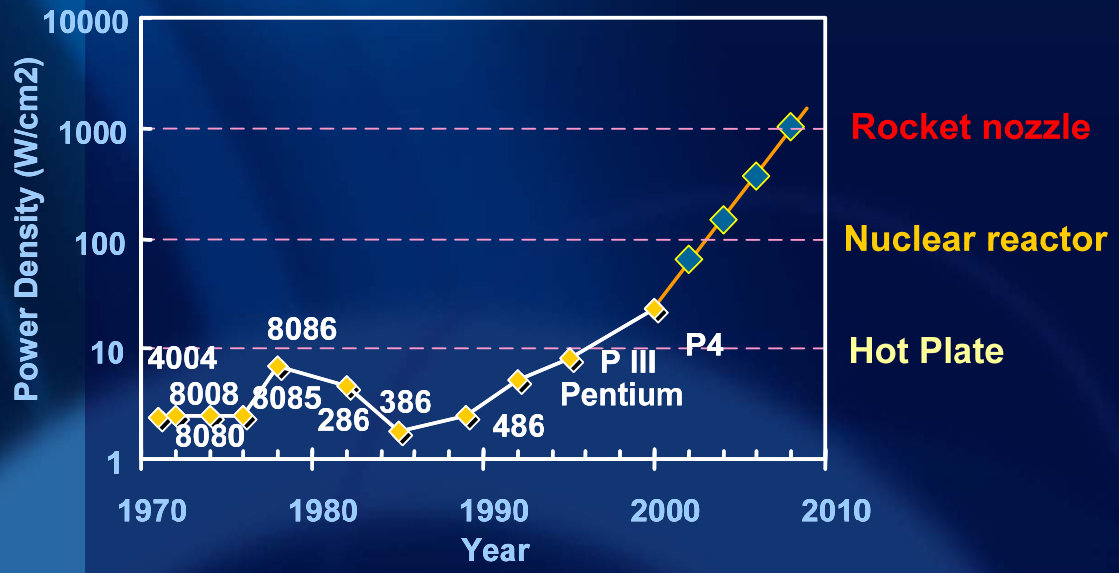
Scaling down

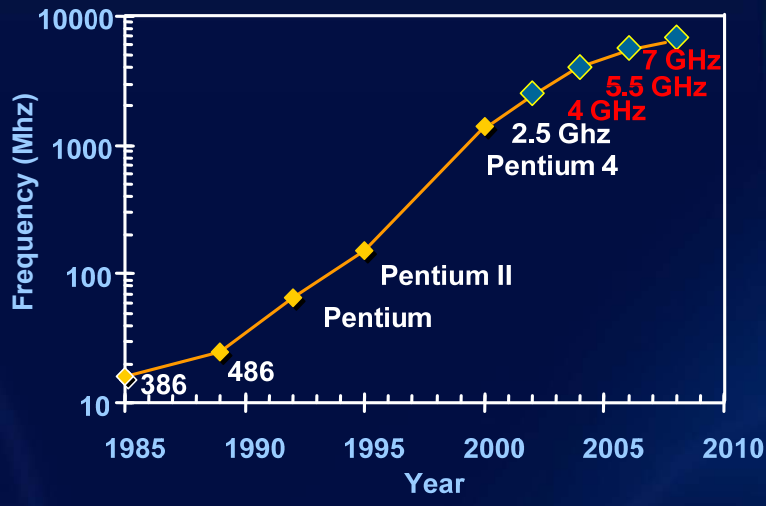
- Faster operation
- More functionality



- Higher leakage
- Reliability issues
- Variability issues
- Power/thermal issues

Scaling: Highway to Hell?

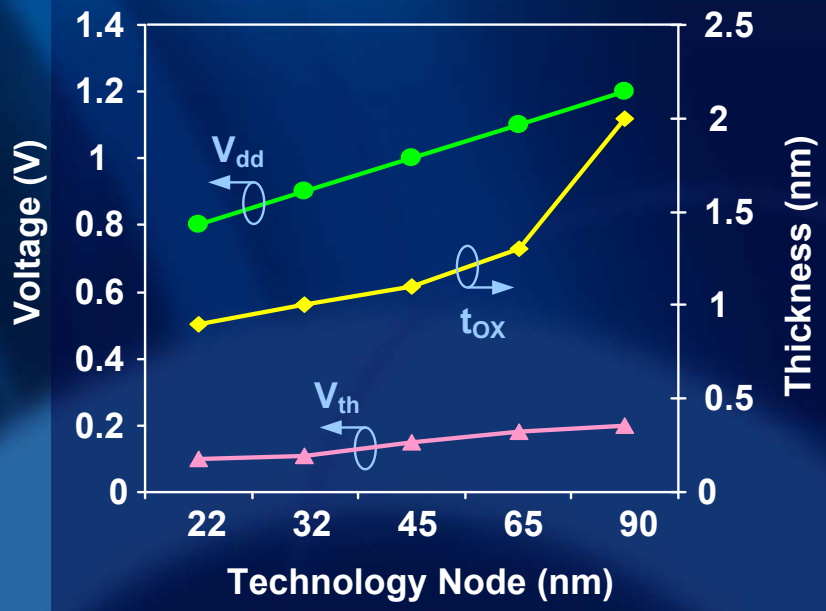




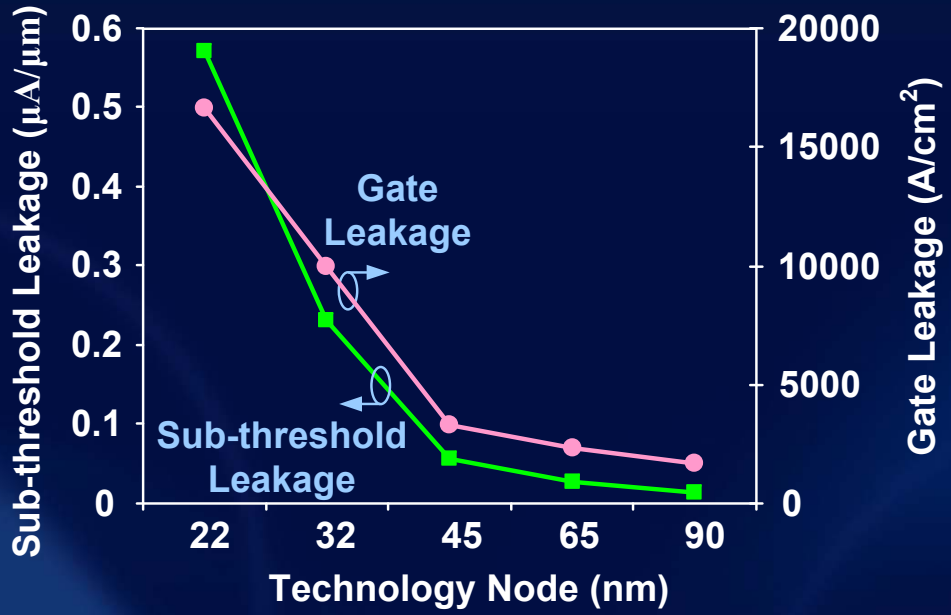
Source: Intel

- Power density increases rapidly due to scaling
- Increasing power consumption limits the faster operation offered by scaling

CMOS Scaling Trends



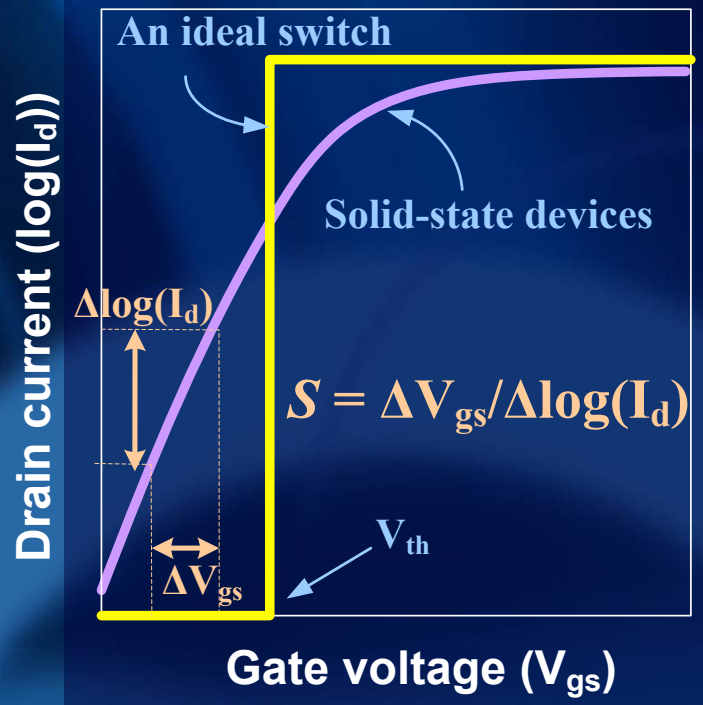
Source: *ITRS 2005*



Source: *ITRS 2005*

- **Subthreshold and gate leakage increase dramatically with scaling device parameters**

Theoretical Limit for Sub-threshold Swing of CMOS Devices



Analytical equation for sub-threshold swing (S) of CMOS devices

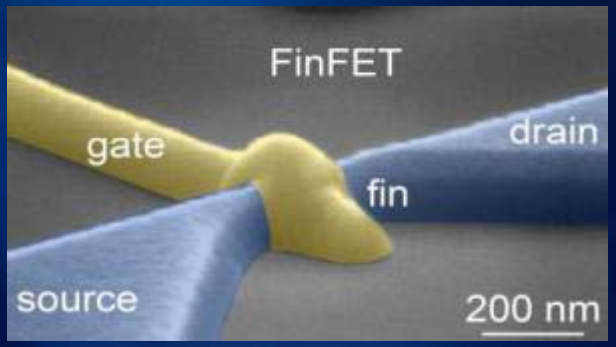
$$I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} (m-1)\left(\frac{kT}{q}\right)^2 e^{q(V_g - V_t)/mkT}\left(1 - e^{-qV_{ds}/kT}\right)$$

$$S = \left(\frac{d(\log_{10} I_{ds})}{dV_g}\right)^{-1} = 2.3\frac{mkT}{q} = 2.3\frac{kT}{q}\left(1 + \frac{C_{dm}}{C_{ox}}\right)$$

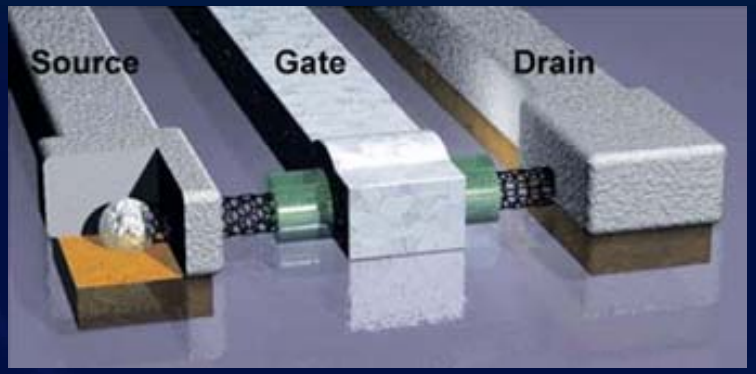
If $C_{dm} \approx 0$, then $S_{Min} = 2.3 \times 26 \approx 60$ mV/decade

- Theoretical limit for sub-threshold swing of all CMOS devices is known to be 60 mV/decade

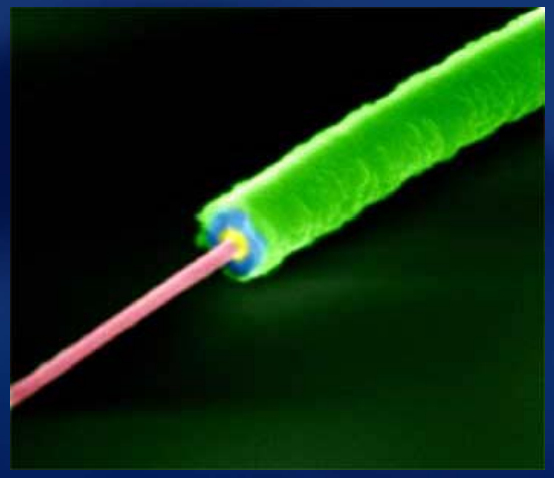
Emerging Technologies



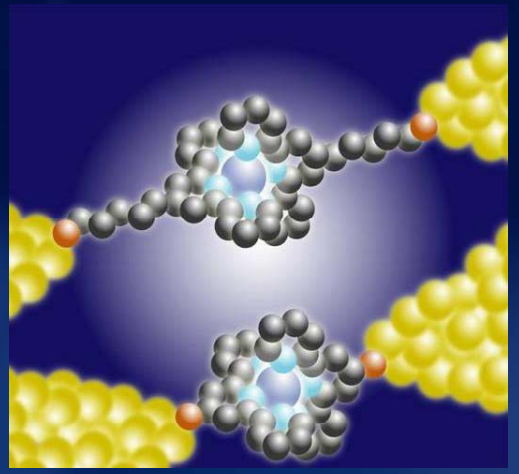
FinFET device
(Courtesy: TU Delft)



Carbon Nano-Tube based device
(Courtesy: Infineon)

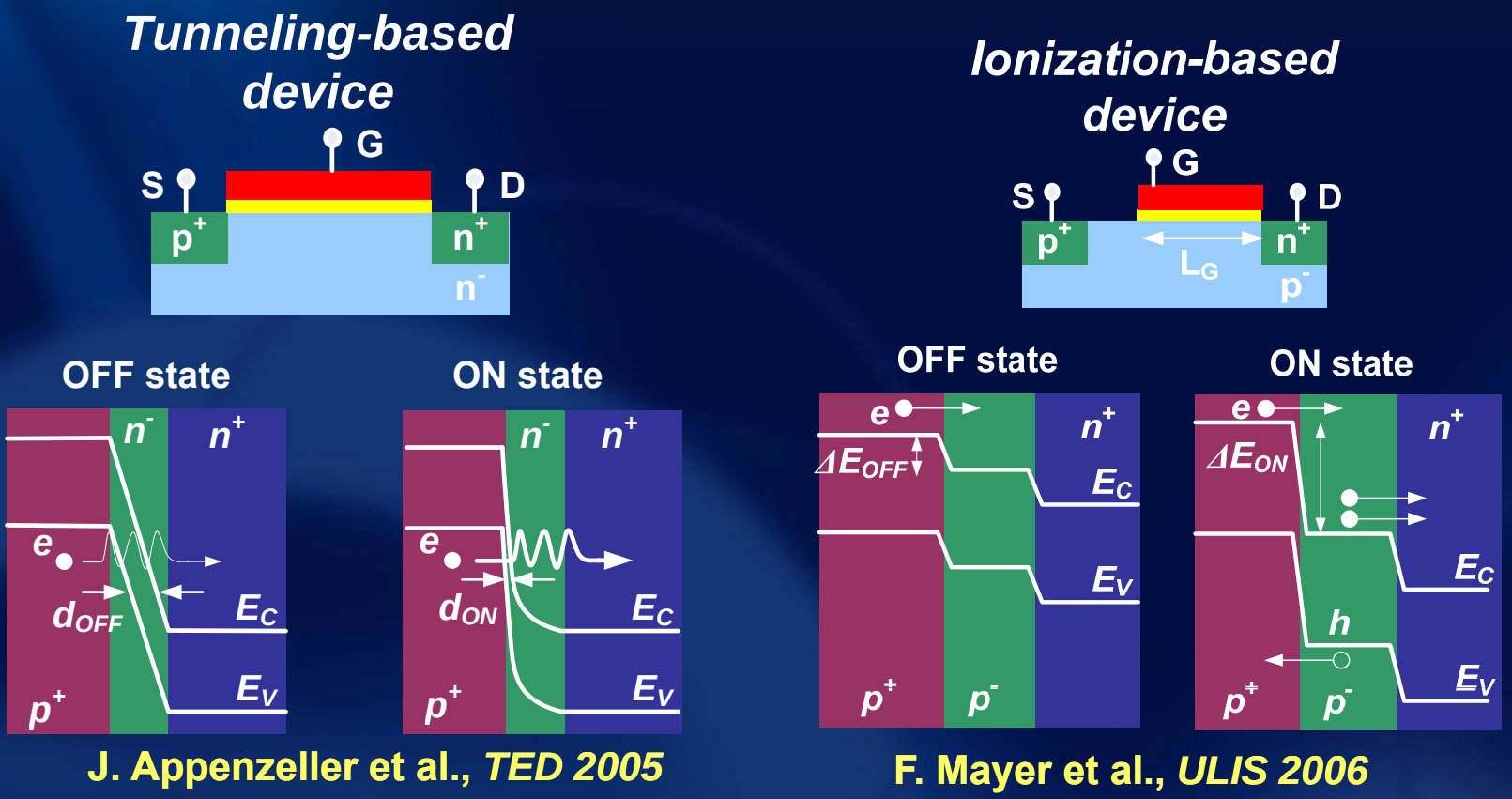


Nano Wire based devices
(Courtesy: IEEE Spectrum)



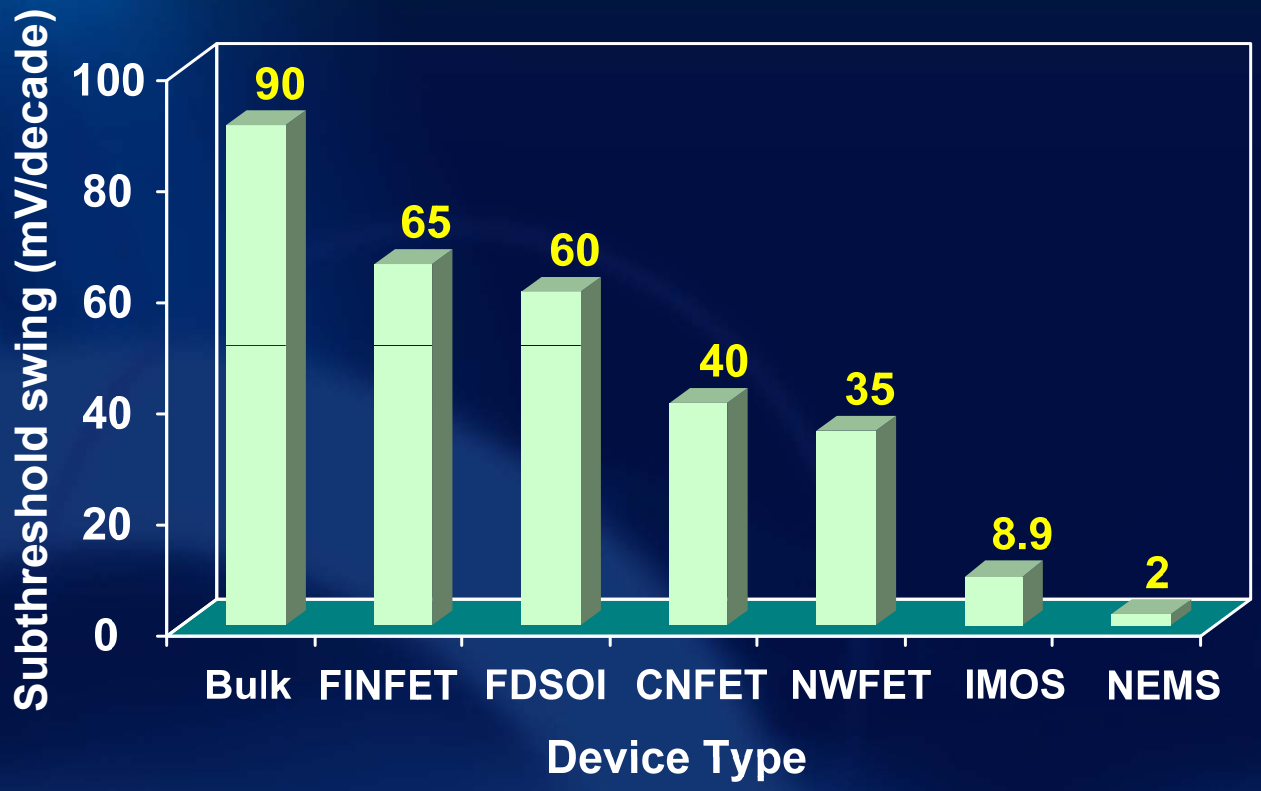
Single Electron Transistor
(Courtesy: American Physical Society)

Sub-kT/q Devices….



- **Tunneling and ionization based devices can beat the 60 mv/decade limit of bulk CMOS devices….**

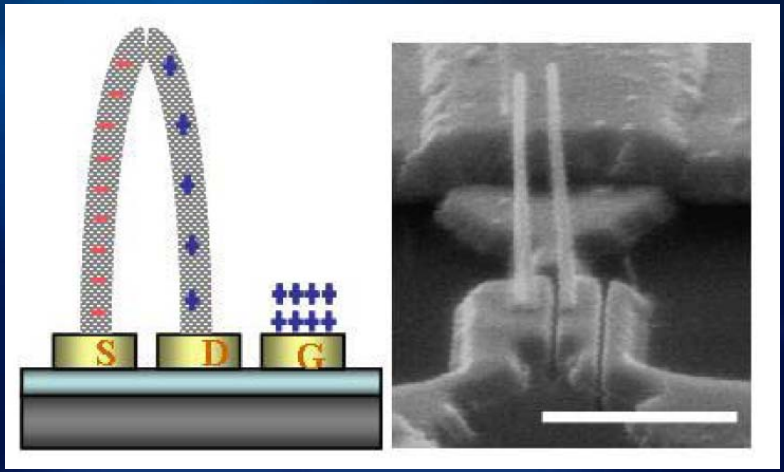
Low Sub-threshold Swing Transistors



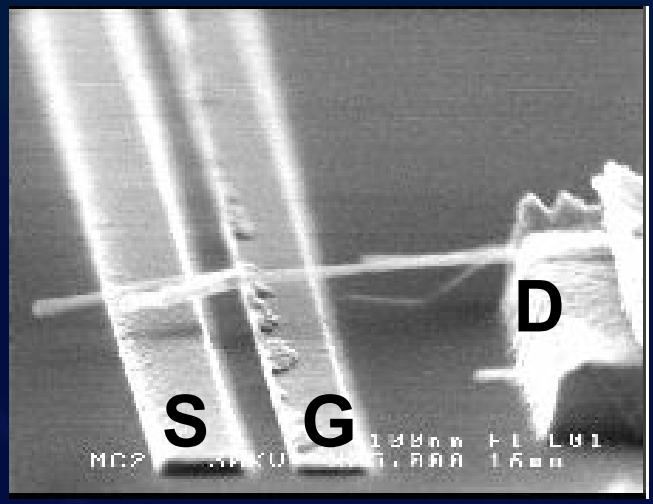
- **Minimum measured subthreshold swing value for different MOS devices reported in the literature**

  H. Dadgour and K. Banerjee, DAC 2007

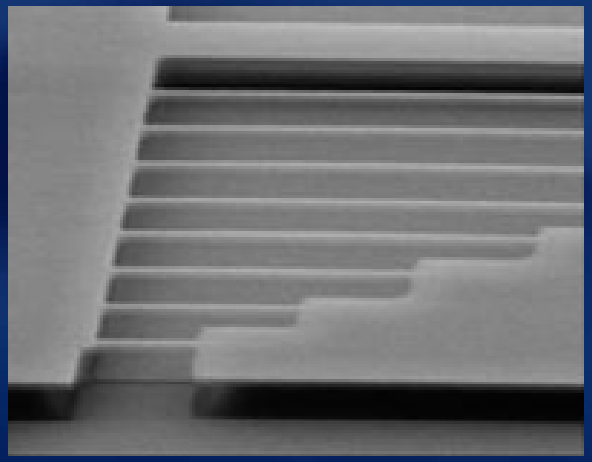
Nano-Electro Mechanical Systems (NEMS)



NEMS-based DRAM
Jang, et al. *IEDM 2005*



CNT-based relay
Lee, et al. *Appl. Phys. 2003*

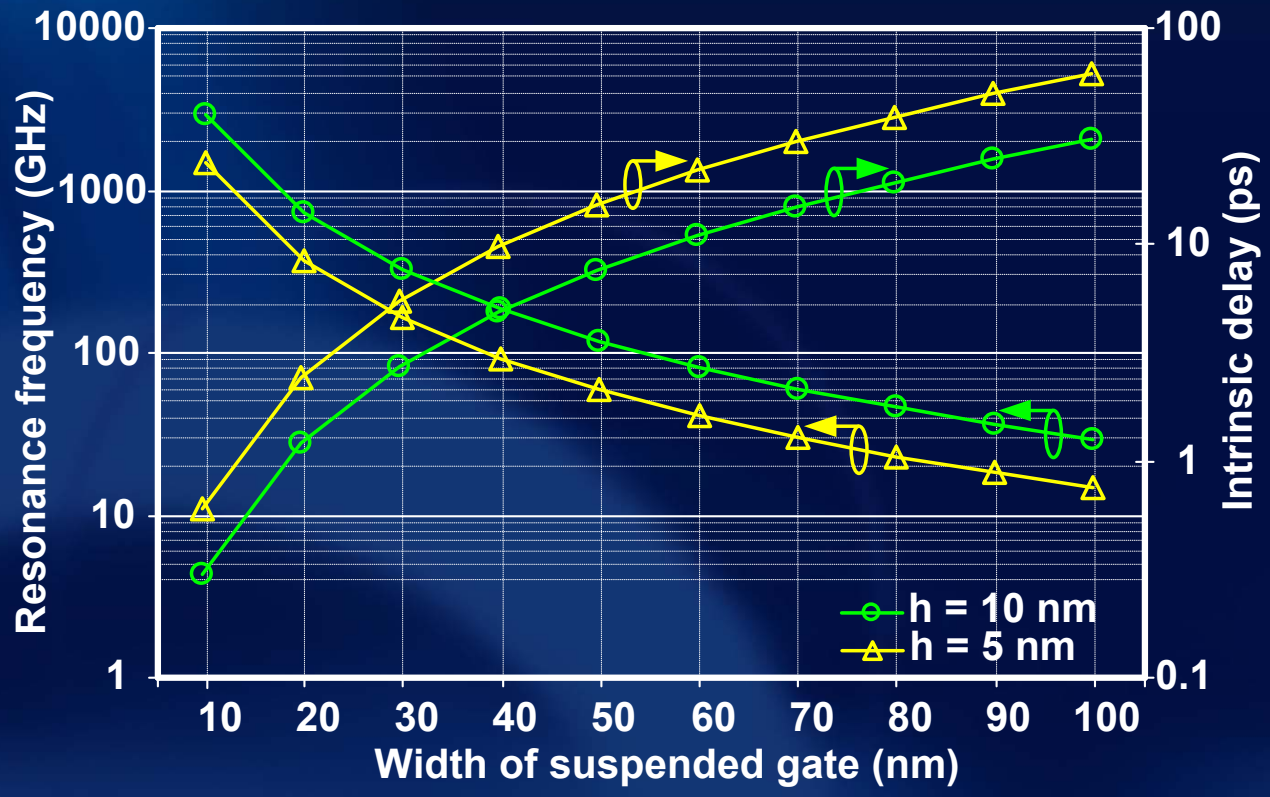


NEMS resonators
Carr, et al. *Appl. Phys. 1999*

- **NEMS can operate in GHz range due to very small mass**
- **NEMS resonators of *l = 2um* can have Resonance frequency of *400 MHz***

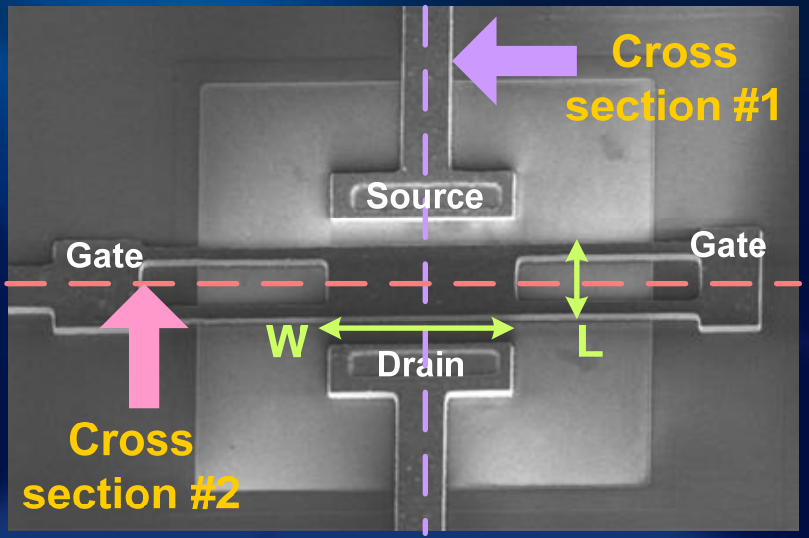
$$f_0 = \frac{(4.730)^2}{2\pi}\frac{1}{l^2}\sqrt{\frac{EI}{\rho A}}$$

High Frequency Operation of NEMS

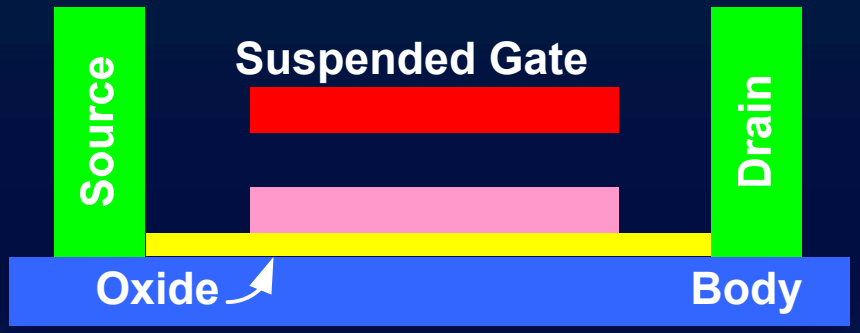


- **GHz operation is achievable by NEMS in nano-scaled technologies**

Suspended Gate MOSFET (SG-MOSFET)

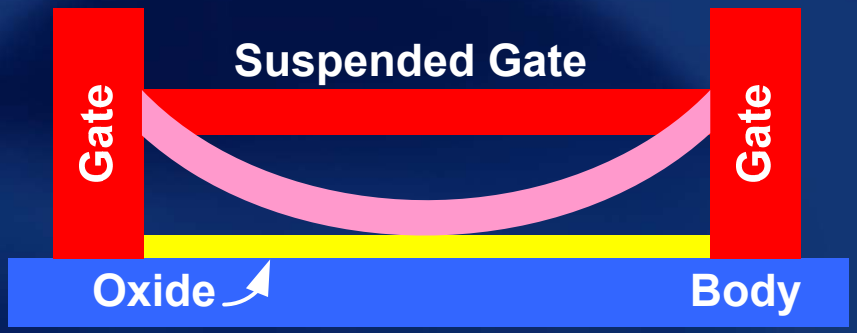


Proposed by Ionescu, et al. *ISQED 2002* & Fabricated in Abele, et al. *IEDM 2005*



Cross section #1

- Gate when the device is ON
- Gate when the device is OFF



Cross section #2

- Gate when the device is ON
- Gate when the device is OFF

Advantages

- Very low gate leakage
- Very low subthreshold leakage
- Possible Integration in CMOS process

Disadvantage

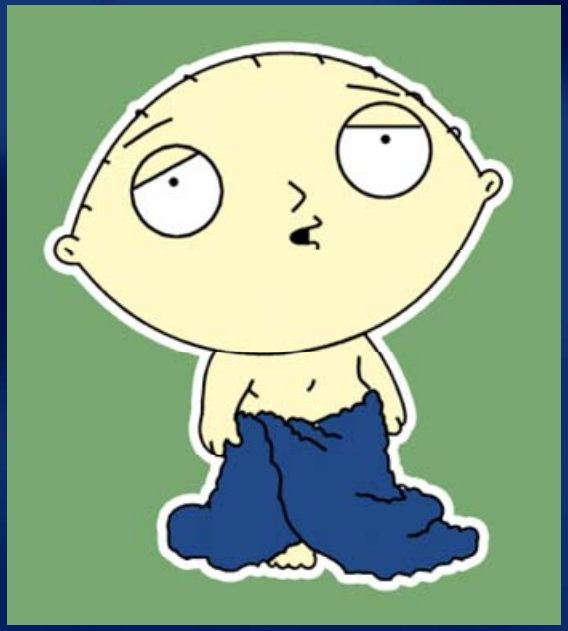
- Low ON current compared to CMOS devices

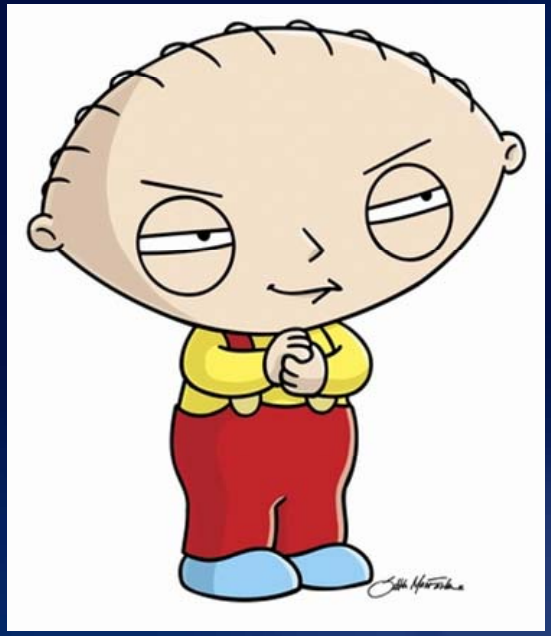
Idea: Hybrid NEMS-CMOS

CMOS ?
Very high OFF current
High ON current

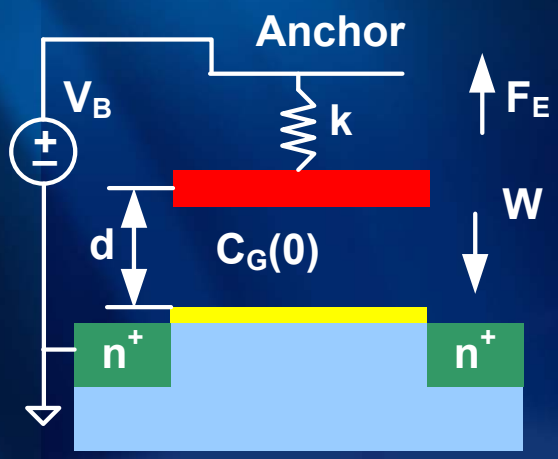
NEMS ?
Very low OFF current
Low ON current

Hybrid NEMS-CMOS
Very low OFF current
High ON current

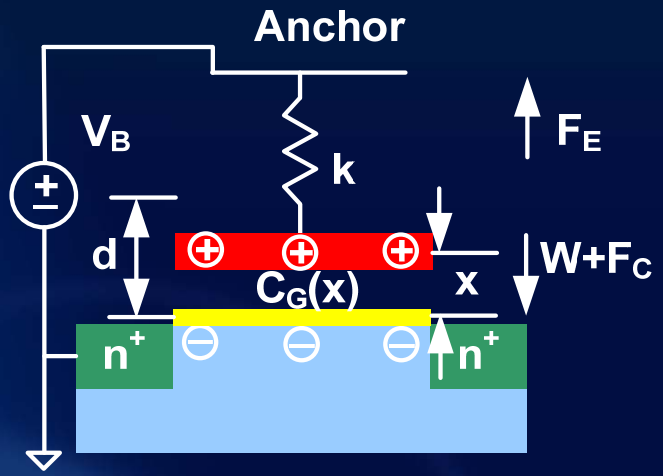




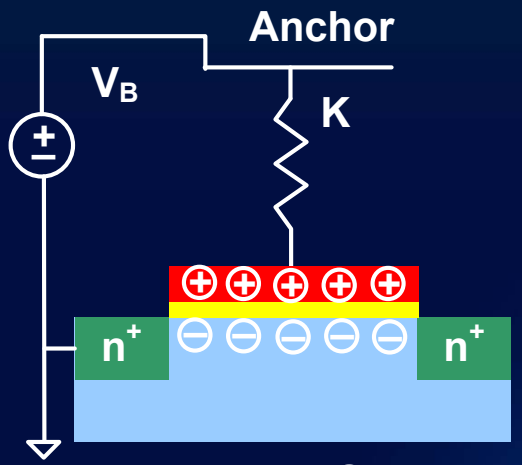
Abrupt Switching of SG-MOSFET



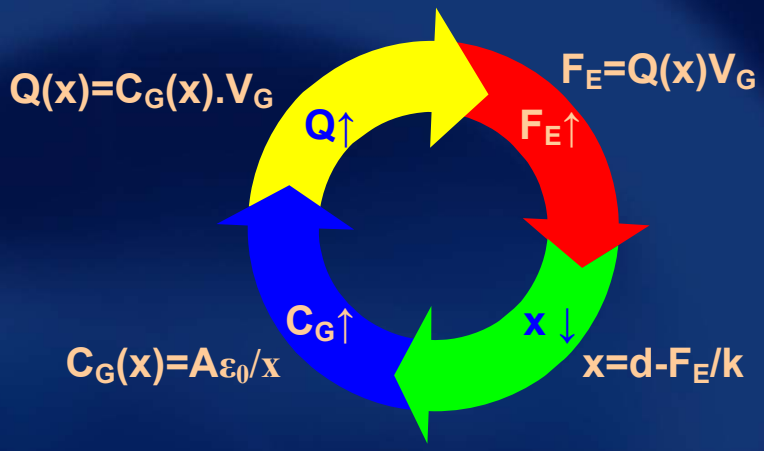
(a) V_B=0 (OFF state)

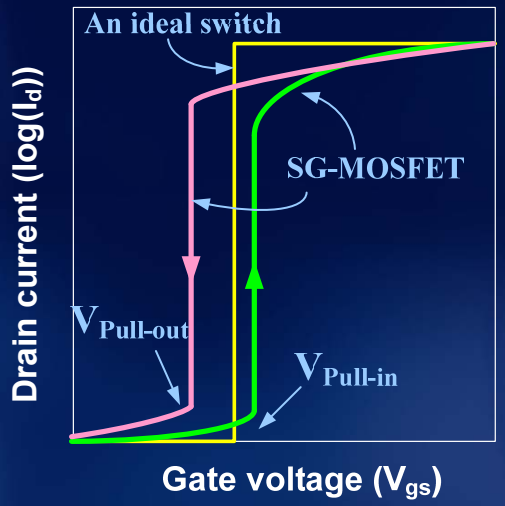


(b) $0<V_B<V_{Pull\text{-}in}$ (OFF state)



(c) $V_B>V_{Pull\text{-}in}$ (ON state)





- **Operation of SG-MOSFET under different bias conditions.**

SG-MOSFET Modeling

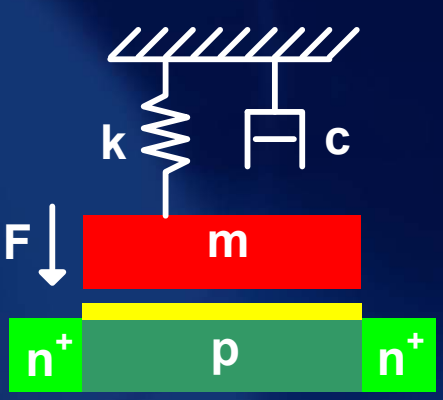
Electrical	Mechanical
$V = I.R$	$f = v.c$
$V = C\int I.dt$	$f = K^{-1}\int v.dt$
$V = L\frac{dI}{dt}$	$f = m\frac{dv}{dt}$

Analogous equations

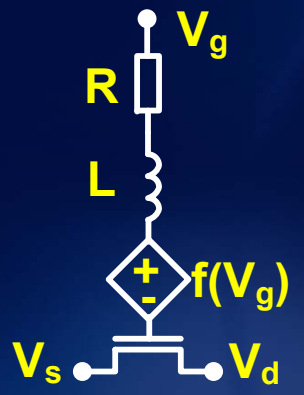
Electrical	Mechanical
Voltage, *V*	Force, *f*
Current, *I*	Velocity, *v*
Resistance, *R*	Damping, *c*
Capacitance, *C*	Stiffness^{-1},K^{-1}
Inductance, *L*	Mass, *m*

Analogous parameters

- Interaction between mechanical and electrical entities complicates modeling of SG-MOSFET
- However, a simplified equivalent HSPICE model is proposed by



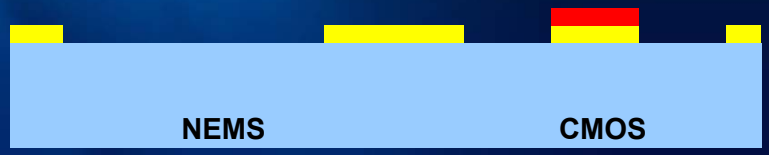
SG-MOSFET structure



Equivalent electrical model

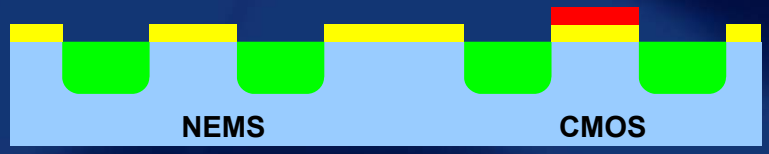
Ionescu, et al. *ISQED 2002*

Fabrication Feasibility of SG-MOSFET

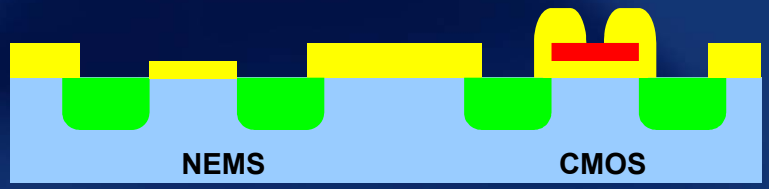


(a) Formation of poly gate for CMOS

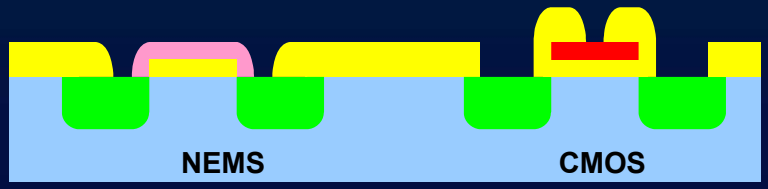
(b) Definition of active area for CMOS



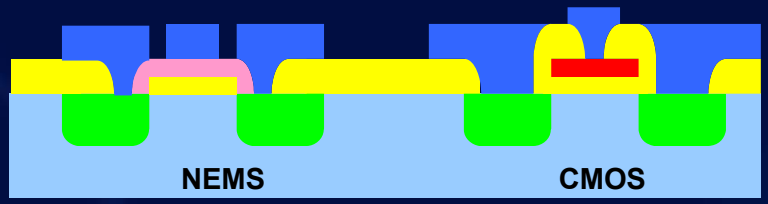
(c) Definition of active area for NEMS



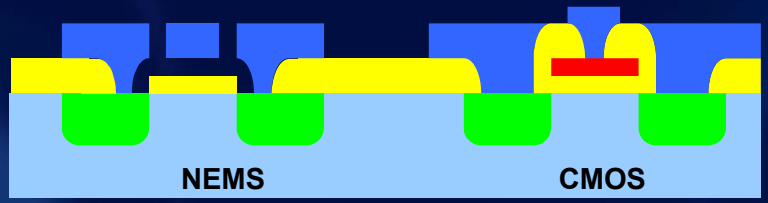
(d) Growth of thick oxide layer



(e) Sacrificial layer deposition



(f) AlSi metalization and dry etching

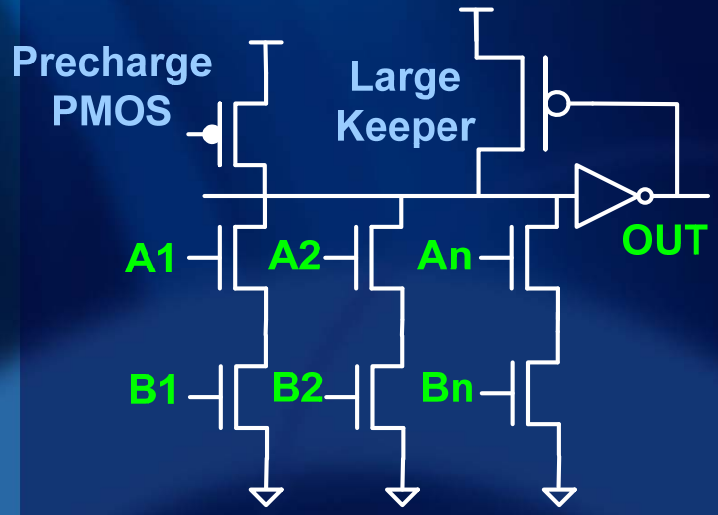


(g) Release of metal gate

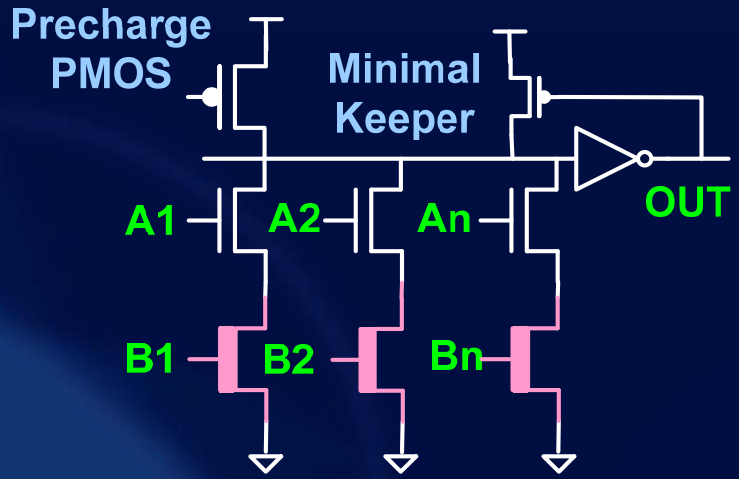
ALSi 1% Poly Oxide
Source/Drain Polymide

- **Simplified proposed fabrication model for hybrid NEMS-CMOS technology (Based on Abele, et al. *IEDM 2005*)**

Hybrid NEMS-CMOS Dynamic OR Gates



Conventional CMOS OR gate



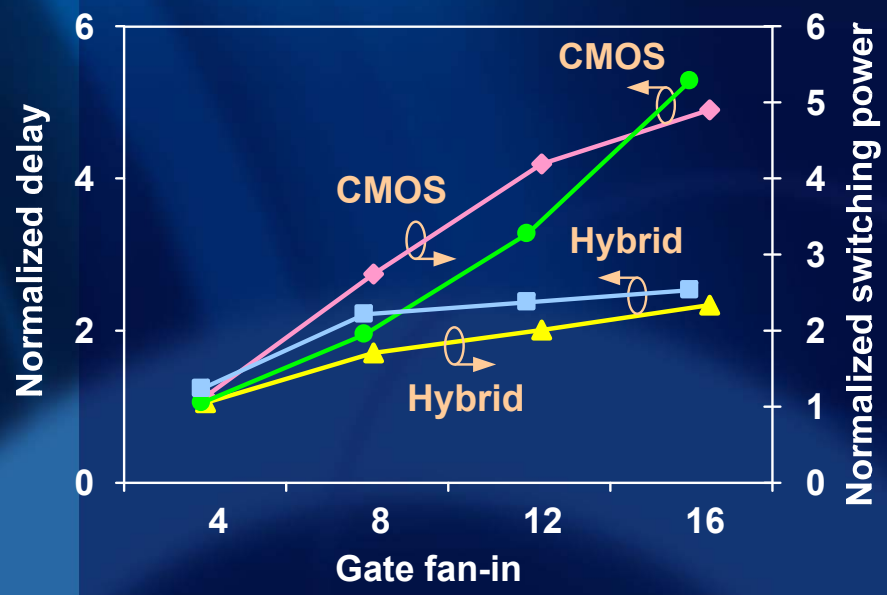
Hybrid NEMS-CMOS OR gate

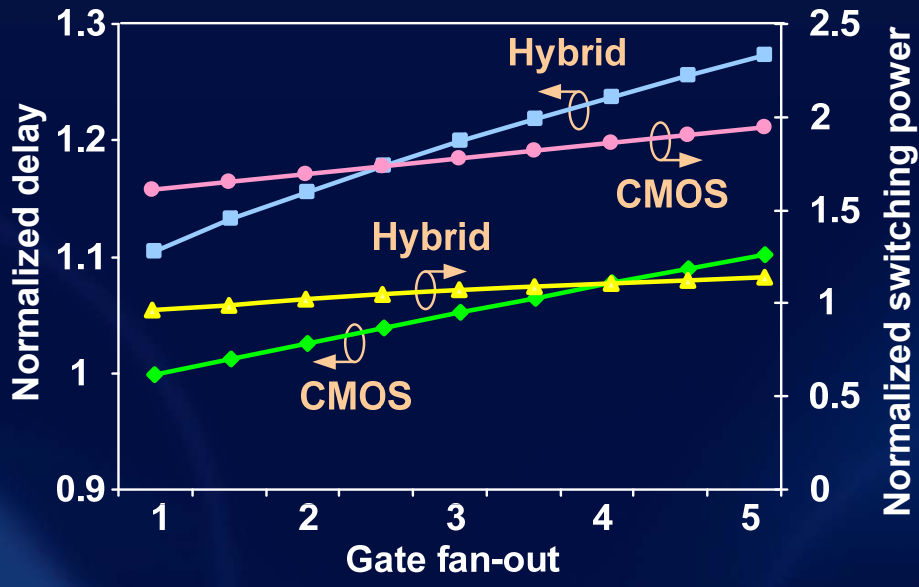
Regular CMOS

SG-MOSFET

- **SG-MOSFET devices reduce leakage and hence, allows us to use minimal-size keeper in the hybrid architecture**

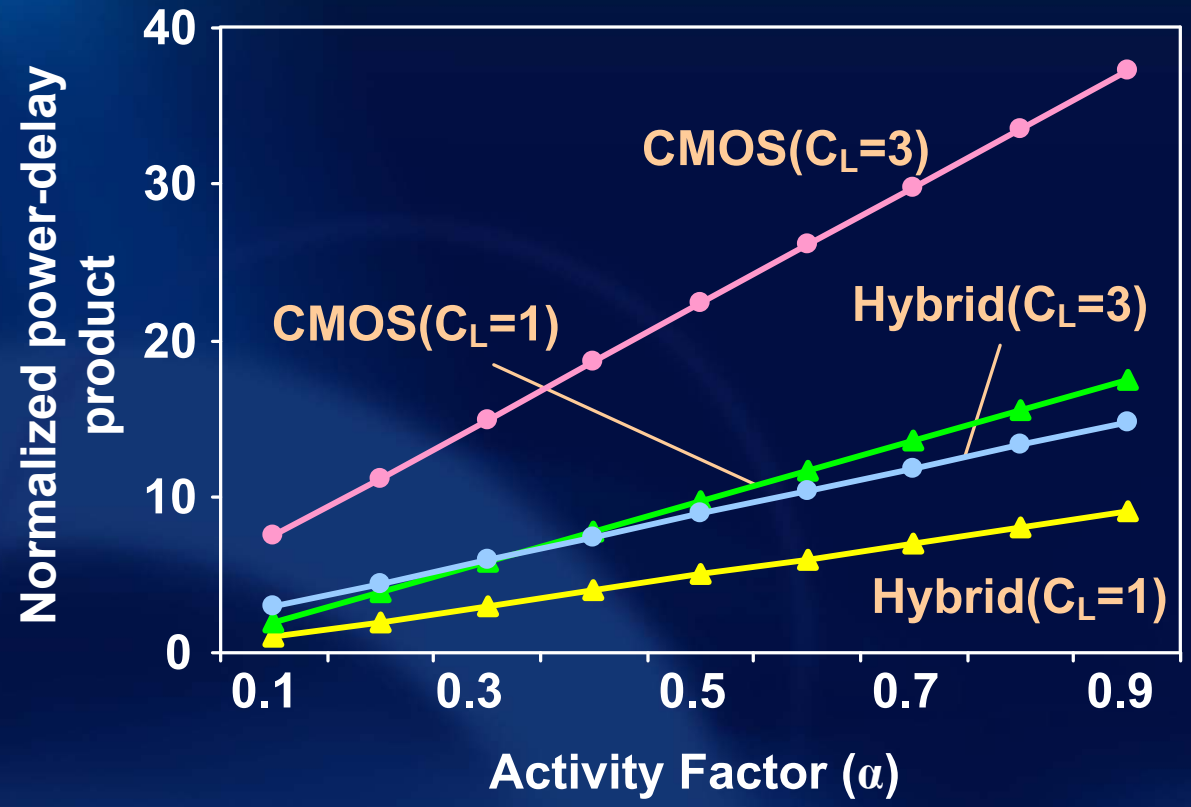
Dynamic OR Gates Simulation Results





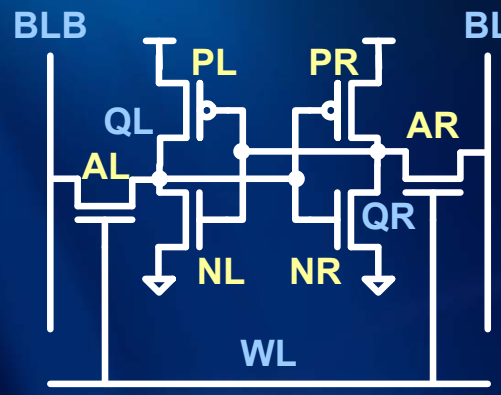
- Dynamic OR gates can achieve 60-80% lower switching power
- For high fan-in values, the hybrid gate outperforms the CMOS gate in terms of both delay and power consumption

Dynamic OR Gates Simulation Results

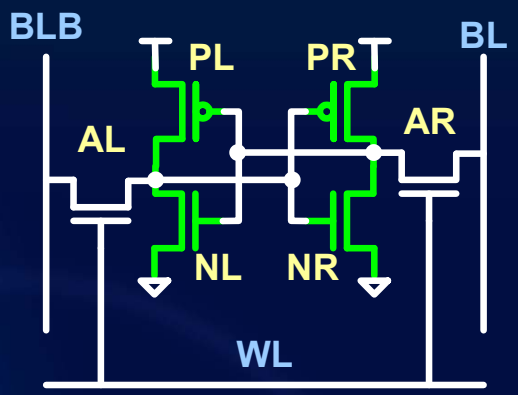


- **The hybrid gates have lower power-delay product over entire range of activity factor.**

Different Low-leakage SRAM Cell Designs



Conventional CMOS Cell

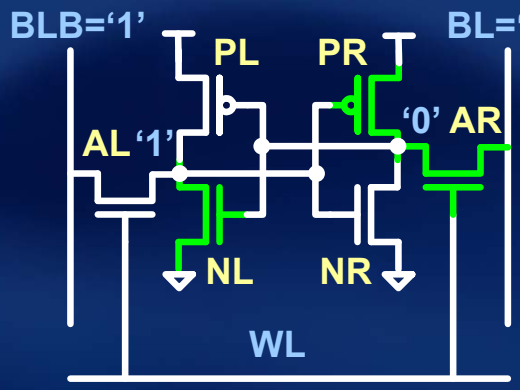


Dual V_t Cell

Hamzaoglu, et al. *ISLPED2000*

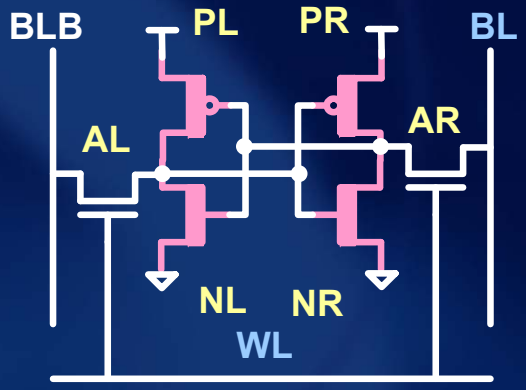
Regular CMOS

High V_t Device



Asymmetric Cell

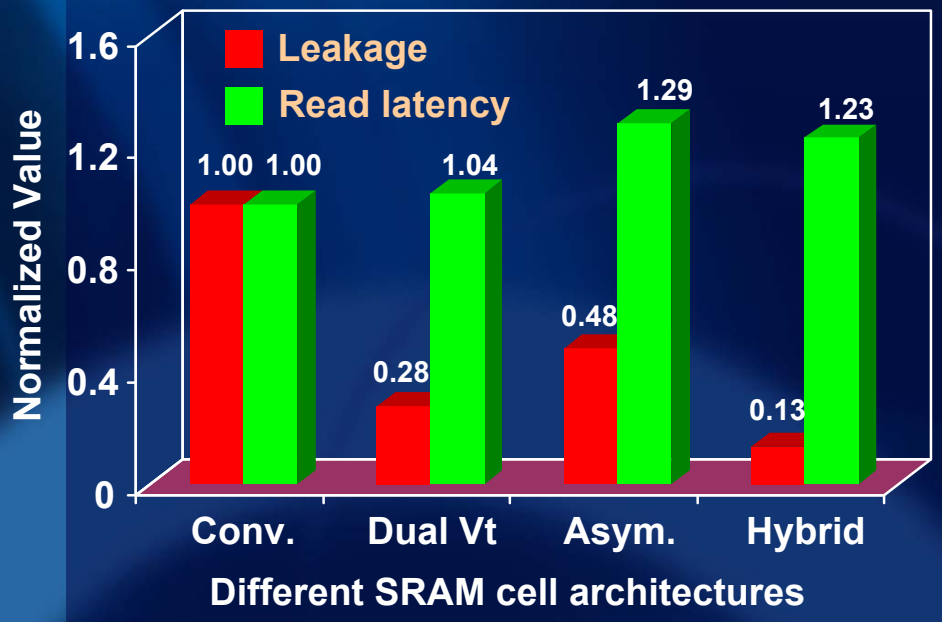
Azizi, et al. *DAC 2006*

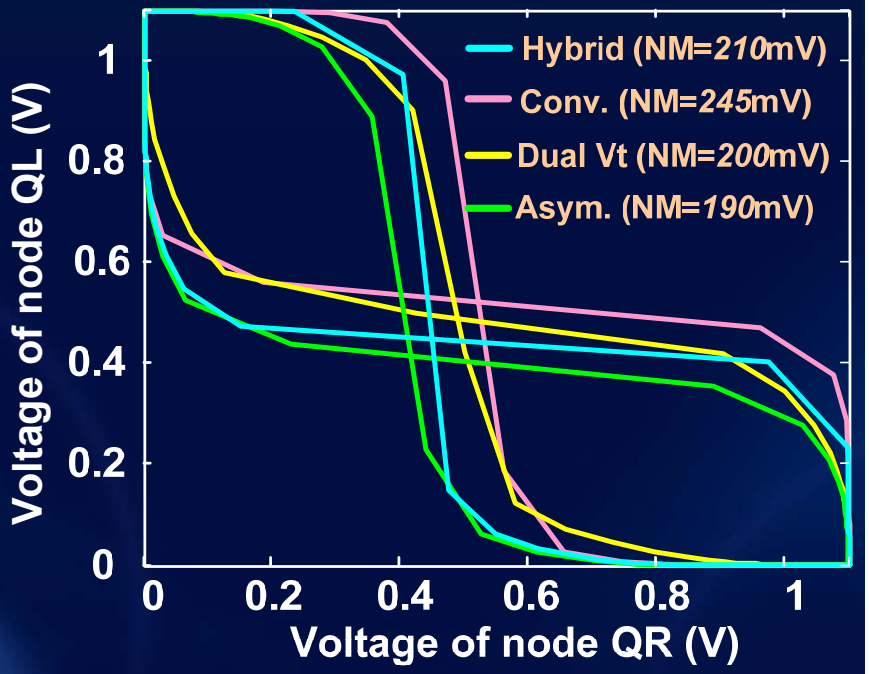


Hybrid NEMS-CMOS Cell

SG-MOSFET

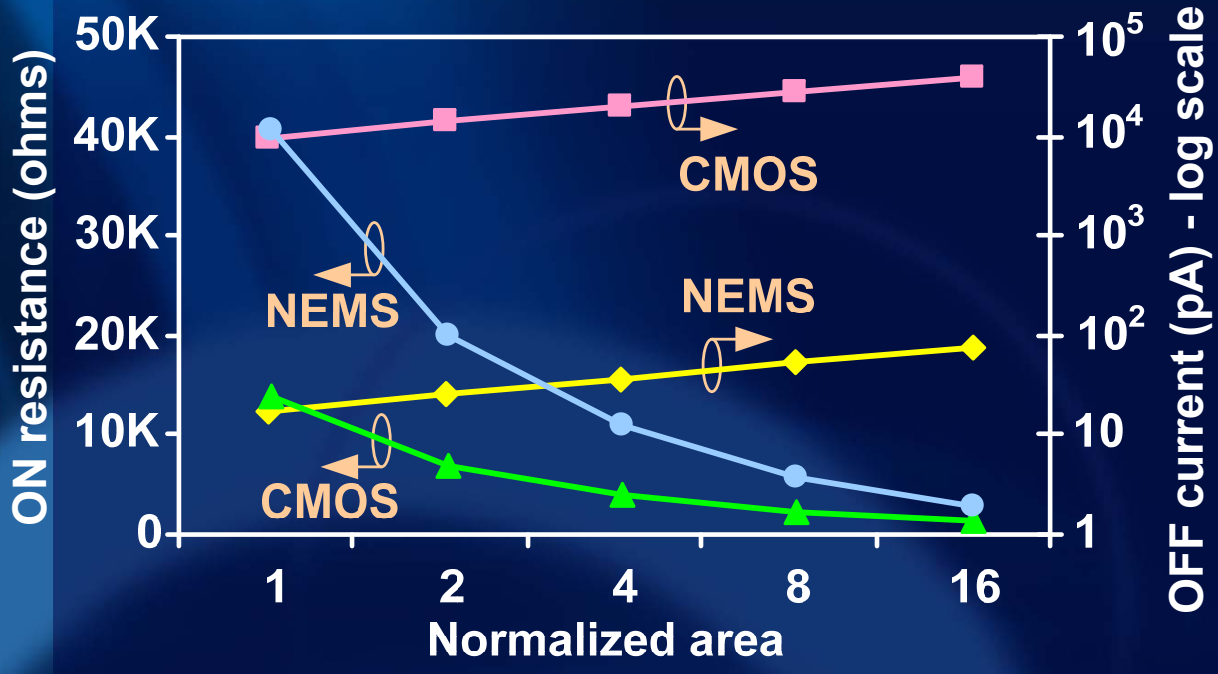
SRAM Cell Simulation Results

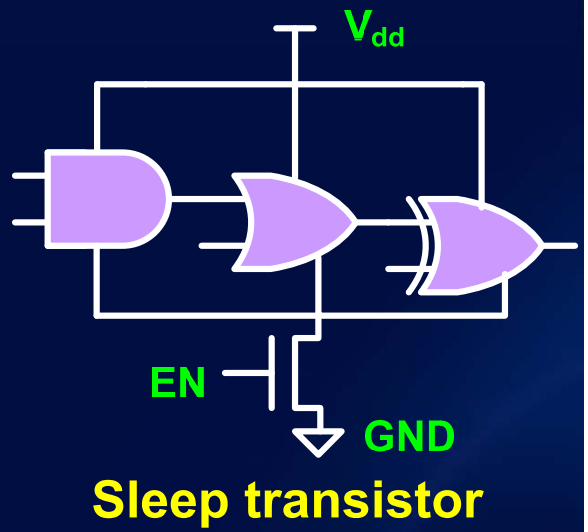




- Hybrid SRAM cell has nearly 8X lower leakage
- Hybrid cell offers higher noise margin than Asymmetric and Dual-V_t architectures

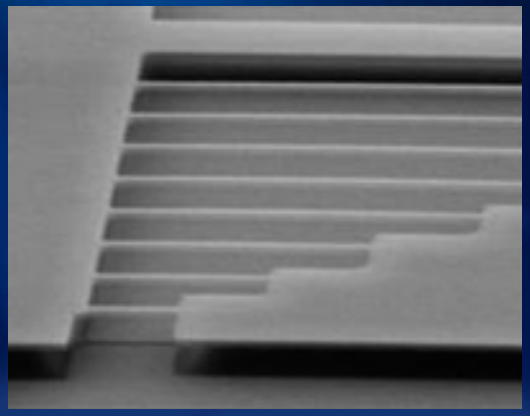
Sleep Transistor Simulation Results





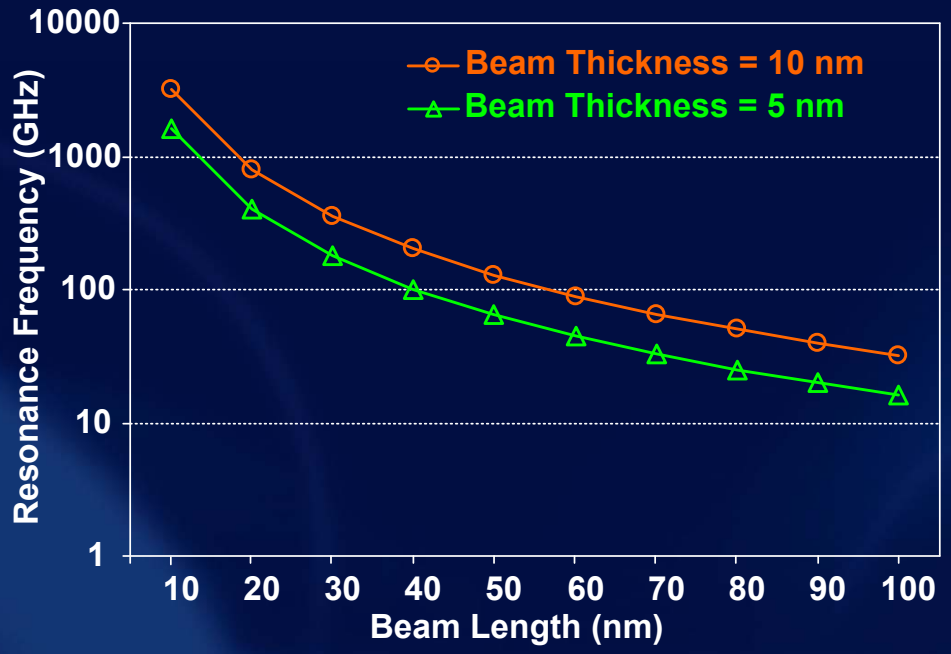
- For the same area, NEMS sleep transistors offer three orders of magnitude lower OFF current
- NEMS sleep transistors have slightly higher ON resistance

GHz Operation Using NEMS



NEMS resonators
Carr, et al. *Appl. Phys. 1999*

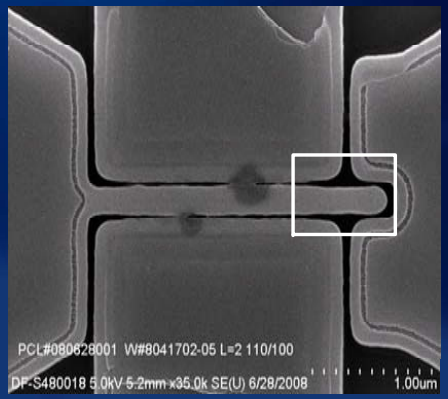
$$f_0 = \frac{(4.730)^2}{2\pi}\frac{1}{l^2}\sqrt{\frac{EI}{\rho A}}$$



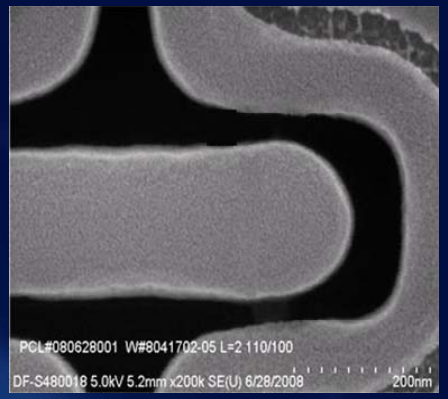
- NEMS can operate in GHz range due to very small mass
- NEMS resonators of *l = 2um* can have Resonance frequency of *400 MHz*

Laterally-Actuated Double-Gate NEMS

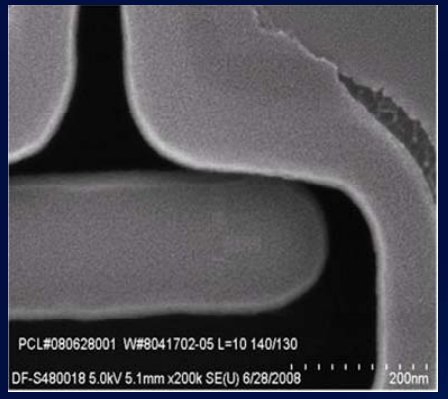
SEM picture



OFF state

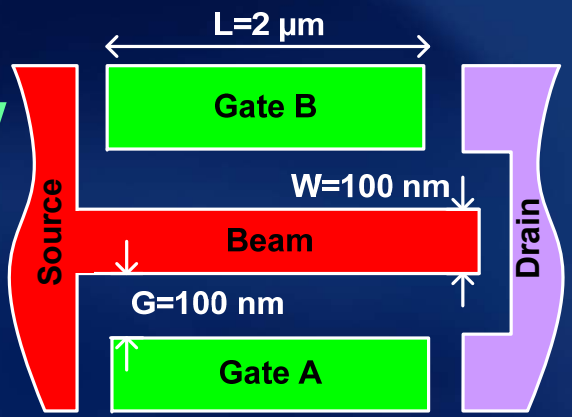


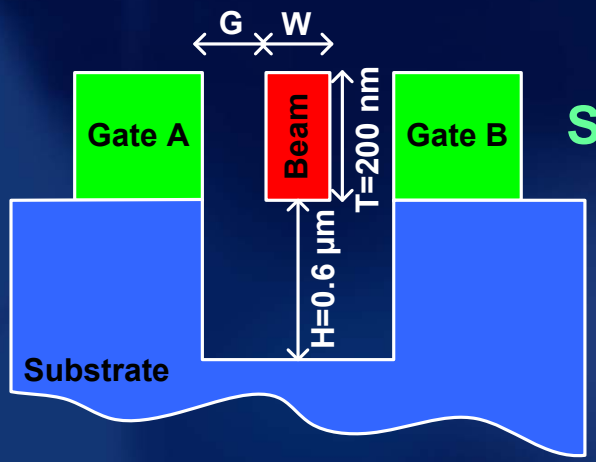
ON state



Dadgour et al., DAC 2010

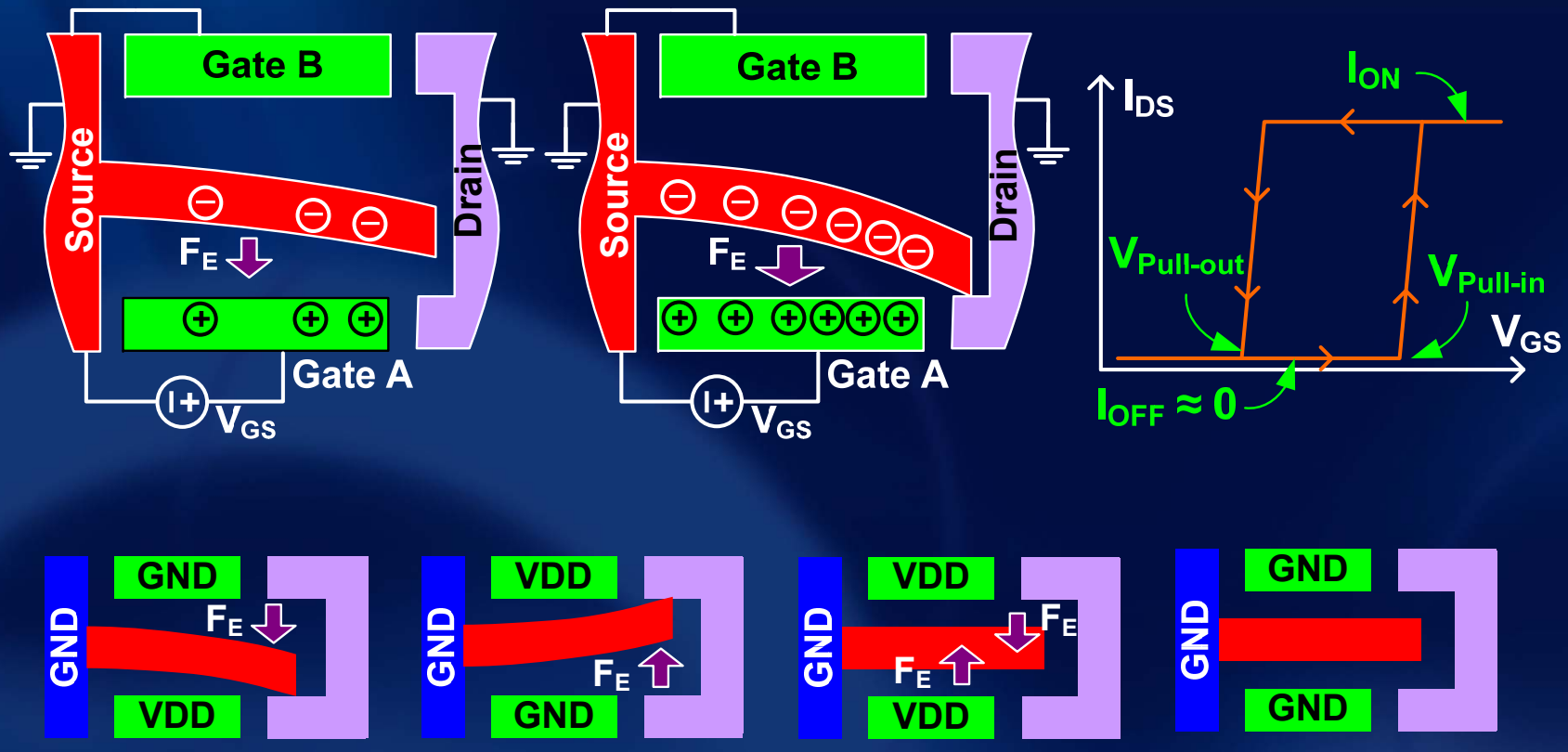
Top View





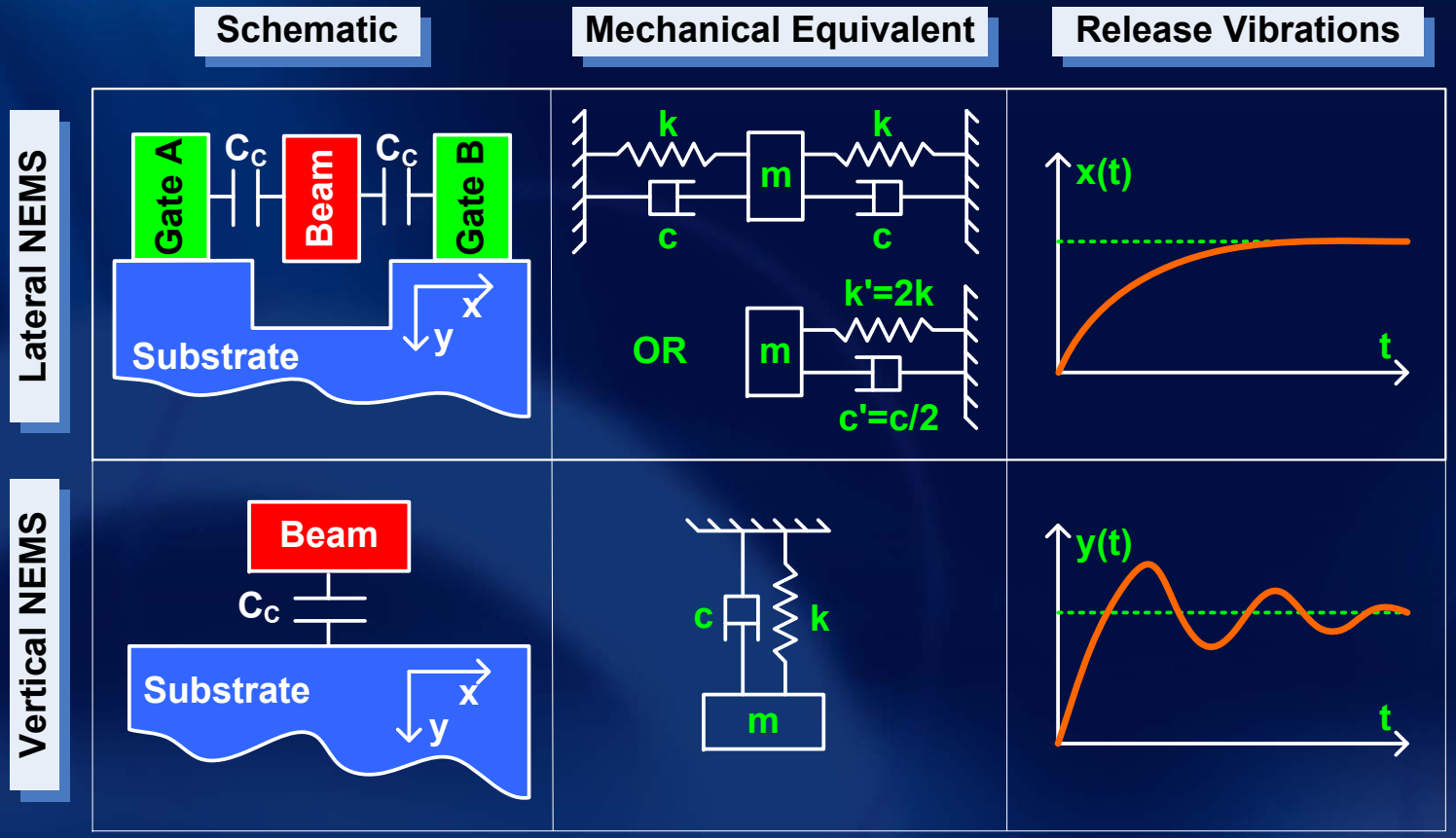
Side View

The Basic Operation of the Device



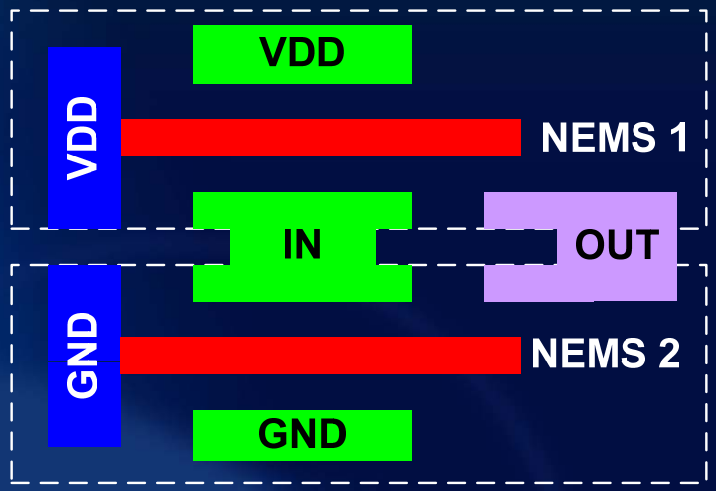
- Depending on the bias condition, the beam can deflect and form a conduction path between source and drain terminals

Lateral vs. Vertical NEMS

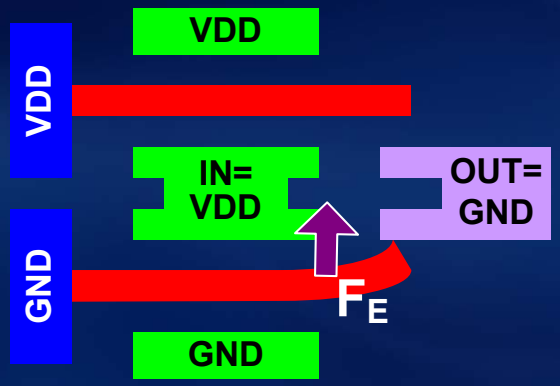


- **Lateral NEMS offer smoother switching responses**

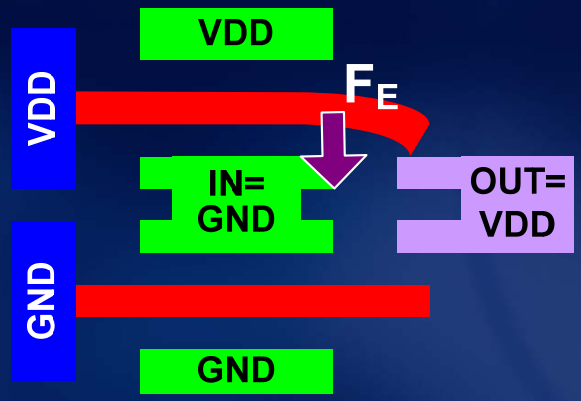
Inverter Gate



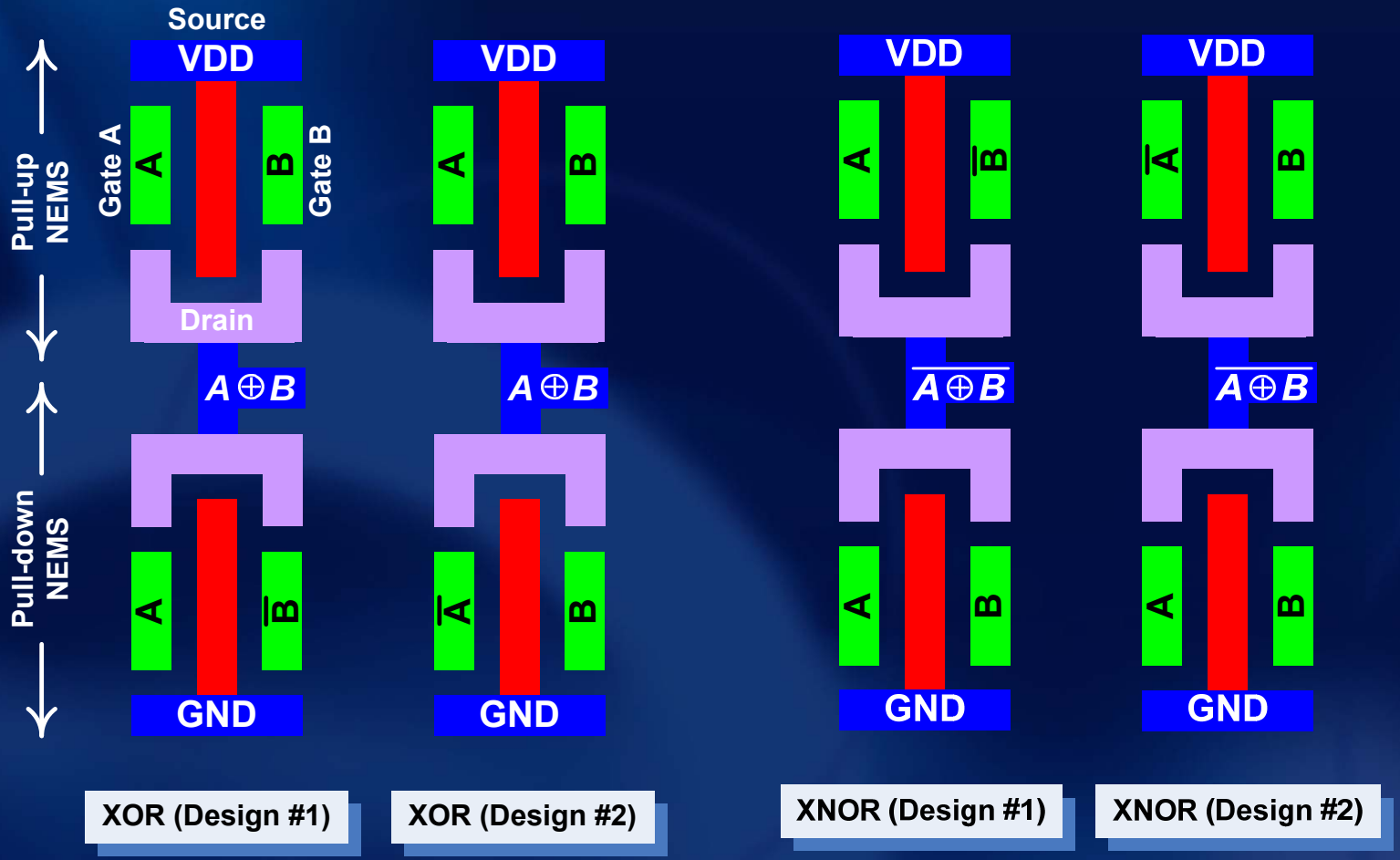
IN=VDD & OUT=GND



IN=GND & OUT=VDD



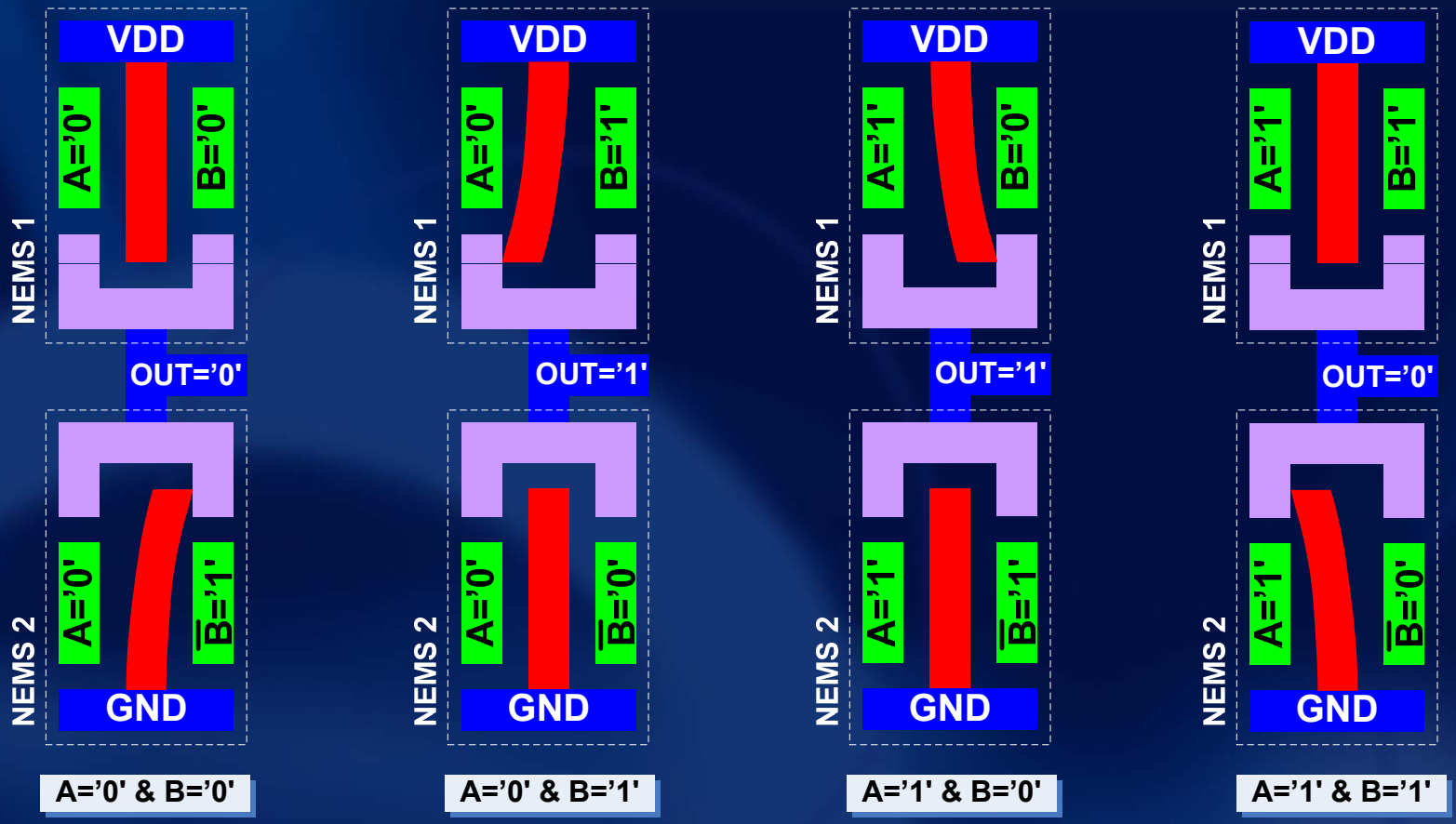
XOR/XNOR Gates



XOR (Design #1) XOR (Design #2) XNOR (Design #1) XNOR (Design #2)

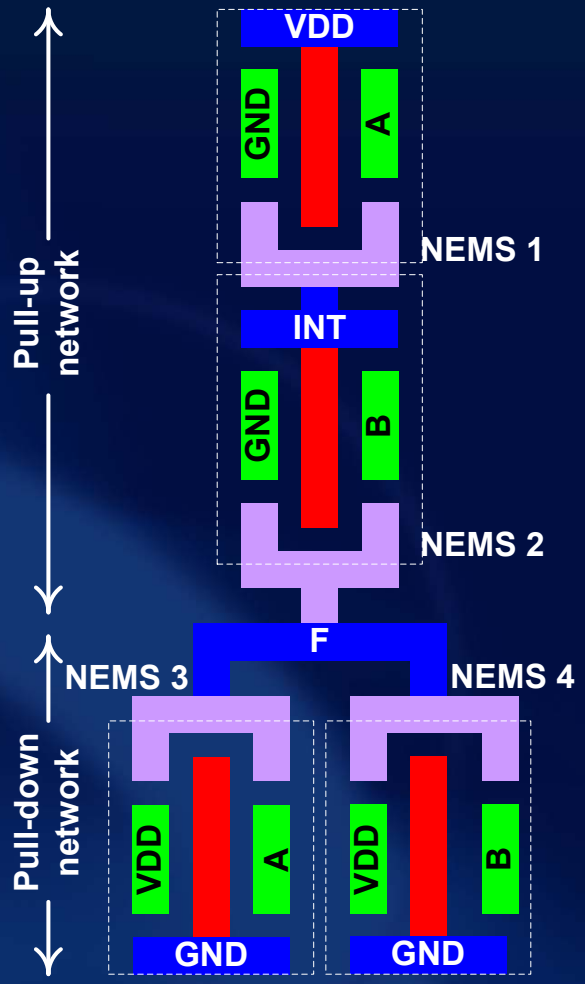
- Alternative implementations of XOR/XNOR gates

The Operation of the XOR Gate



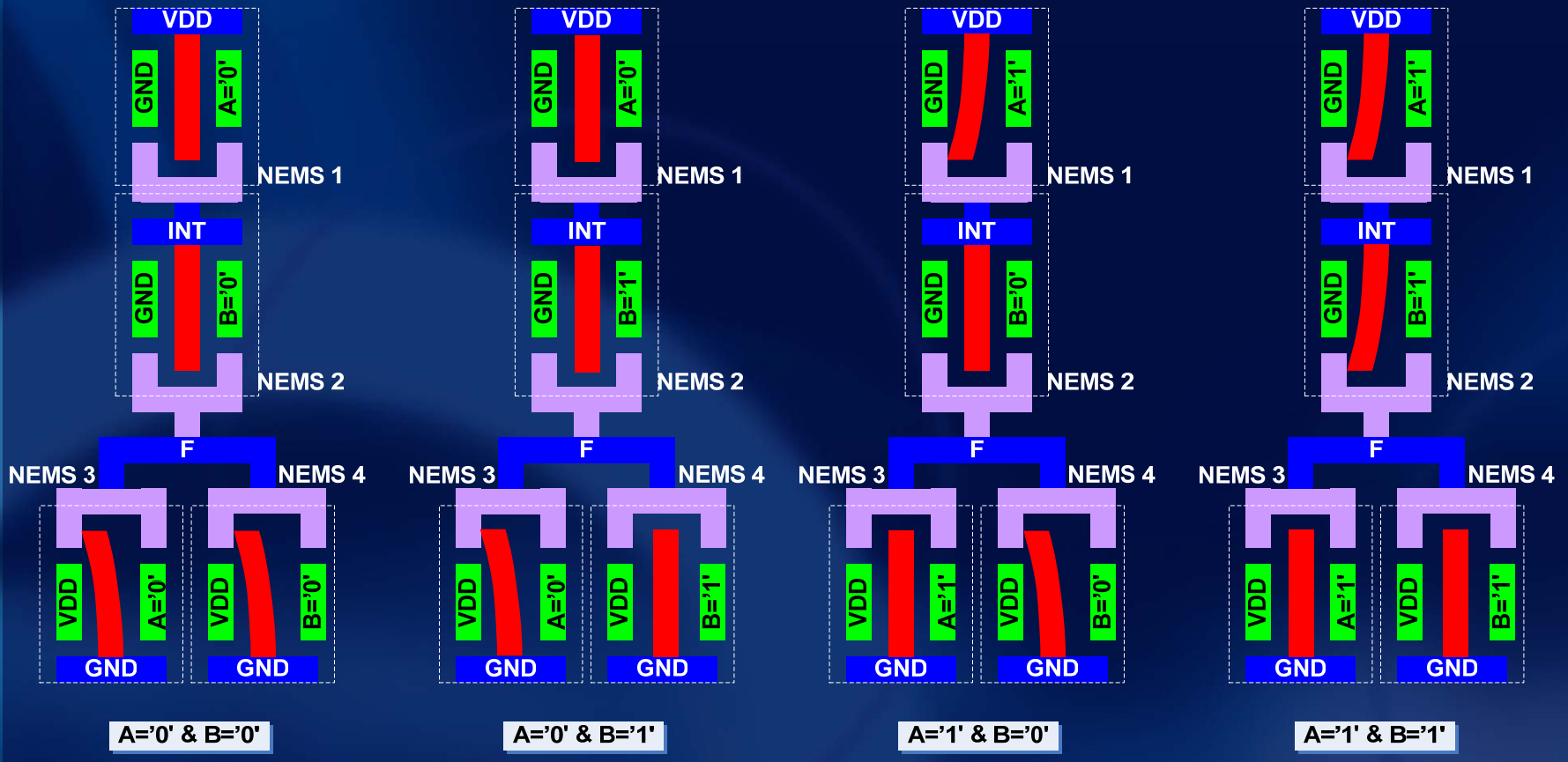
- The operation of the XOR gate for all possible input combinations

AND Gates



- The implementation of a two-input AND gate

The Operation of the AND Gate



- The operation of the AND gate for all possible input combinations

Karnaugh maps (K-maps)

Dadgour et al., ISLPED 2010

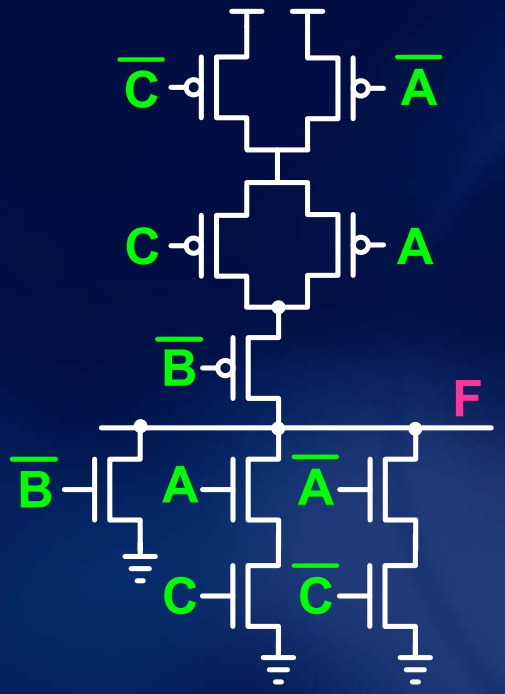
C \ AB	00	01	11	10
0	0	1	1	0
1	0	1	0	0

$$F = \bar{A}BC + \bar{A}B\bar{C} + \bar{A}B\bar{C} + AB\bar{C}$$

$$\rightarrow F = \bar{A}B + B\bar{C}$$

C \ AB	00	01	11	10
0	0	0	1	0
1	0	1	0	0

$$F = AB\bar{C} + \bar{A}BC = B(A\bar{C} + \bar{A}C)$$



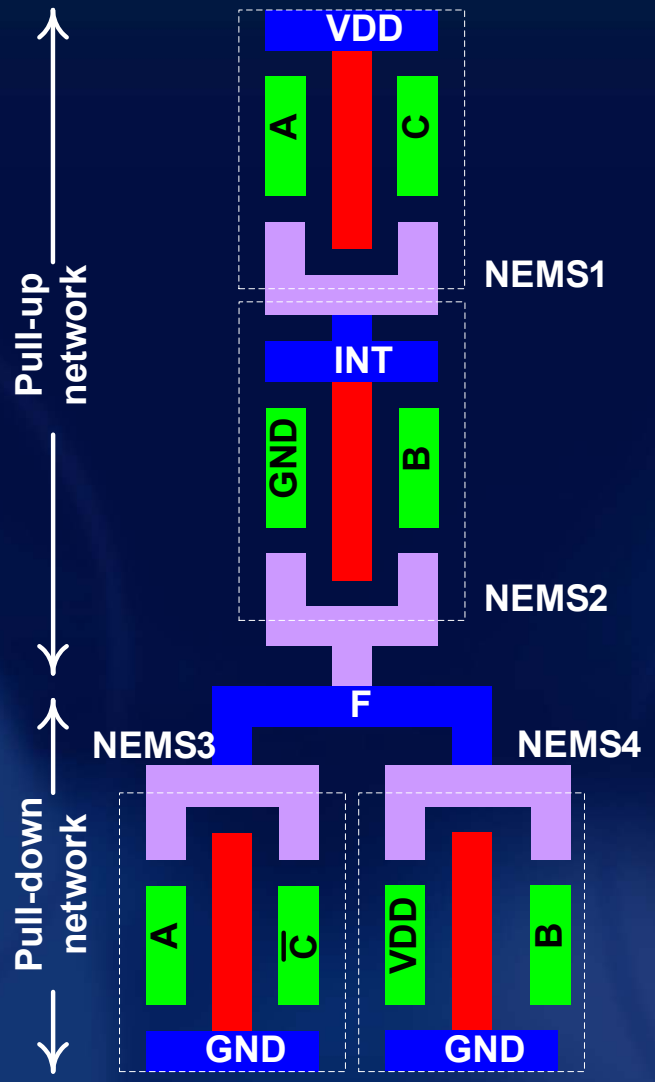
- In the standard Karnaugh map approach, only horizontal and vertical groupings of ‘1’s are allowed

The New Logic Minimization Paradigm

C \ AB	00	01	11	10
0	0	0	1	0
1	0	1	0	0

$$F = AB\bar{C} + \bar{A}BC = B(A\bar{C} + \bar{A}C) = B(A \oplus C)$$

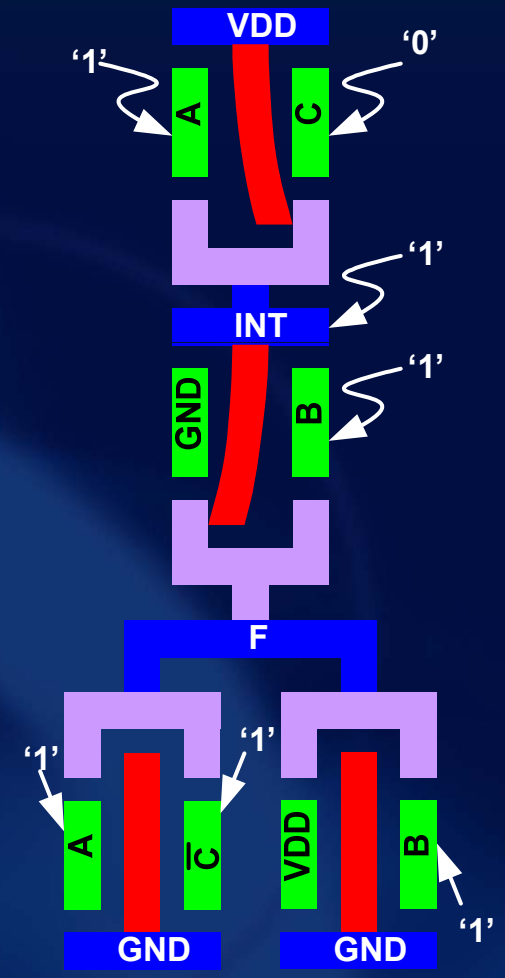
- The availability of compact XOR/XNOR gates allows the diagonal grouping of ‘1’s



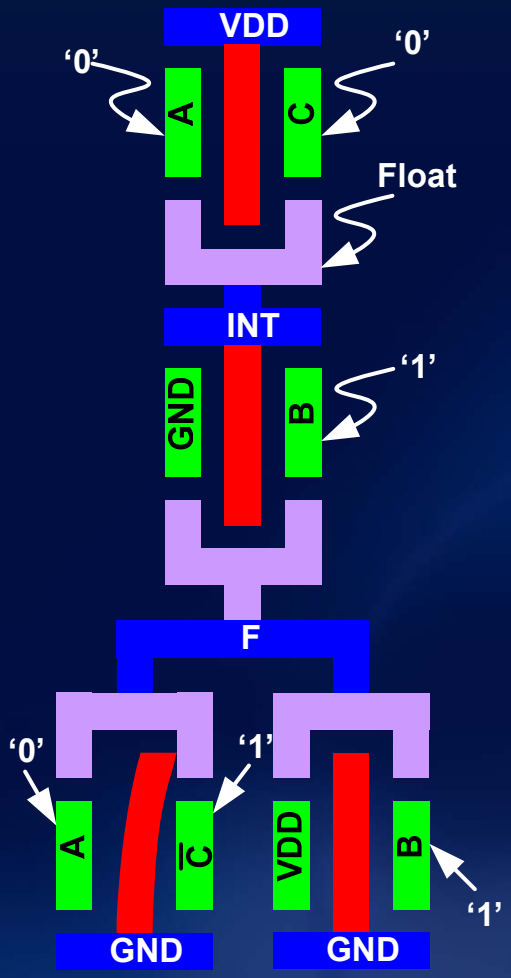
Verification of the Design

C \ AB	00	01	11	10
0	0	0	1	0
1	0	1	0	0

$$F = AB\overline{C} + \overline{A}BC = B(A\overline{C} + \overline{A}C) = B(A \oplus C)$$



A='1' & B='1' & C='0'

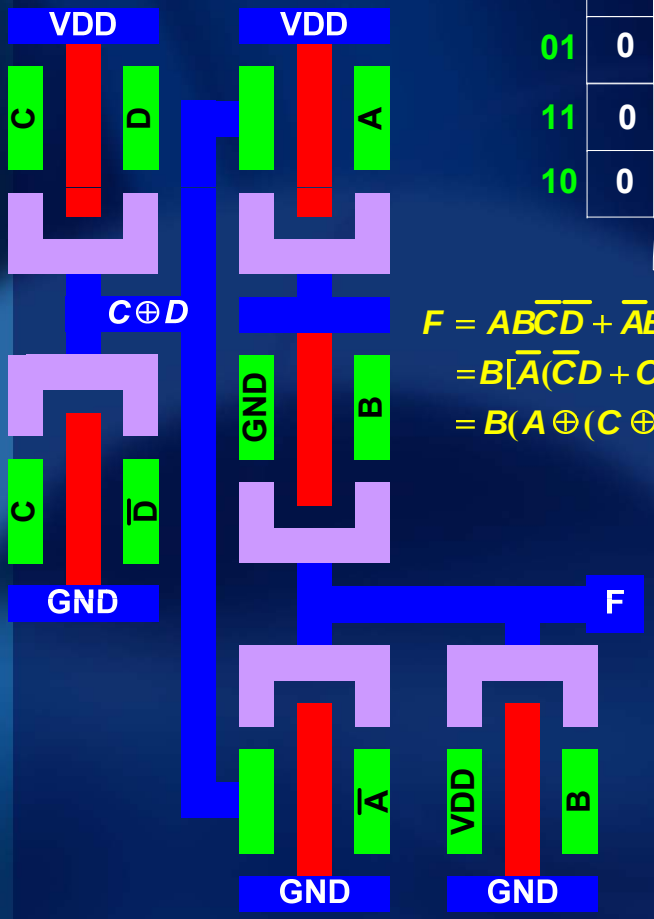


A='0' & B='1' & C='0'

More Design Examples

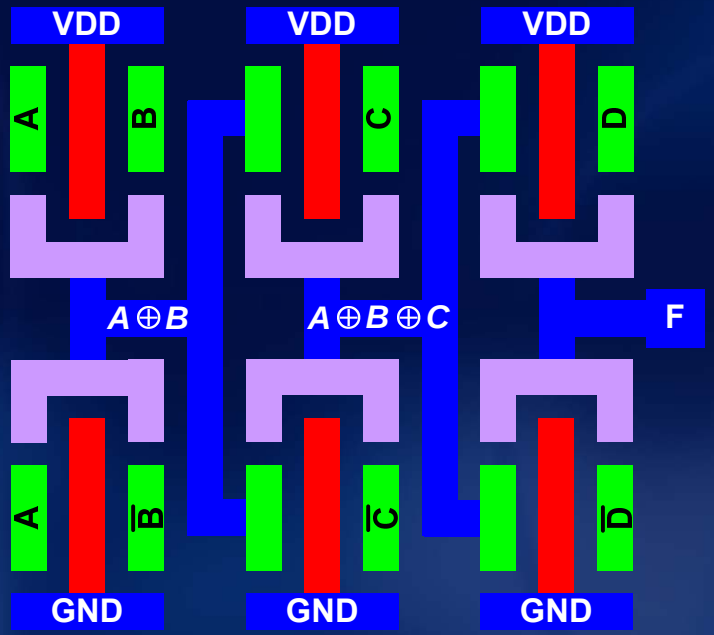
CD \ AB	00	01	11	10
00	0	0	1	0
01	0	1	0	0
11	0	0	1	0
10	0	1	0	0

$$F = AB\overline{C}\,\overline{D} + \overline{A}B\overline{C}\,\overline{D} + ABCD + \overline{A}BC\overline{D}$$
$$= B[\overline{A}(\overline{C}D + C\overline{D}) + A(CD + \overline{C}\,\overline{D})]$$
$$= B(A \oplus (C \oplus D))$$



CD \ AB	00	01	11	10
00	0	1	0	1
01	1	0	1	0
11	0	1	0	1
10	1	0	1	0

$$F = (A \oplus (B \oplus (C \oplus D)))$$



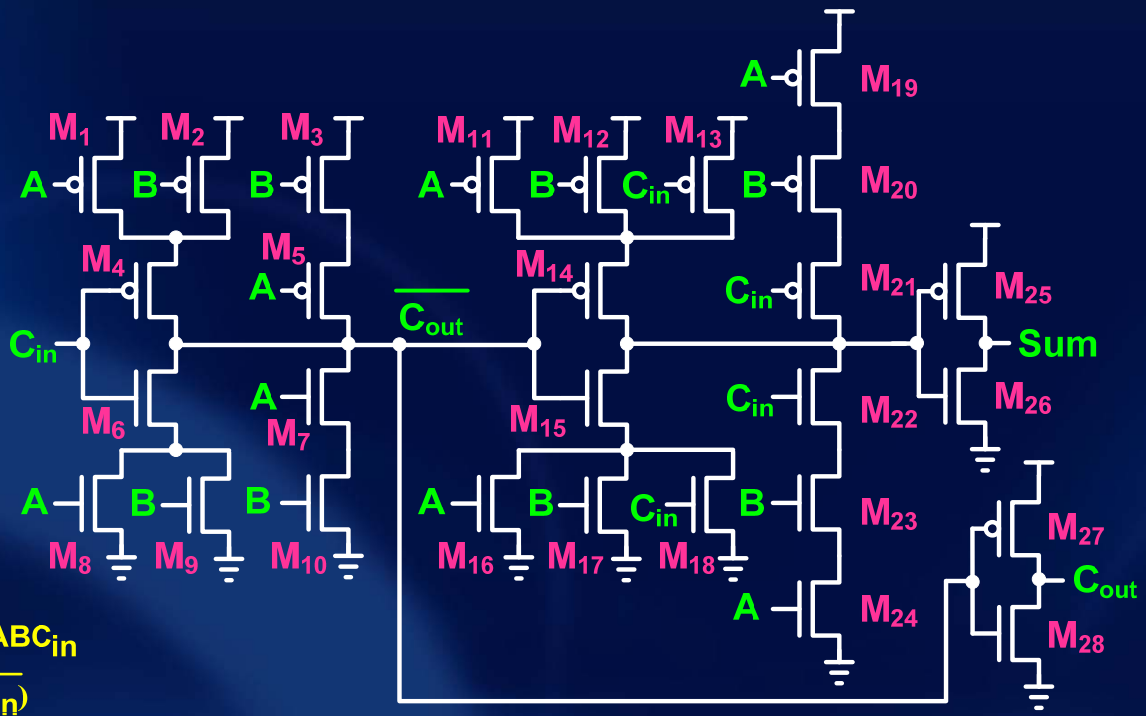
Standard CMOS-Based Full-Adder

Sum

C_{in} \ AB	00	01	11	10
0	0	1	0	1
1	1	0	1	0

C_{out}

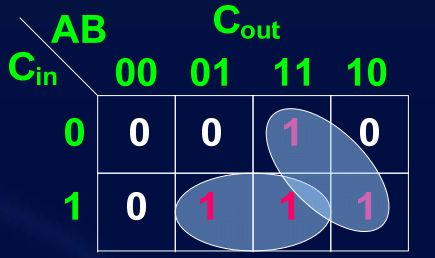
C_{in} \ AB	00	01	11	10
0	0	0	1	0
1	0	1	1	1



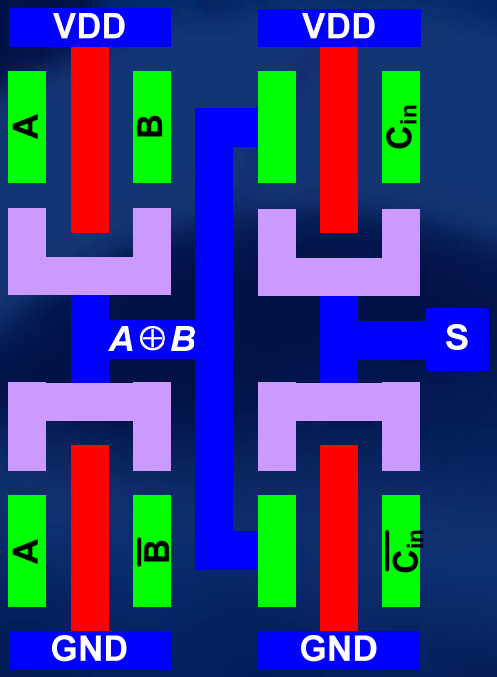
$$C_{out} = AB + AC_{in} + BC_{in}$$

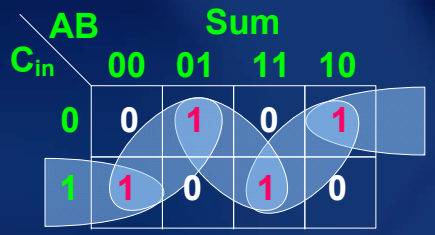
$$\begin{aligned}
Sum &= A\bar{B}\bar{C}_{in} + B\bar{A}\bar{C}_{in} + C_{in}\bar{A}\bar{B} + ABC_{in} \\
&= A(\bar{B}\bar{C}_{in} + \bar{A}\bar{C}_{in} + \bar{A}\bar{B} + \overline{ABC_{in}}) \\
&\quad + B(\bar{B}\bar{C}_{in} + \bar{A}\bar{C}_{in} + \bar{A}\bar{B} + \overline{ABC_{in}}) \\
&\quad + C_{in}(\bar{B}\bar{C}_{in} + \bar{A}\bar{C}_{in} + \bar{A}\bar{B} + \overline{ABC_{in}}) + ABC_{in} \\
&= (A + B + C_{in})[\bar{B}\bar{C}_{in} + \bar{A}\bar{C}_{in} + \bar{A}\bar{B} + \overline{ABC_{in}}] + ABC_{in} \\
&= (A + B + C_{in})\overline{C_{out}} + ABC_{in}
\end{aligned}$$

NEMS-Based Full-Adder

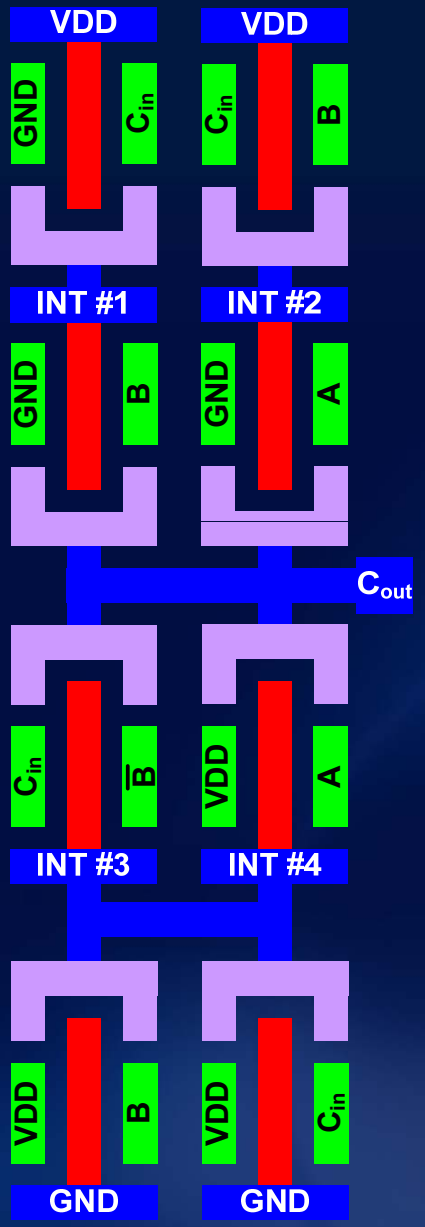


$C_{out} = BC_{in} + A(B \oplus C_{in})$

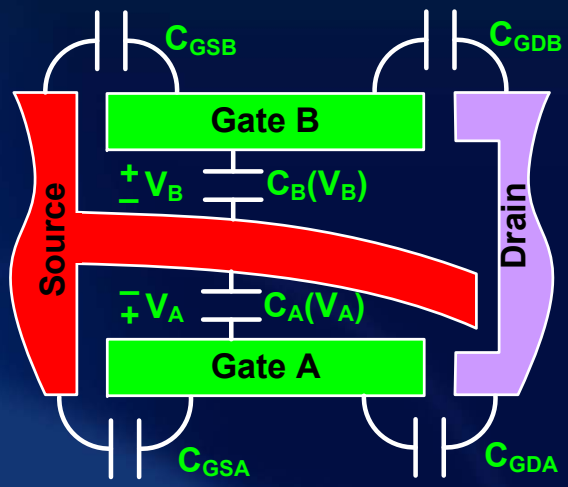


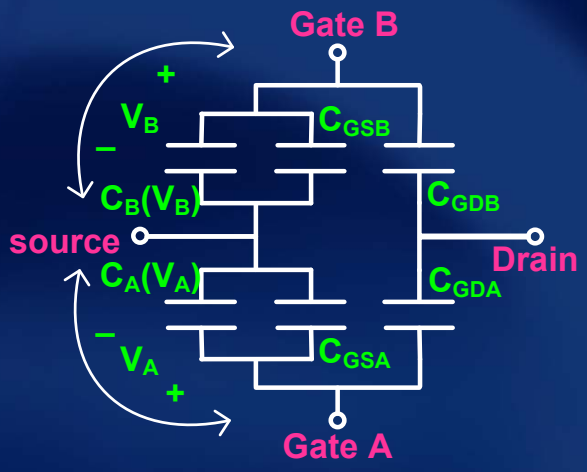


$Sum = (C_{in} \oplus (A \oplus B))$

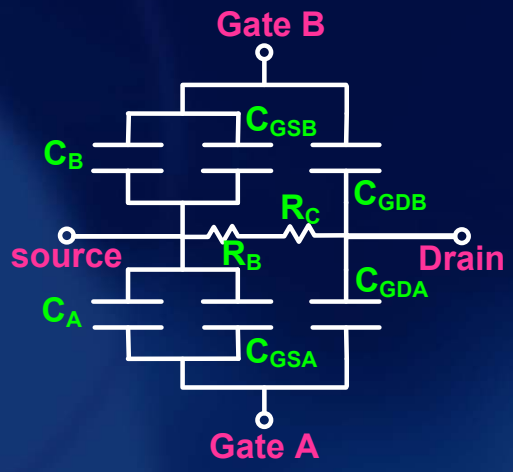


NEMS Device Models



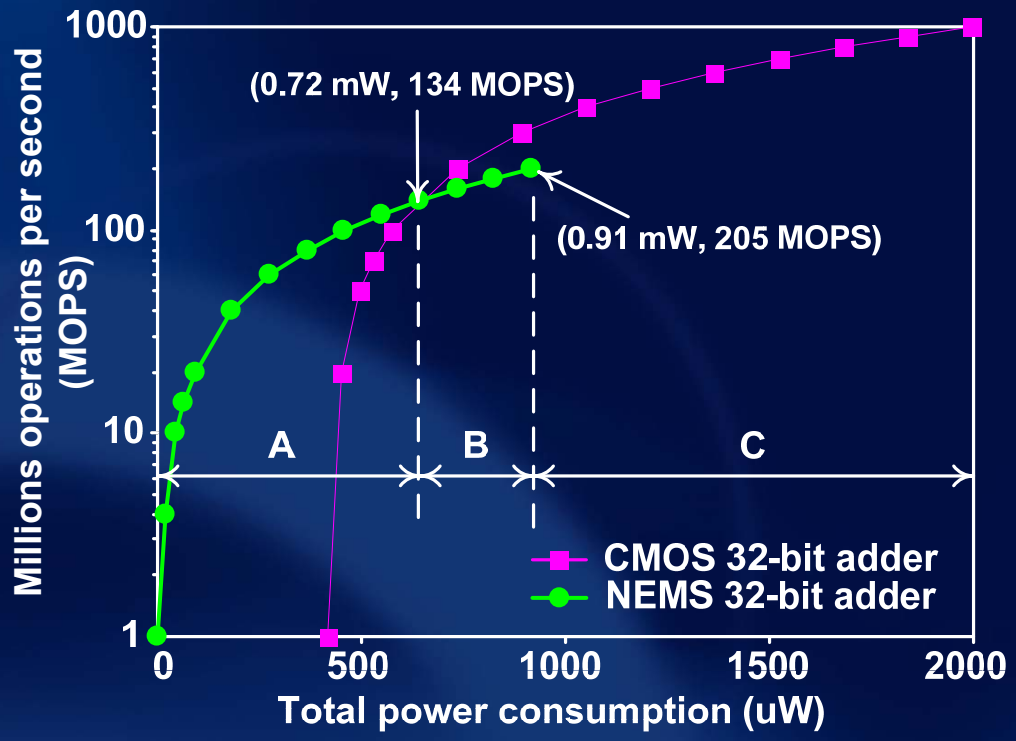


OFF state



ON state

Power-Performance Comparison



- **Power-performance comparison for 32-bit adders simulated using the NEMS device models and BPTM models for CMOS transistors**

Summary

- Compact NEMS-based XOR/XNOR gates are proposed
- The existence of compact XOR/XNOR gates makes it possible to used diagonal grouping of ‘1’s
- Some complex K-maps can be implemented in a more compact fashion using the diagonal grouping
- As an example, a full-adder is implemented using NEMS devices
- 32-bit NEMS- and CMOS-based adders are simulated for comparison