

ECE 225
High-Speed Digital IC Design
Lecture 14

3-D Integrated Circuits
....for Low-Power & More than Moore
Technologies

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Outline

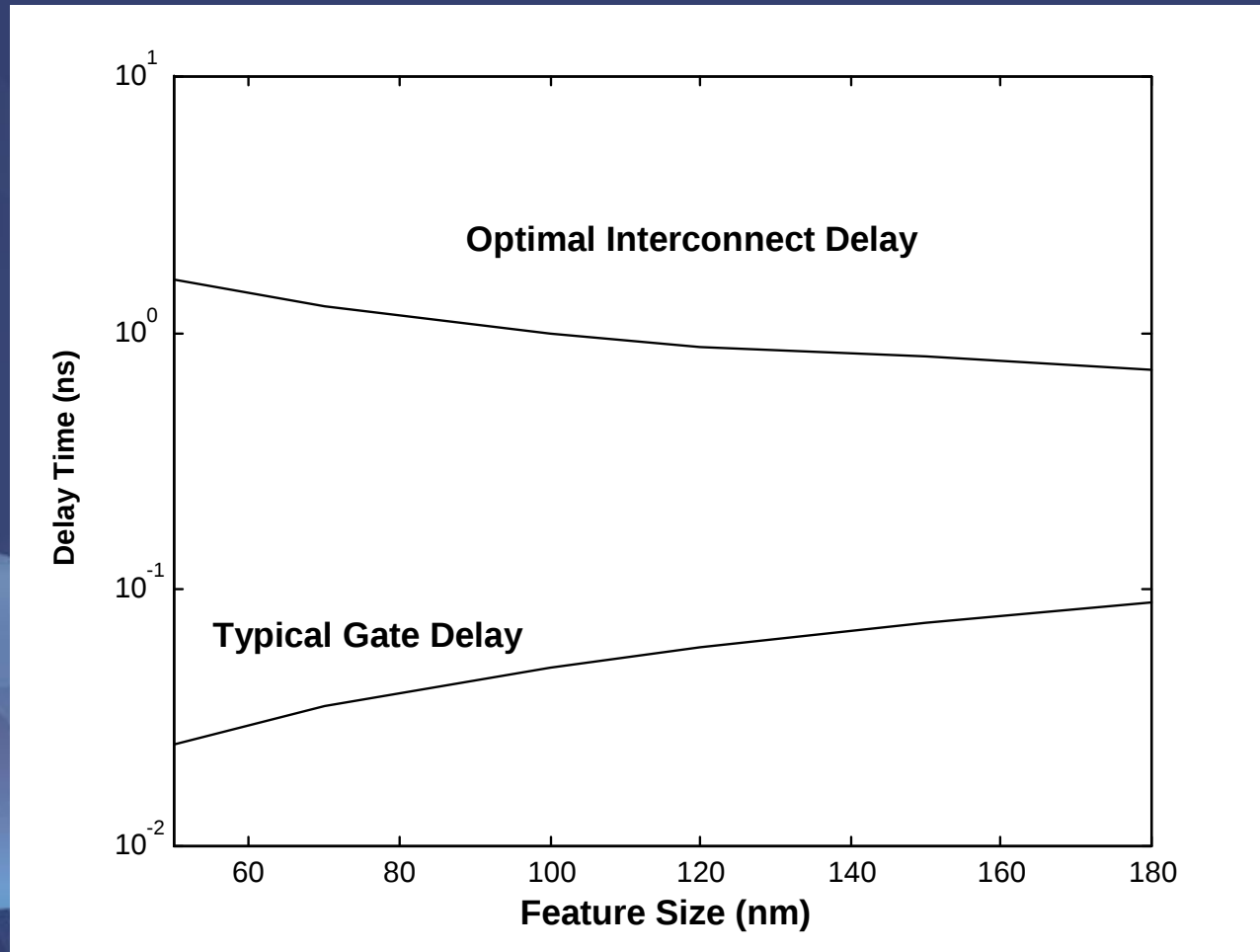
- Motivation for 3-D ICs
- Performance Analysis
- Thermal Analysis
- Technologies for 3-D ICs
- Applications
- Summary

Motivation for 3-D ICs

- Increasing Chip Size and Interconnect Delay
- Limitations of Cu/Low-k
- Limitations of Repeaters
- Effects on Design Process
- Heterogeneous Integration

Banerjee et al., Proceedings of the IEEE, May 2001

Interconnect Delay is Increasing (ITRS '99)



Will better materials like copper
and low-k dielectrics solve the
interconnect problem?

Low-k Dielectrics

IBM Says Process Can Make Chips More Powerful

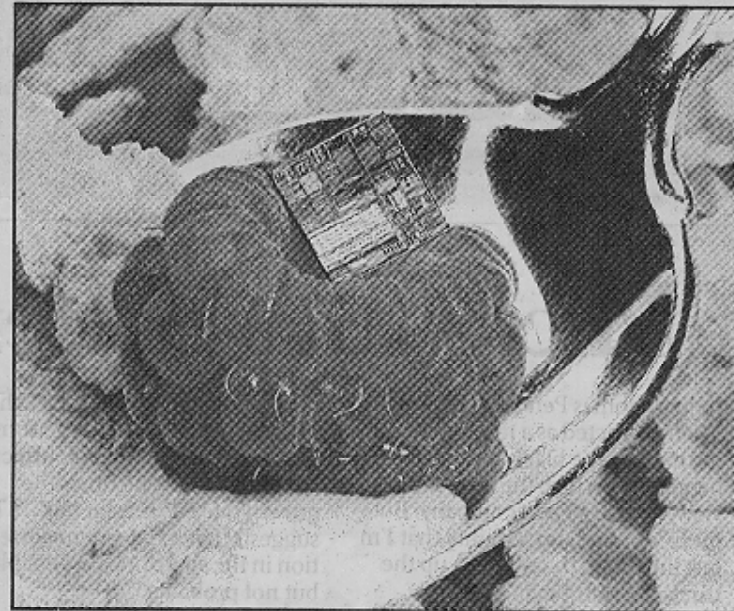
By Bruce Meyerson
ASSOCIATED PRESS

NEW YORK — IBM Corp. has developed a method for insulating the tiny circuits on a computer chip so they can be placed even closer together, making room for more computing power on each semiconductor.

The new process, which coats the circuits with a chemical polymer instead of silicon dioxide, can either improve a chip's processing speed by as much as 30 percent or halve the amount of power it uses, IBM said yesterday.

The insulation cuts down on magnetic interference, or "crosstalk," between the electrical pulses that travel along the millions of copper circuits that a chip uses to crunch data.

Because the electrical pulses are better shielded from the magnetic fields generated by neighboring pulses, the distance between circuits can be reduced by more than a



Associated Press

IBM said its new process for insulating circuits on small computer chips (such as this planted in a spoon of fruit and cereal for size comparison) should increase computing speed and performance by as much as 30 percent.

quarter to 0.13 microns — a measurement 600 times thinner than a human hair.

Thanks to the space savings, chipmakers can double the number of transistors they cram onto a piece of silicon to about 400 million, said Bijan Davari, a vice president of IBM's semiconductor research and develop-

ment center in East Fishkill, N.Y.

Chips made with the new insulation are expected to be available next year, IBM said.

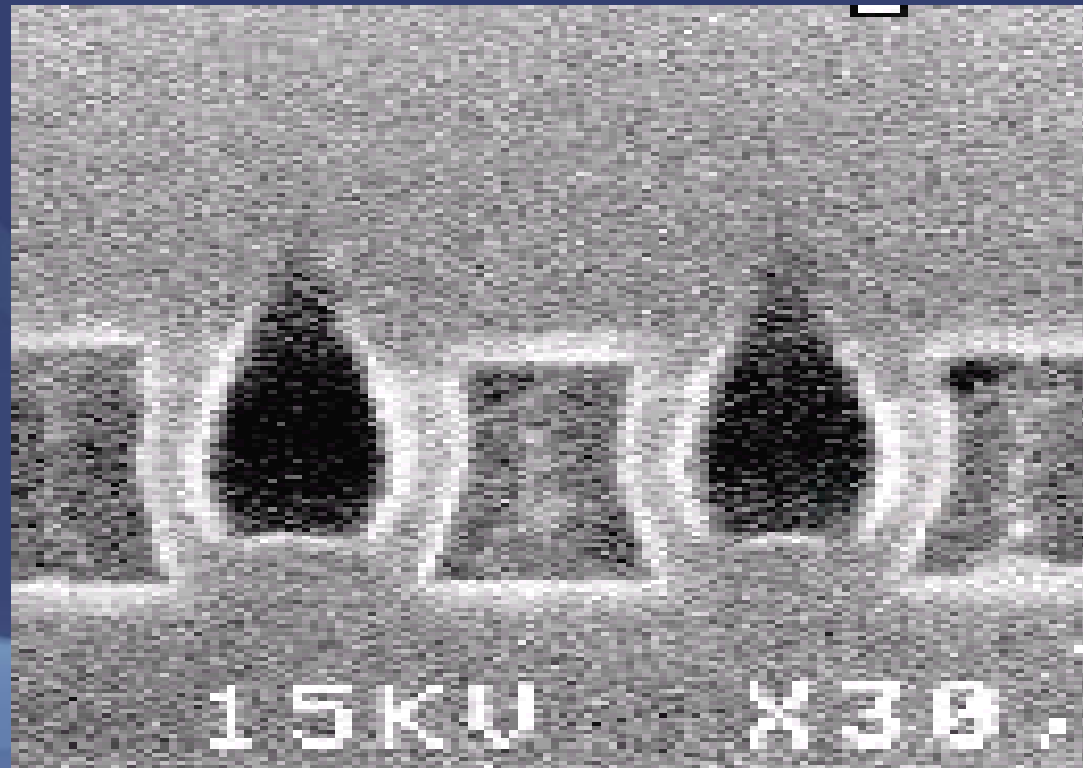
The first application will be to produce powerful microprocessors for major business systems like those used to run Web sites and communications networks.

Old dielectric SiO_2 $K = 4$

New dielectric Silk $K = 2.5$

The difference is not even a factor of 2!

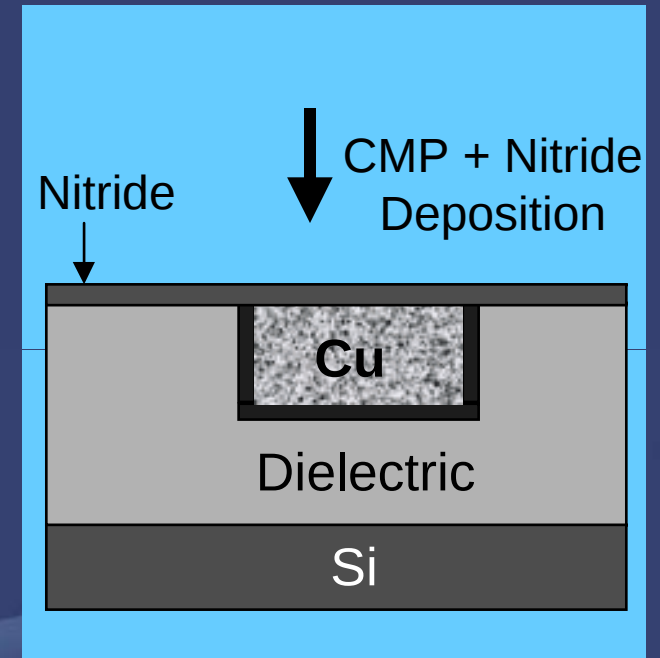
Limit of Low-k Dielectrics (Air: $K = 1$)



Air-Gap Interconnect Structure

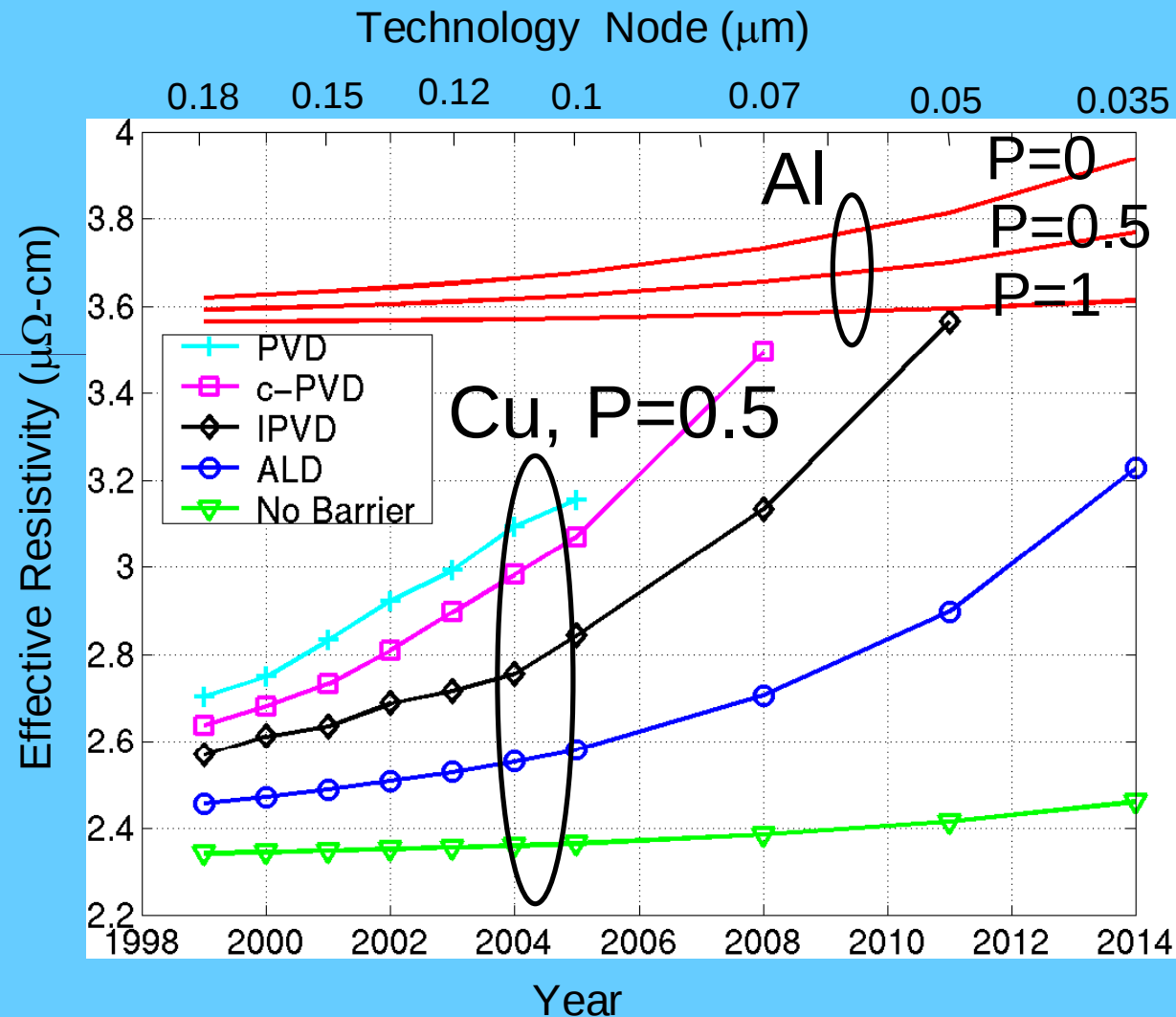
Cu Resistivity: Effect of Scaling

- Effect of Cu diffusion Barrier
 - Barriers have higher resistivity
 - Barriers can't be scaled below a minimum thickness
- Effect of Electron Scattering
 - e scattering from the surface
 - increases effective resistivity



Problem is worse than anticipated in the ITRS roadmap

Cu Resistivity: Effect of Scaling

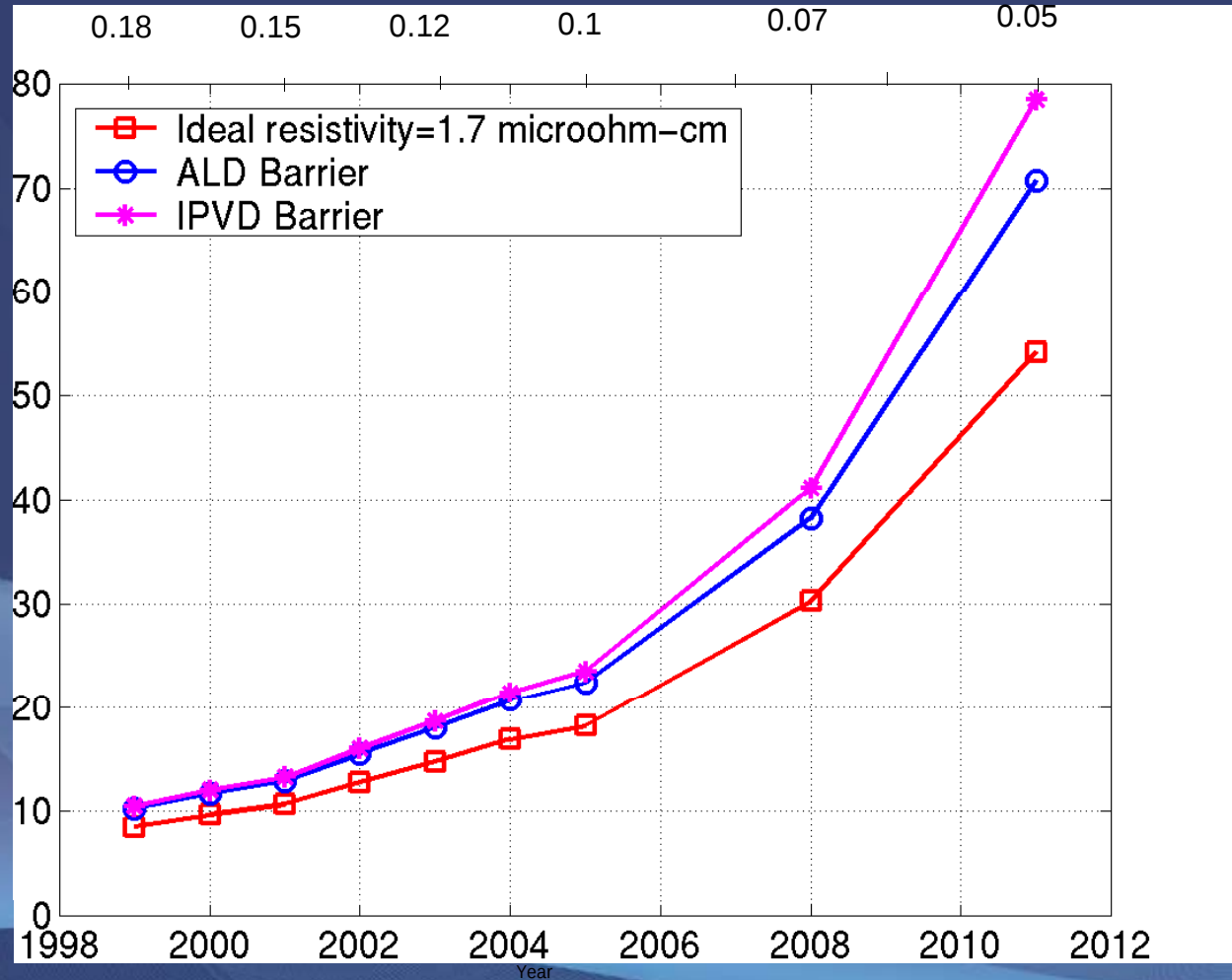


$T = 100^\circ\text{C}$

Cu Resistivity: Effect of Scaling

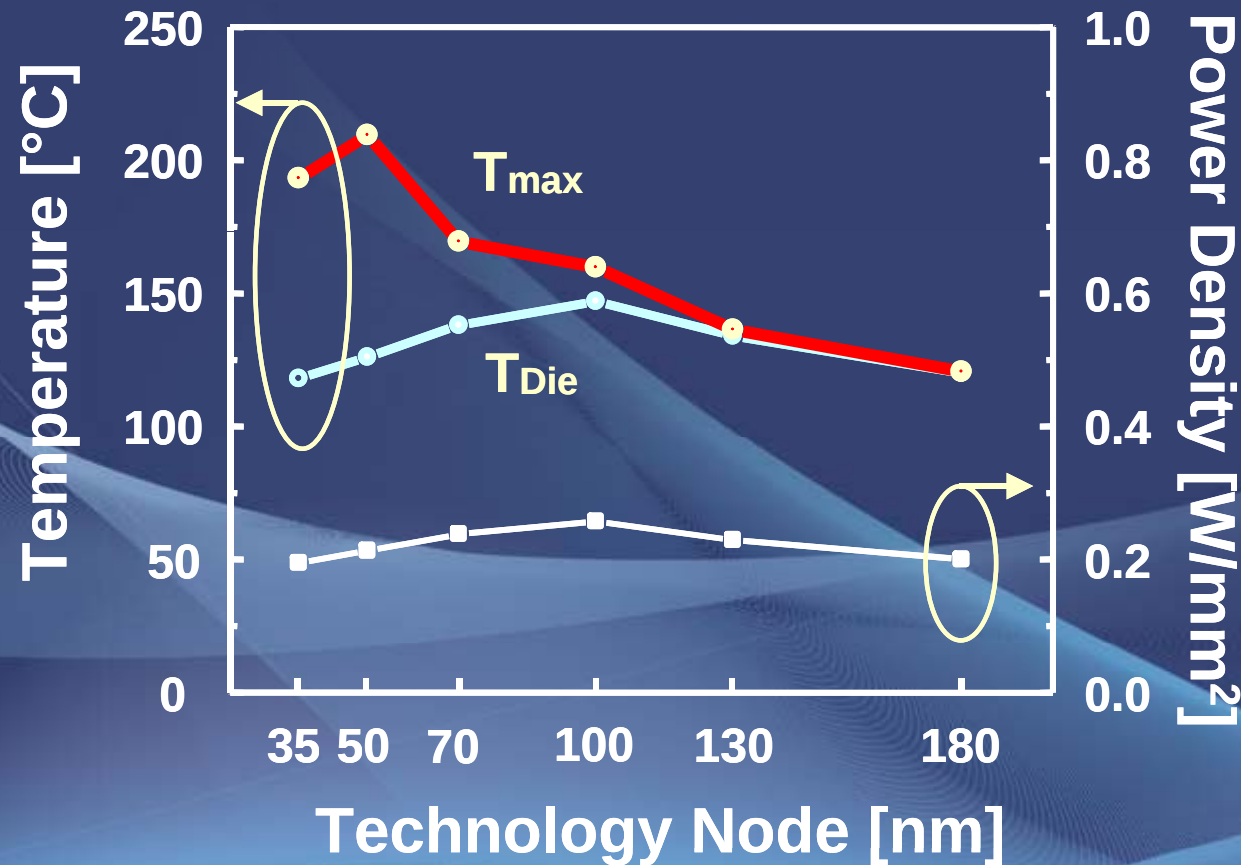
Technology Node (μm)

Repeaters per Longest Global Line



Scaling Effects: Maximum Chip Temperature

(IEDM 2000)

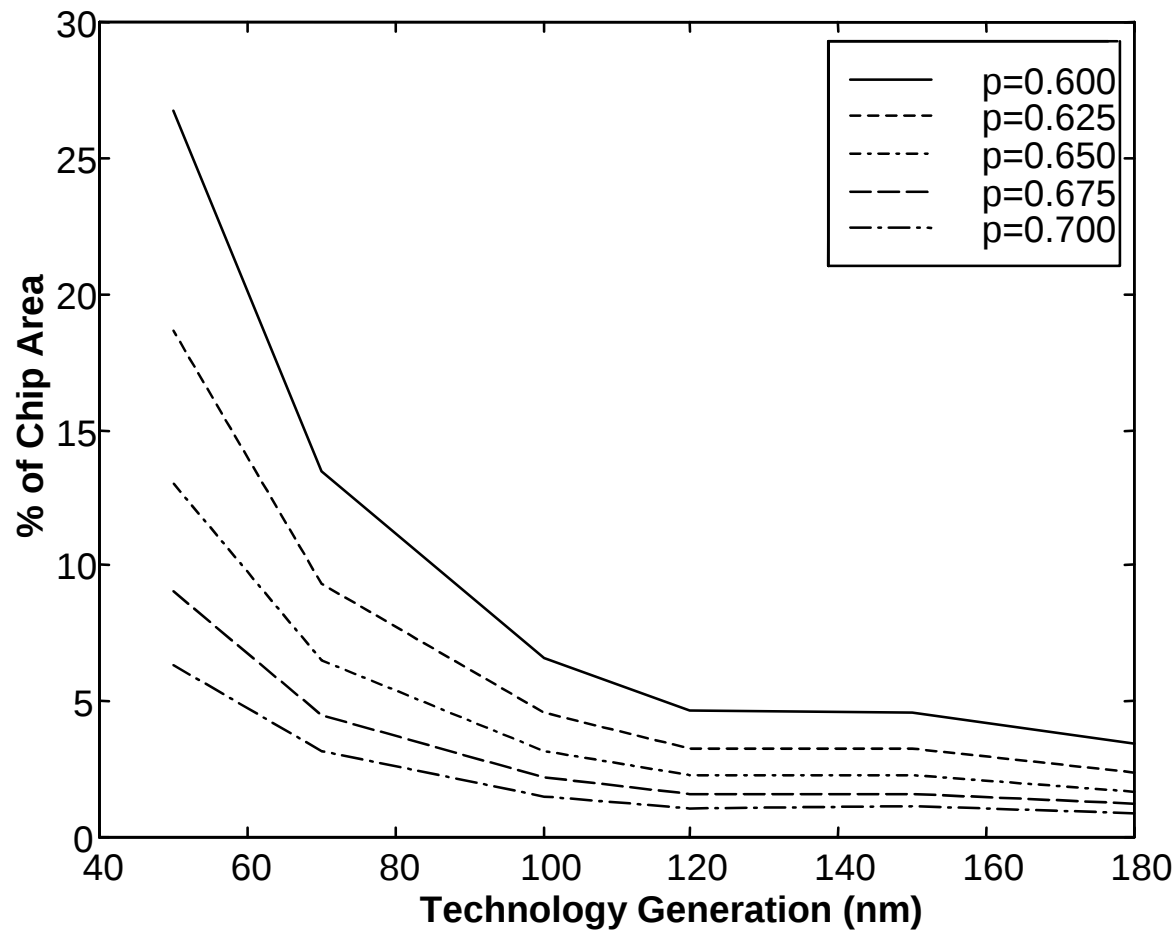


- Negligible Change in Power Density (ITRS '99)
- Increase in T_{max} Due to Joule Heating of Interconnects (FEM Simulation)

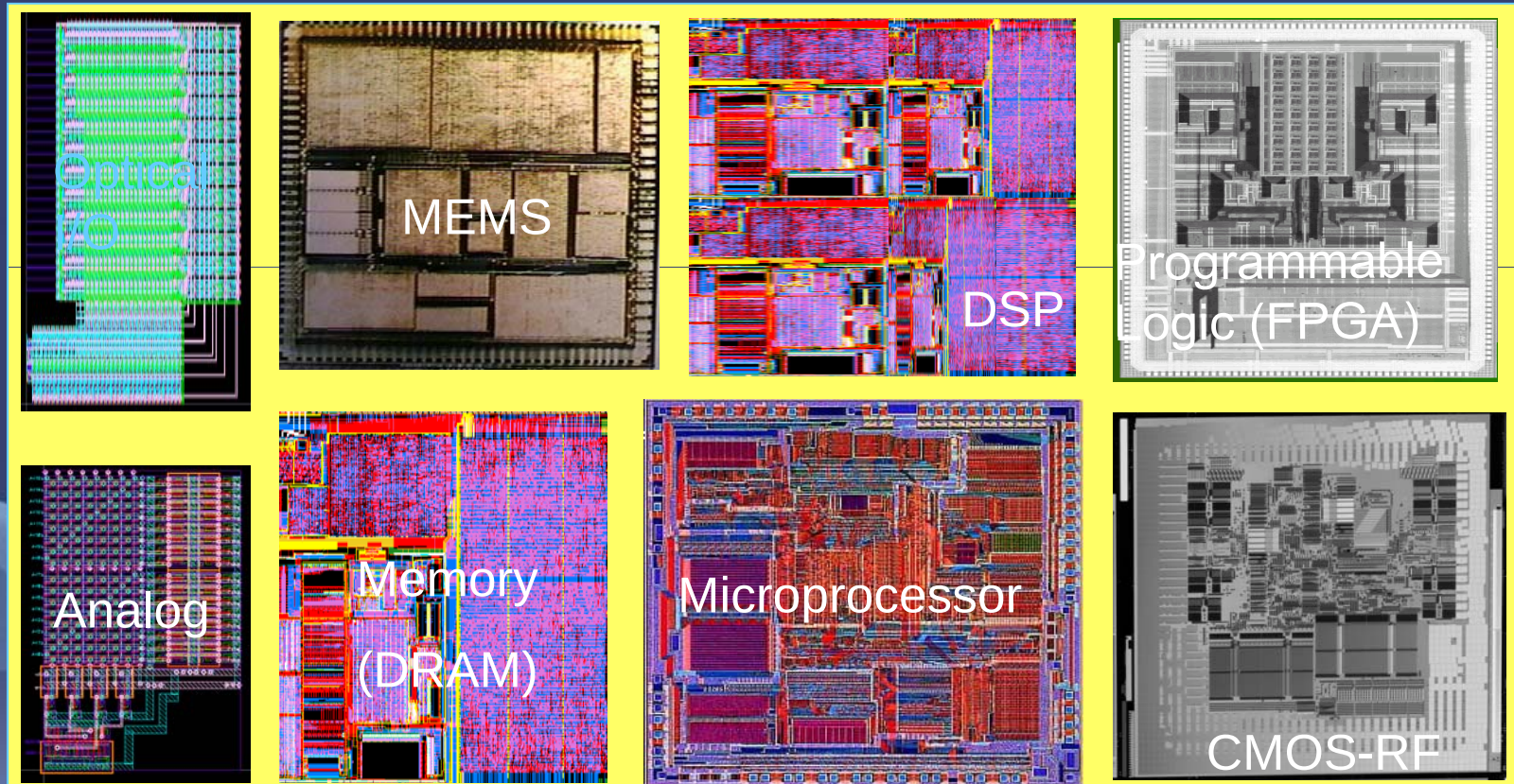
Effects on Design Process

- Increasing wire delay causes timing closure problem
- Prevents CAD methodologies to adopt higher levels of abstraction to simplify and accelerate the design process

Can we solve the problem by using more repeaters?

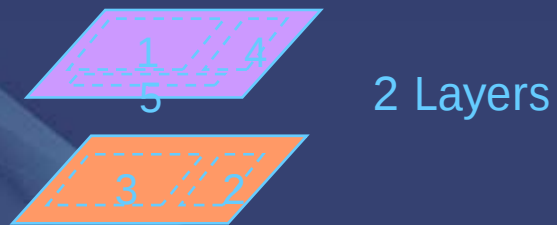
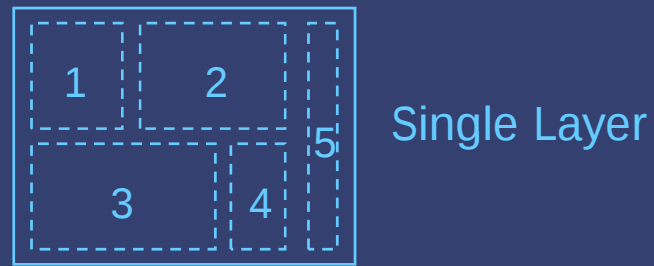


Integrated SoC to Sense, Process, and Collaborate



Difficult in Planar IC Technology

Novel Design Architectures Needed!



Replace horizontal by vertical
interconnect

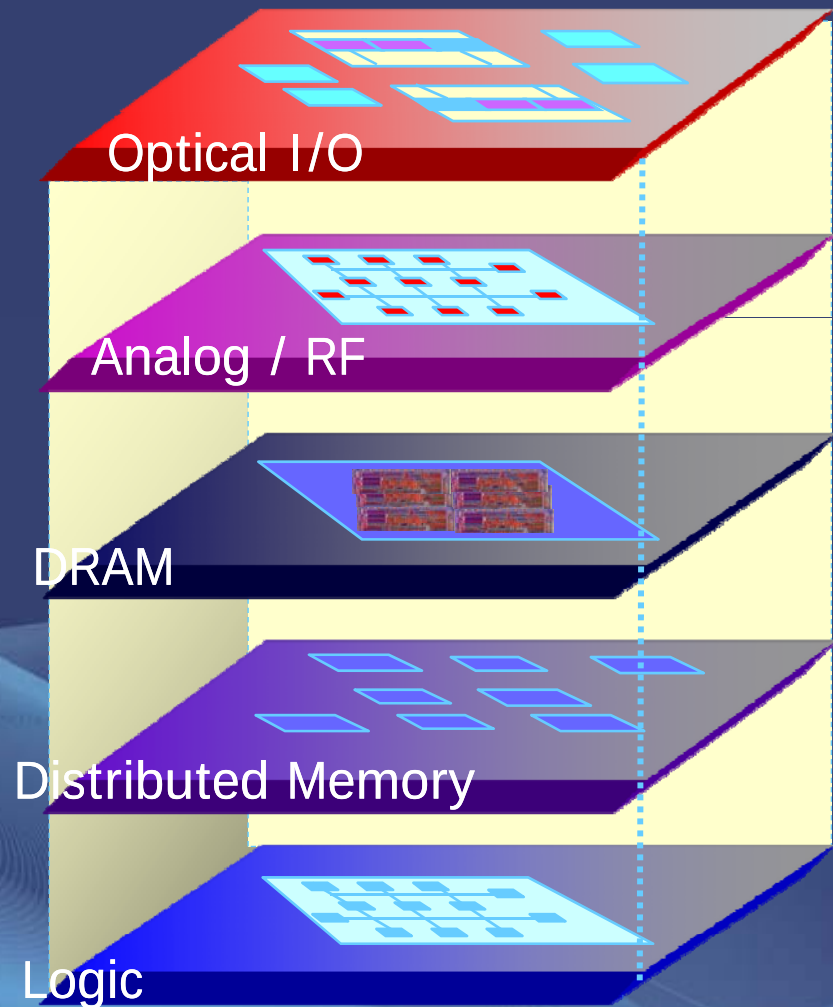
3-D ICs utilize the vertical dimension

3-D ICs : Multiple Active Si Layers

(Banerjee et al., Proc. IEEE 2001)

- **Advantages**

- Reduce Interconnect Length by Vertically Stacking Multiple Si Layers....**lower power**
- Improve Chip Performance
- Reduce **Chip Area**
- **Heterogeneous integration** possible, e.g., memory, digital, analog, optical, etc.



Performance Analysis Strategy

- Estimate Chip Area
- Estimate Interconnect Delay

Chip Area Determined from Wiring Requirement
Used 50 nm ITRS Data

Wire-Length Distribution

Calculate # of Interconnects of length 1

- Conservation of I/O's

$$T_A + T_B + T_C = T_{A\text{-to-}B} + T_{A\text{-to-}C} + T_{B\text{-to-}C} + T_{ABC}$$

$$T_A + T_B = T_{A\text{-to-}B} + T_{AB}$$

$$T_B + T_C = T_{B\text{-to-}C} + T_{BC}$$

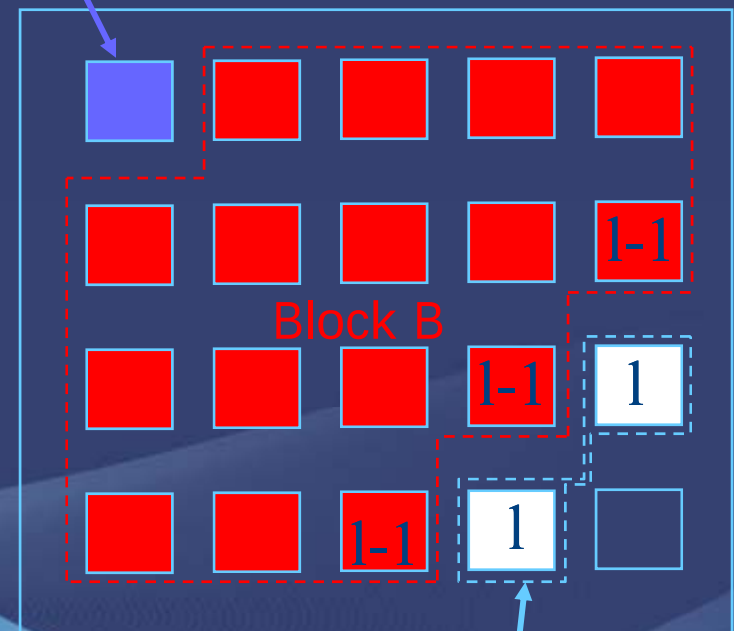
- Values of T within a block or collection of blocks are calculated using Rent's rule, e.g.,

$$T_A = k (N_A)^p$$

$$T_{ABC} = k (N_A + N_B + N_C)^p$$

- Recursive use of Rent's rule gives wire-length distribution for the whole chip

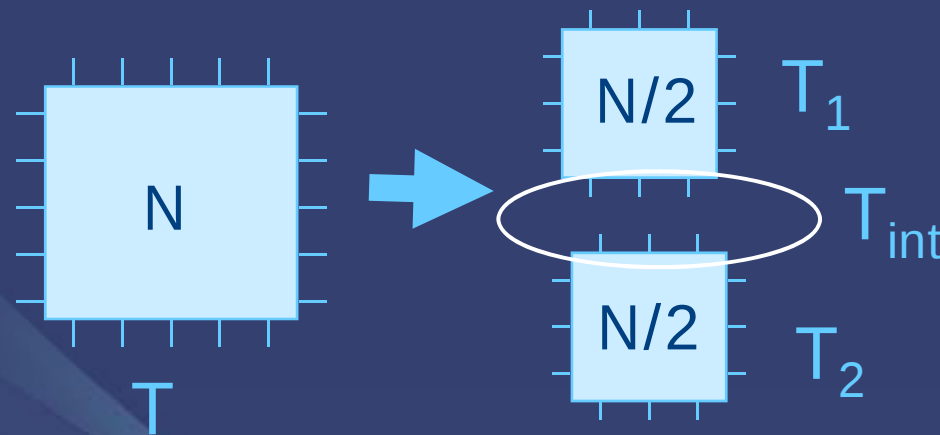
Block A with N_A gates



Block C

Rent's Rule: $T = k N^p$

Wire Length Distribution For 3-D ICs



- $T = k N^p = T_1 + T_2 - T_{int}$

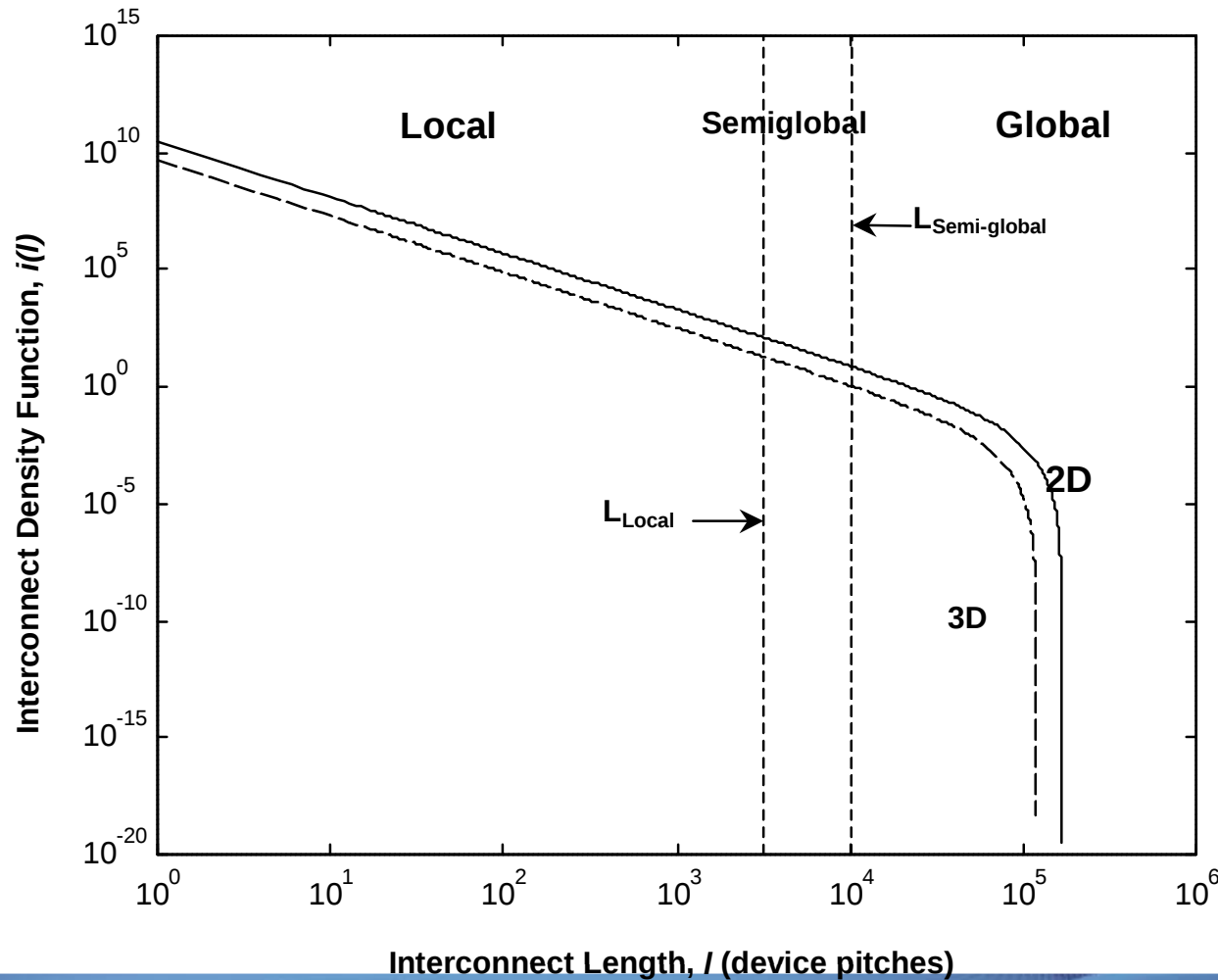
- $T_1 = T_2 = k (N/2)^p$

- $T_{ext, i} = T_i - T_{int}/2 = k 2^{p-1} (N/2)^p$

$$K_{eff, int} = k (1 - 2^{p-1})$$

$$K_{eff, ext} = k 2^{p-1}$$

Wire-Length Distribution

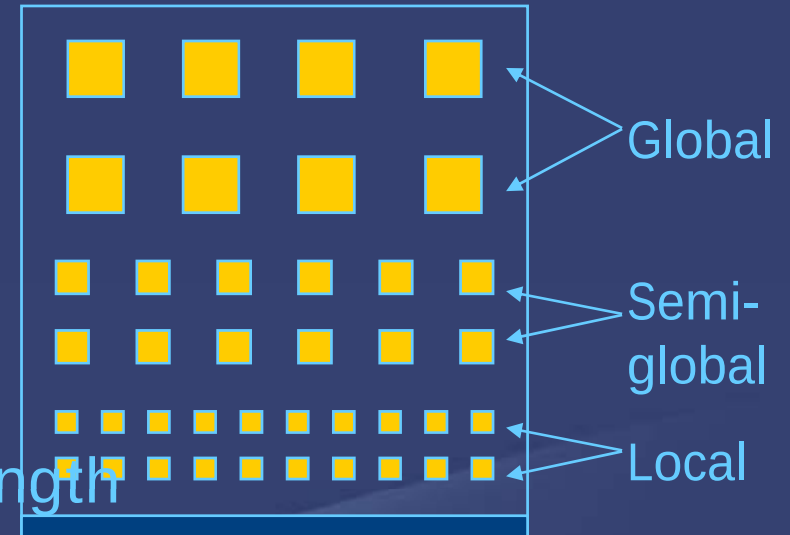


Vertical inter-layer connections reduce metal wiring requirement (50 nm ITRS)

Chip Area Estimation

- Placement of a wire in a tier is determined by some constraint, e.g., maximum allowed RC delay

A 3-tier wiring network



- Wiring Area = wire pitch x total length

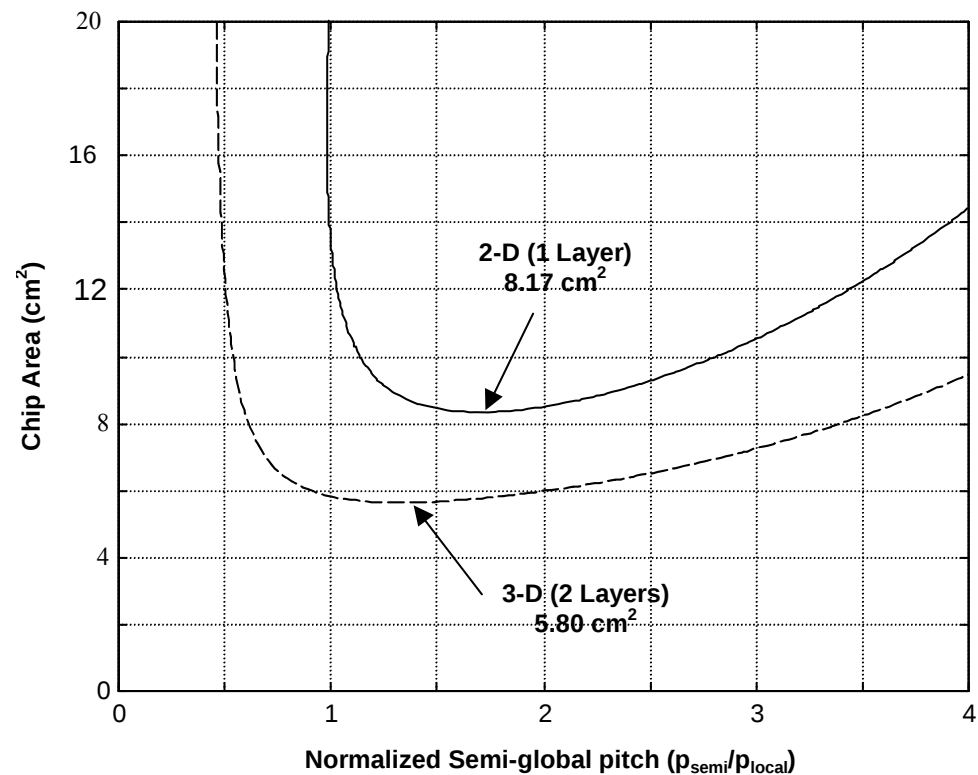
$$A_{\text{req}} = p_{\text{loc}} L_{\text{tot_loc}} + p_{\text{semi}} L_{\text{tot_semi}} + p_{\text{glob}} L_{\text{tot_glob}}$$

$$\text{Chip Area} = \frac{A_{\text{req}}}{\# \text{ of Metal Layers}}$$

- L_{tot} calculated from wire-length distribution

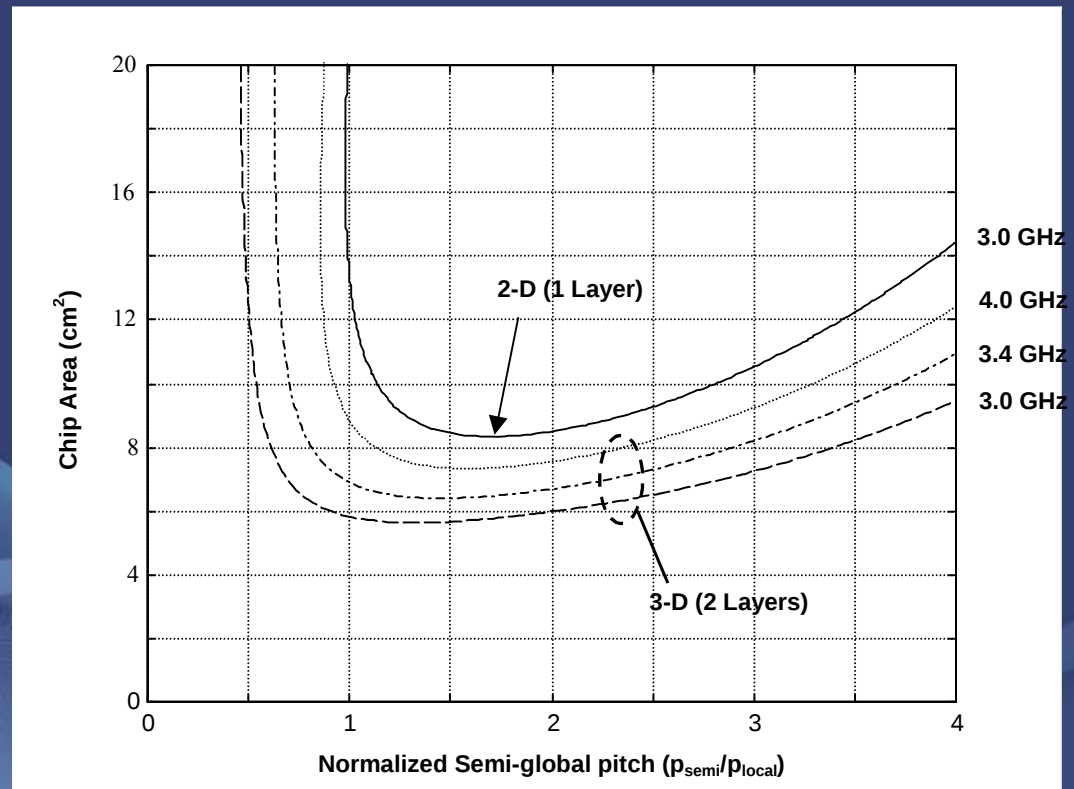
2 Active Layer Results

- constant chip frequency, f_c
- Less wiring needed
- Around 30% reduction in chip area

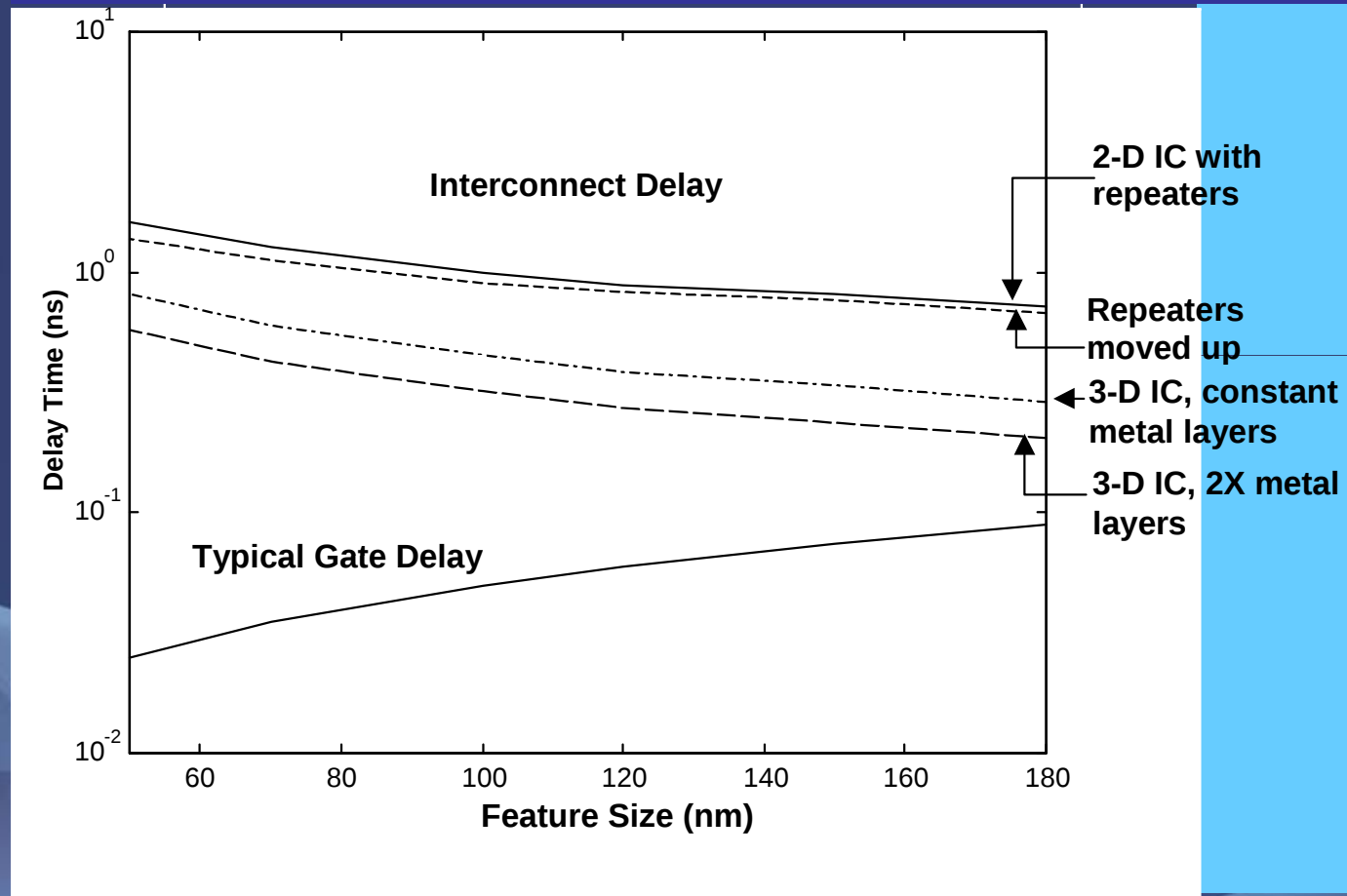


Improved Performance with Area

- Higher f_c obtained from larger wire pitch
- Results in increase in chip area
- Cannot increase f_c indefinitely



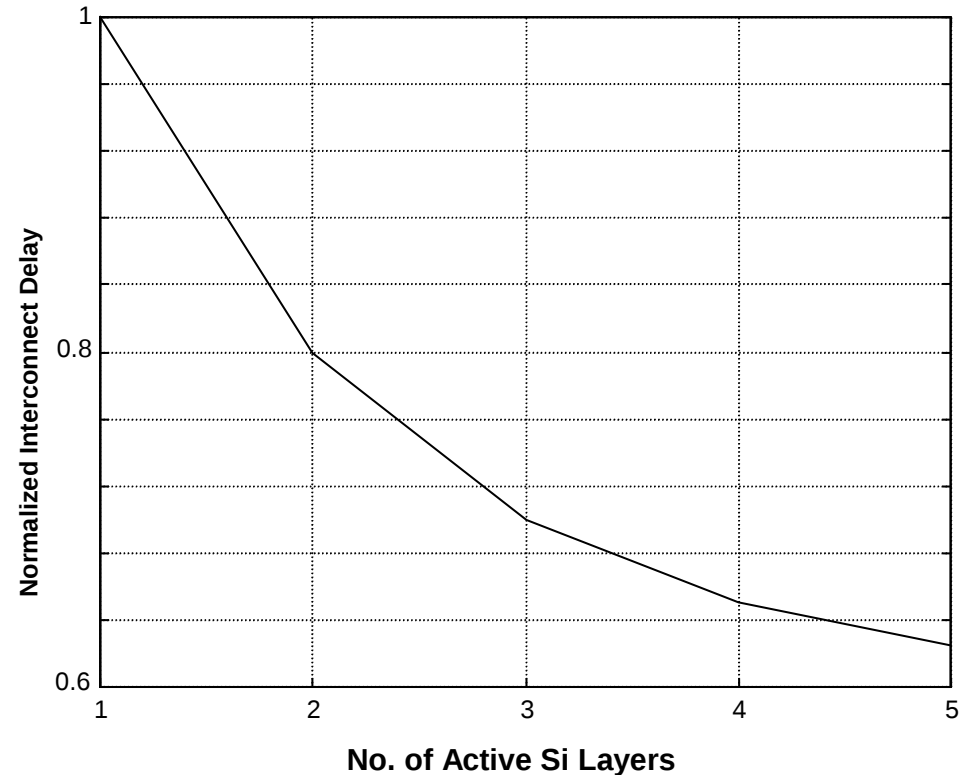
Performance Summary



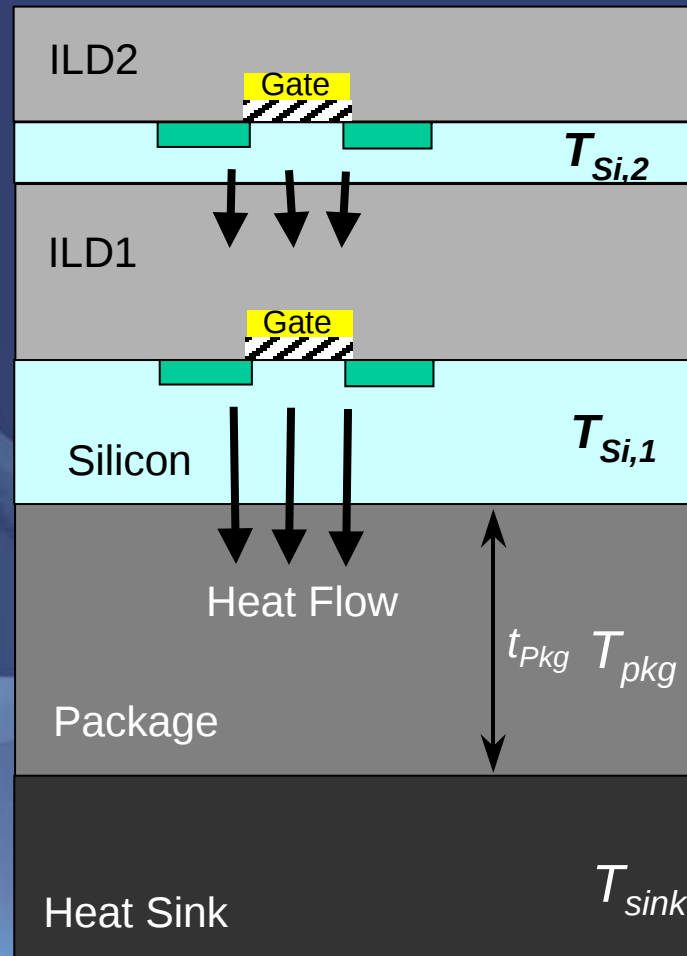
2-Layer 3-D Chip

More Than Two Active Layers

- Simulation based on data from ITRS (50 nm)
- Further improvement in delay achieved



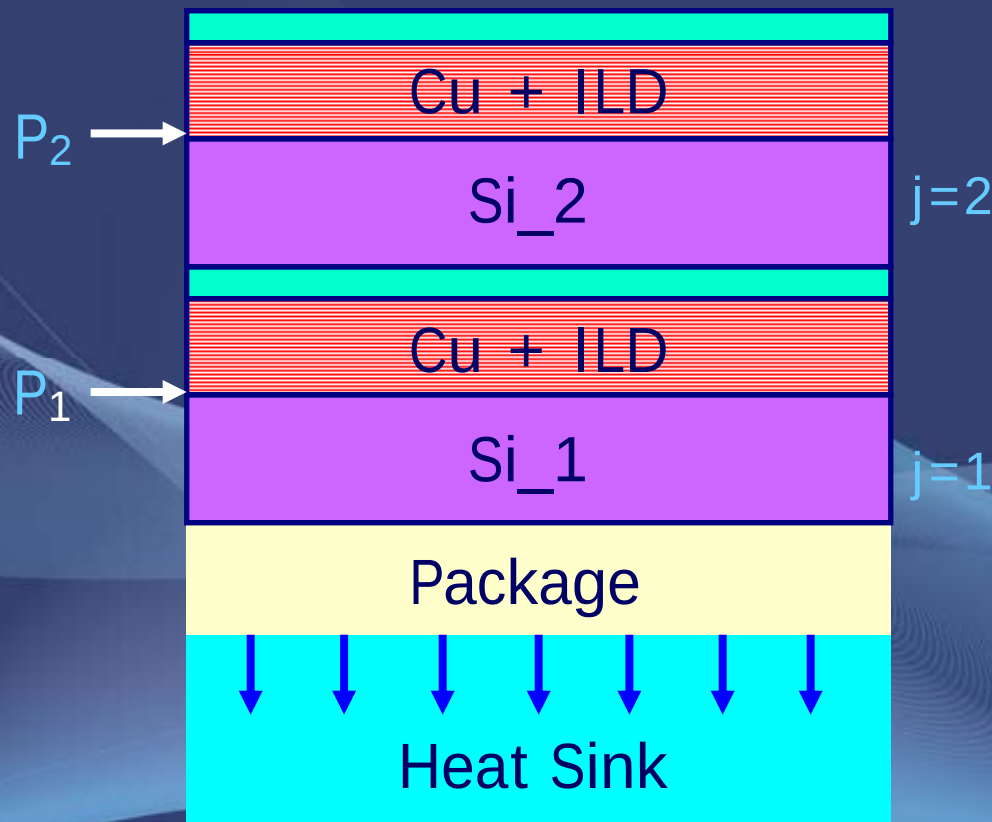
Thermal Issues



Analytical Die Temperature Model

(IEDM 2000)

- Temperature Rise of the j^{th} Active Layer in an n -layer 3-D Chip



$$\Delta T_j = \sum_{i=1}^j \left[R_i \left(\sum_{k=i}^n \frac{P_k}{A} \right) \right]$$

- n = Total Number of Active Layers
- R_i = Thermal Resistance Between Adjacent Layers
- P_k = Power Dissipation in the k^{th} Layer

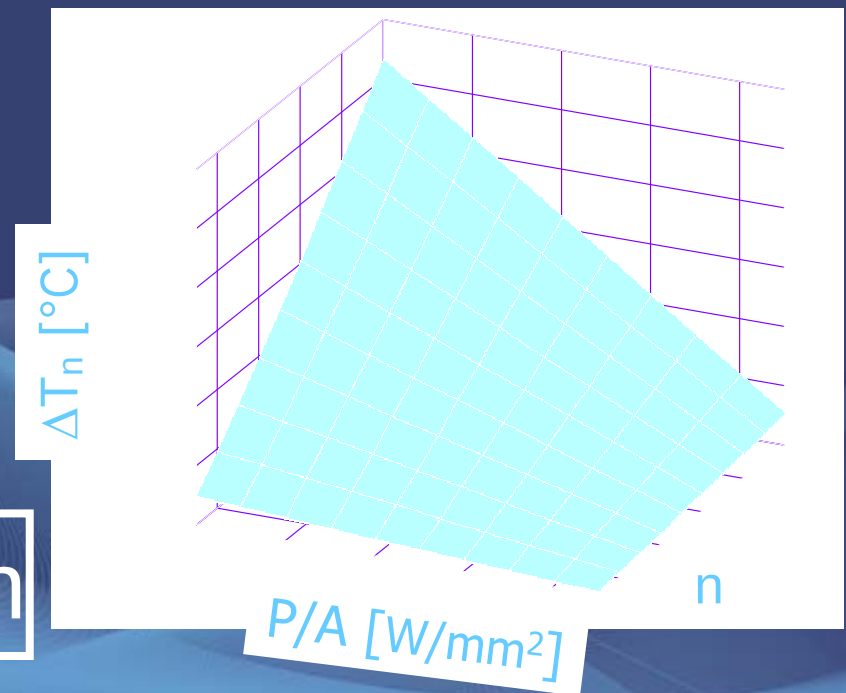
Analytical Die Temperature Model

Temperature Rise of the Uppermost (n^{th}) Layer
in an n -layer 3-D Chip

$$\Delta T_j = \sum_{i=1}^j \left[R_i \left(\sum_{k=i}^n \frac{P_k}{A} \right) \right] \longrightarrow \Delta T_n = \left(\frac{P}{A} \right) \left[\frac{R}{2} n^2 + \left(R_1 - \frac{R}{2} \right) n \right]$$

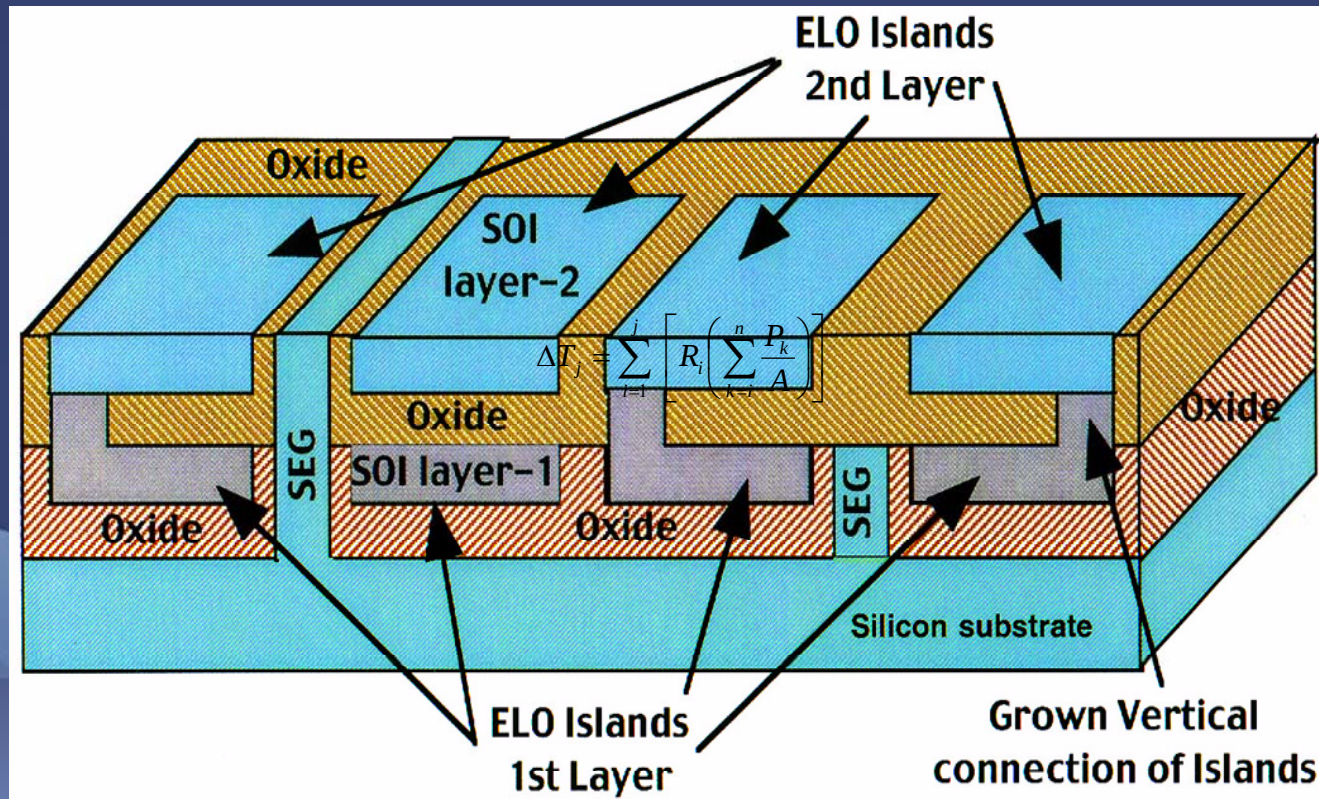
- R = Thermal Resistance Between Adjacent Layers
- R_1 = Package Thermal Resistance

• $R_1 \gg R$ $\xrightarrow{\text{Small } n}$ $\Delta T \propto n$



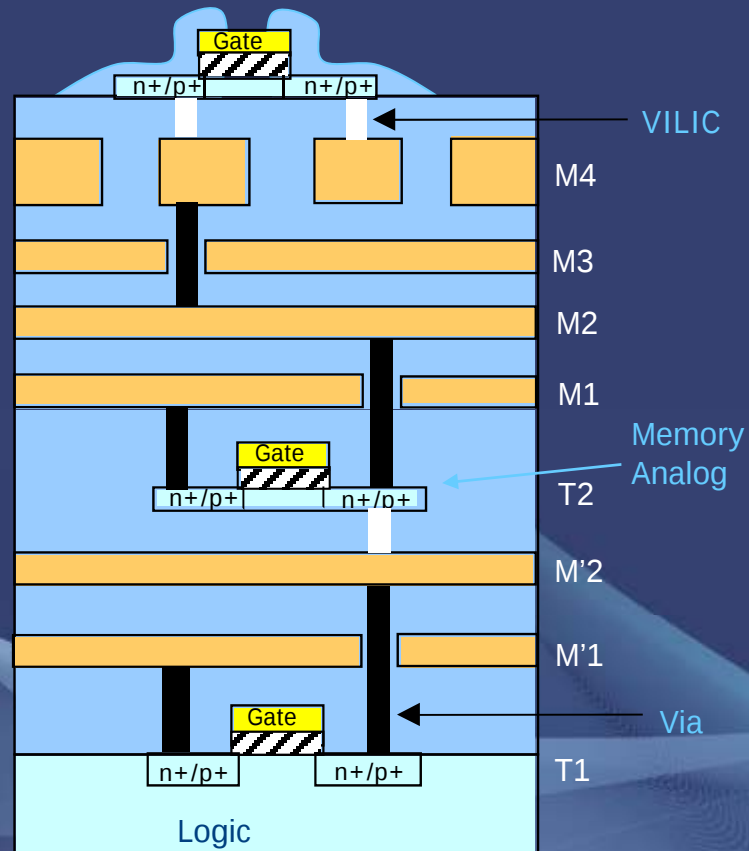
3-D Fabrication Technologies

Epitaxial Lateral Overgrowth

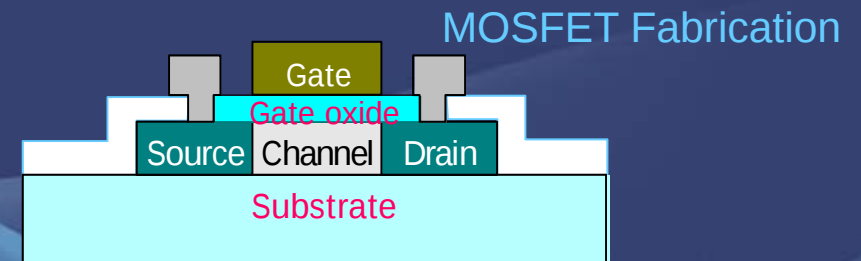
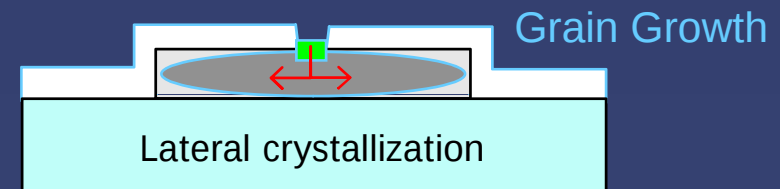
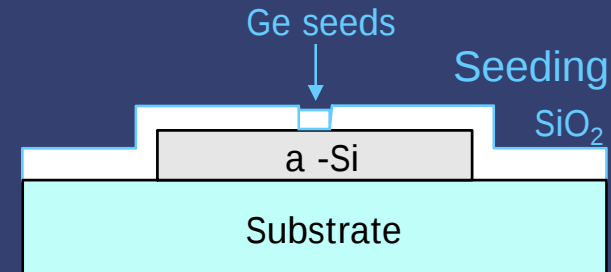


Purdue

3-D Fabrication Technologies



Solid Phase Crystallization of α -Si

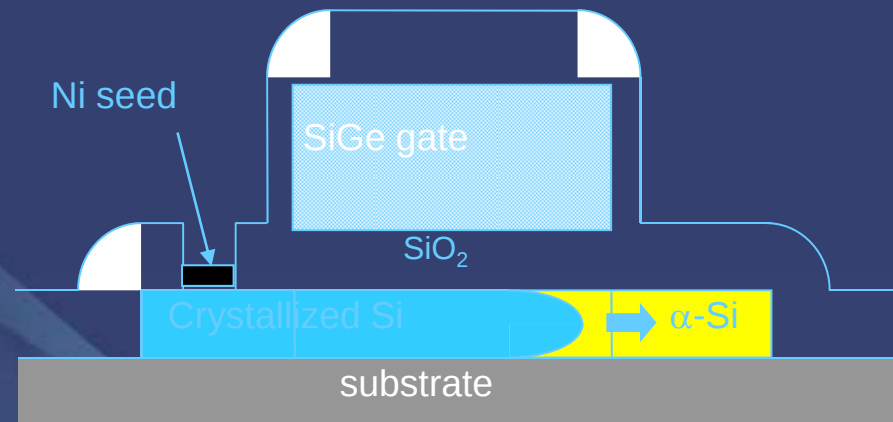


- Locally induce nucleation
- Grow laterally, inhibiting additional nucleation
- Build MOSFET in a single grain with SOI like performance

Stanford

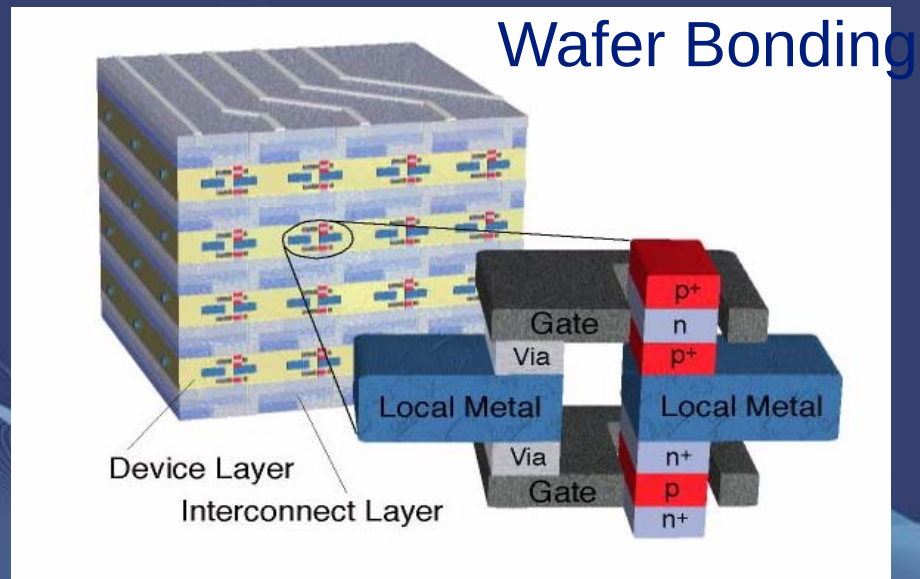
3-D Technologies

Ni Seeded Lateral Crystallization



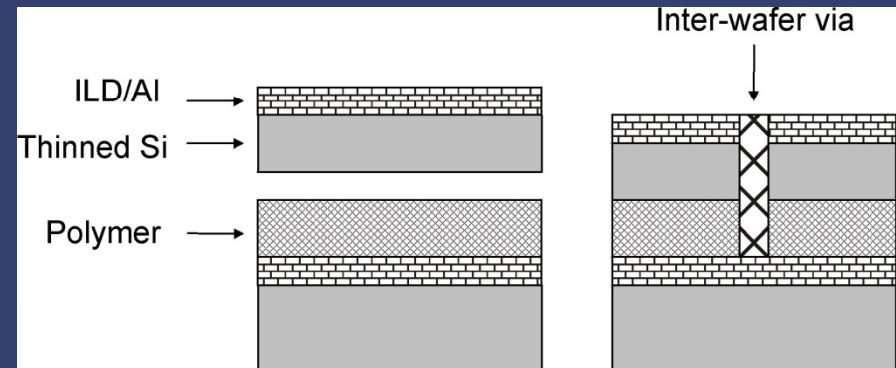
- Initially fabricate amorphous device
- Ni seeding for simultaneous crystallization and dopant activation
- Low thermal budget ($T_{\max} < 500^{\circ}\text{C}$)
- Devices on top of a metal line
 - MOSFETs
 - Optical detectors

3-D Fabrication Technologies

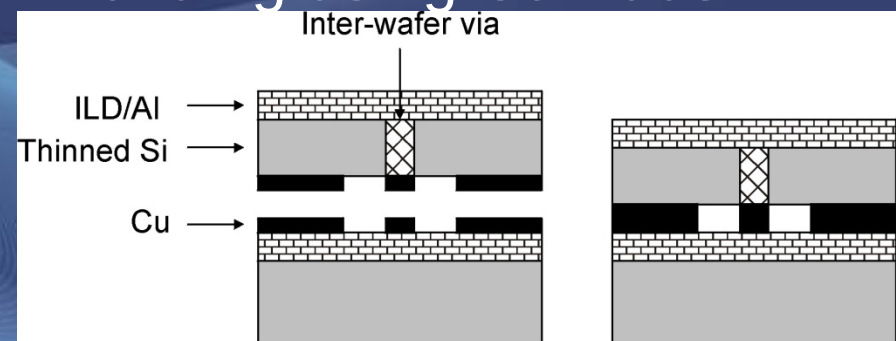


MIT

Bonding using Glue Layer



Thermocompression Bonding using Cu Pads



3D ICs: Implications for Circuit Design

- Critical Path Layout: By vertical stacking, the distance between logic blocks on the critical path can be reduced to improve circuit performance.
- Repeaters: Some chip area can be saved by placing repeaters ($\sim 10,000$ for high performance circuits) on the higher active layers.

3D ICs: Implications for Circuit Design

- Microprocessor Design: on-chip caches on the second active layer will reduce distance from the logic and computational blocks.

“3-D Shared Memory using Wafer Stacking”

K.W. Lee et al., (Tohoku Univ. Japan) IEDM 2000

- 3-D integration technology --wafer stacking
- Parallel processor system with three memory layers --multiport memory, overcomes bus bottleneck

3D ICs: Implications for Circuit Design

- Integration of Disparate Technologies Easier
- **RF and Mixed Signal ICs:** Substrate isolation between the digital and RF/analog components can be improved by dividing them among separate active layers - ideal for system on a chip design.
- **Optical Devices and I/Os** can be integrated on the top layer

3D ICs: Implications for Circuit Design

- **Neuromorphic Vision Chip:** Tohoku Univ.

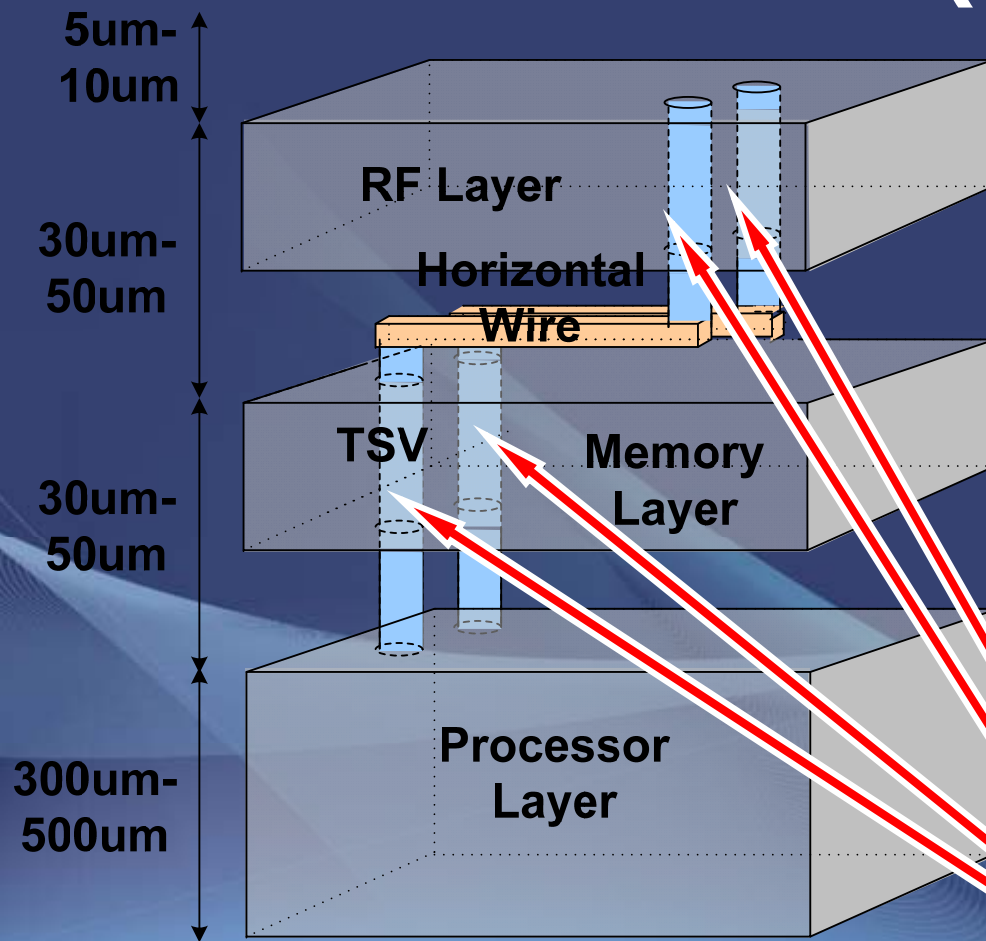
Achieved an image processing and pattern recognition system with parts of functions of the retina and visual cortex using Si

- **3-D Systems-on-a-Chip:** MIT, Lincoln Labs

3D ring oscillators and back-illuminated 64X64 active pixel sensor arrays with fully parallel A/D conversion

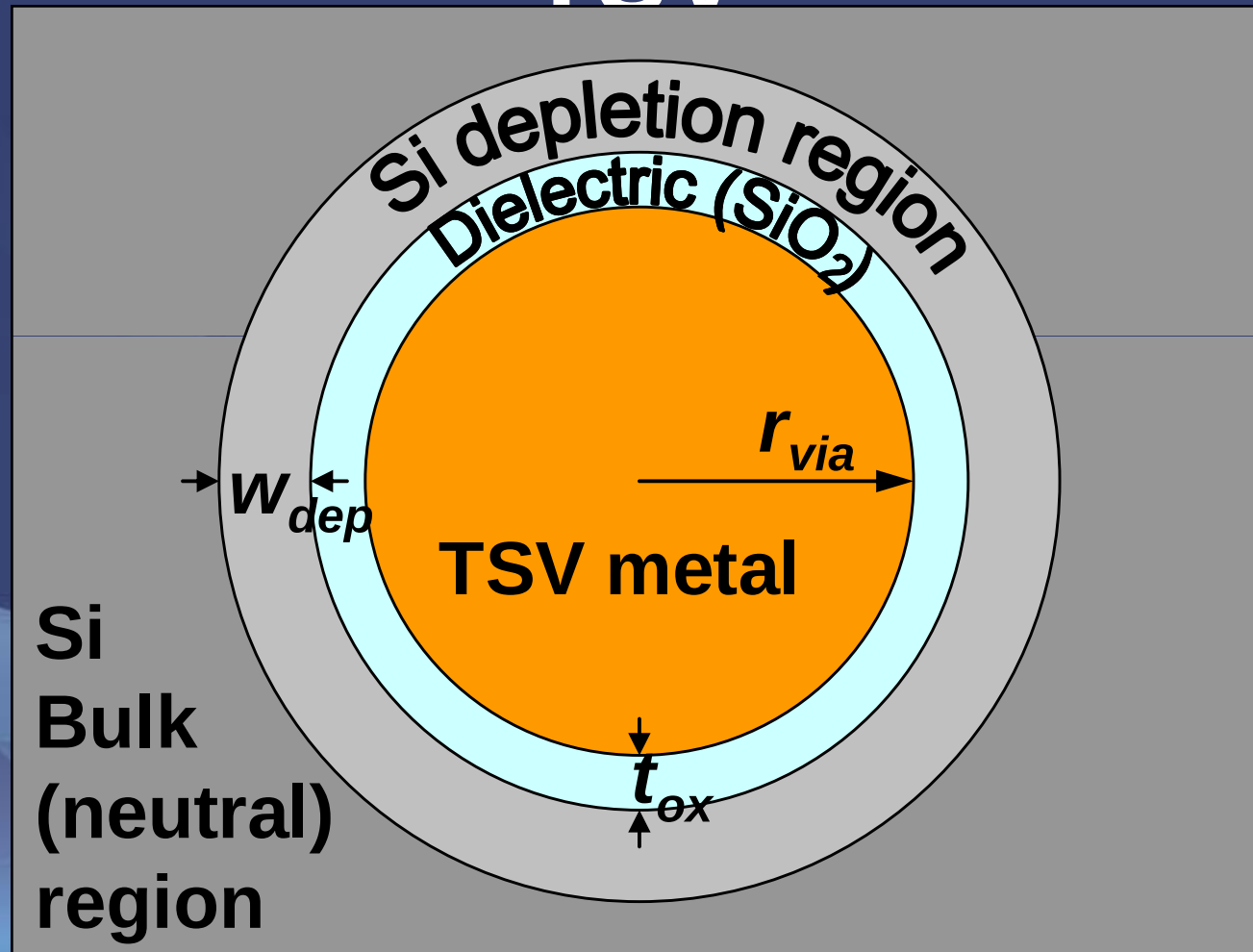
- **3-D Assembly Technology:** North Corp., Japan

Compact Modeling of Through-Si Vias (TSV)



- Increase functionality, performance and integration density...
 - “More-than-Moore” technologies
- TSVs – Connections between layers**

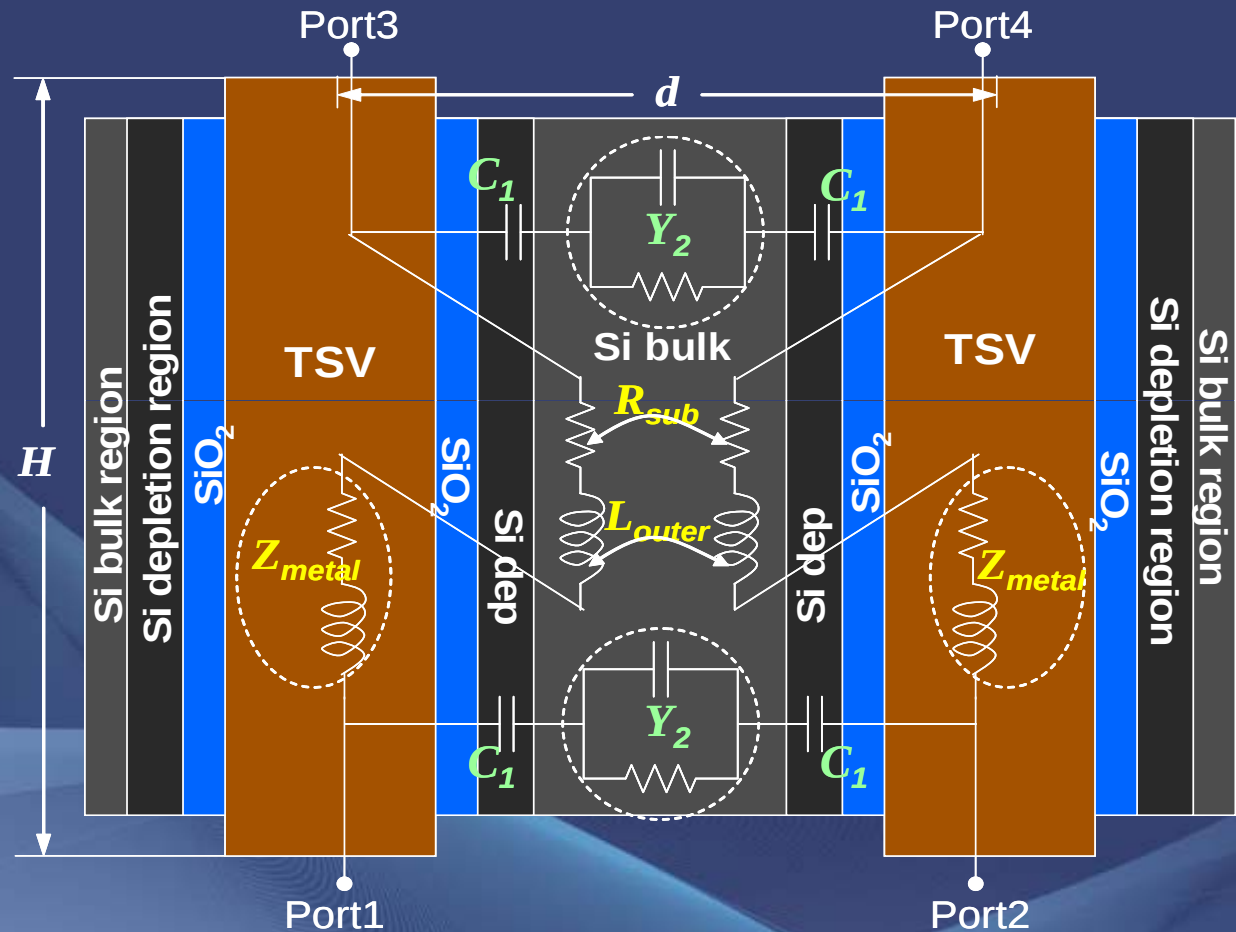
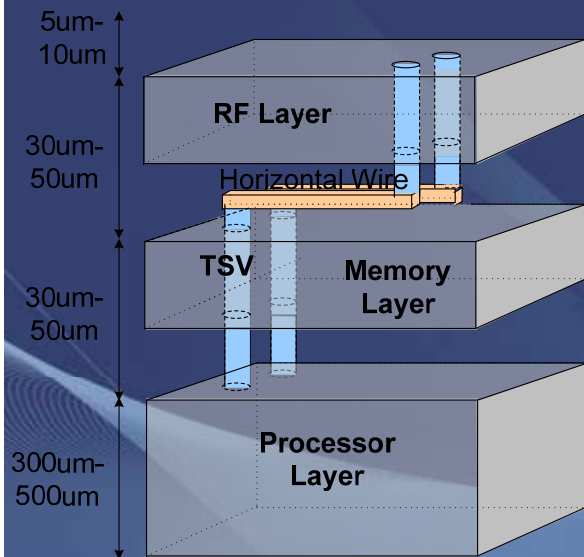
Top Cross-Sectional View of a TSV



Compact TSV Modeling for 3-D ICs

C. Xu, H. Li, R. Suaya and K. Banerjee, *IEDM*, 2009

- High aspect ratio (>10)
- Long lengths ($20\text{-}100\ \mu\text{m}$)

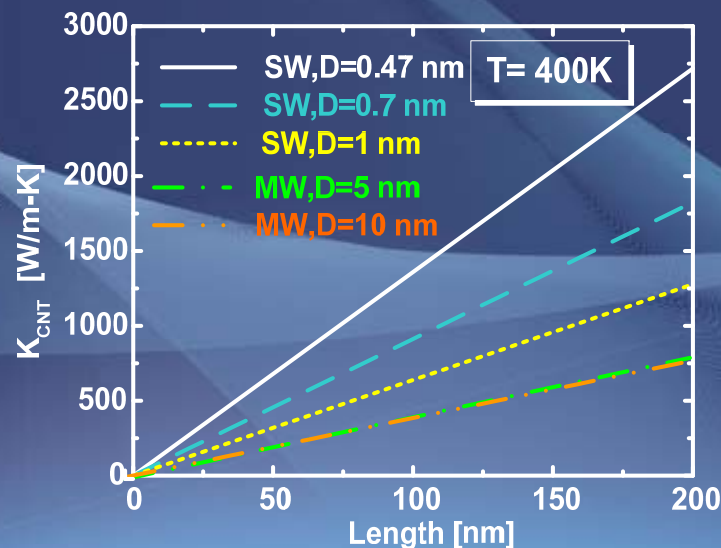


- RLGC transmission line model: with consideration of depletion region, AC conduction and eddy current effect
- C_1 accounts for the electrostatics, Y_2 accounts for the conductance and capacitance of bulk Si, Z_{metal} accounts for the inner impedance of the TSV-metal, L_{outer} and R_{sub} are due to the outer impedance of the TSV-pair

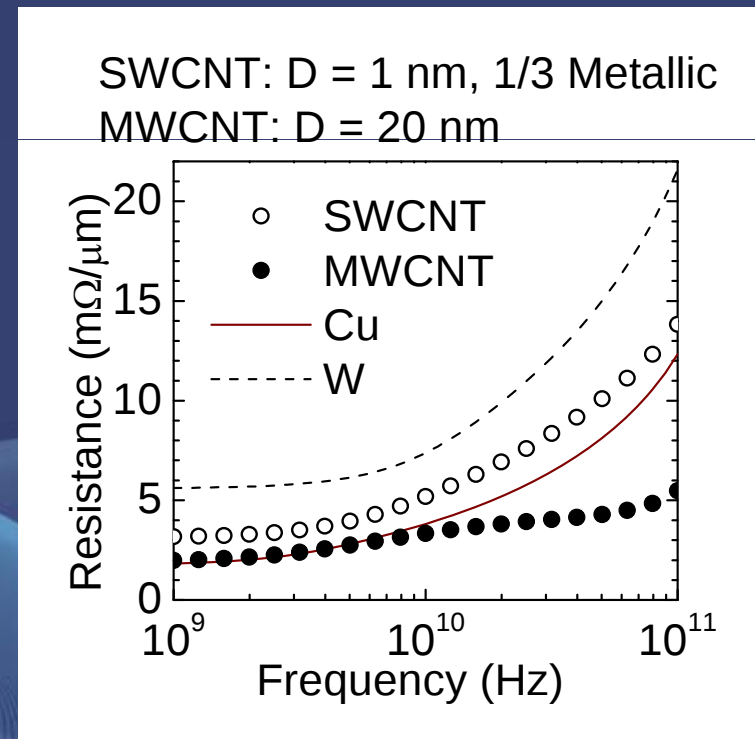
Carbon Nanotube based Through-Si-Vias for 3-D ICs

Why Carbon Nanotubes for TSVs?

- High electrical and thermal conductivity
- Large current carrying capacity
- Reduced skin effect
- Bottom-up growth—high aspect ratio



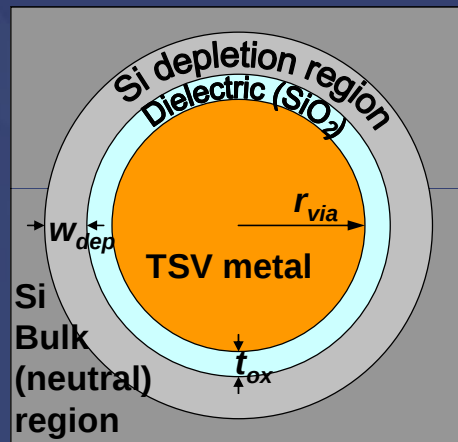
H. Li et al., *IEDM*, 2007



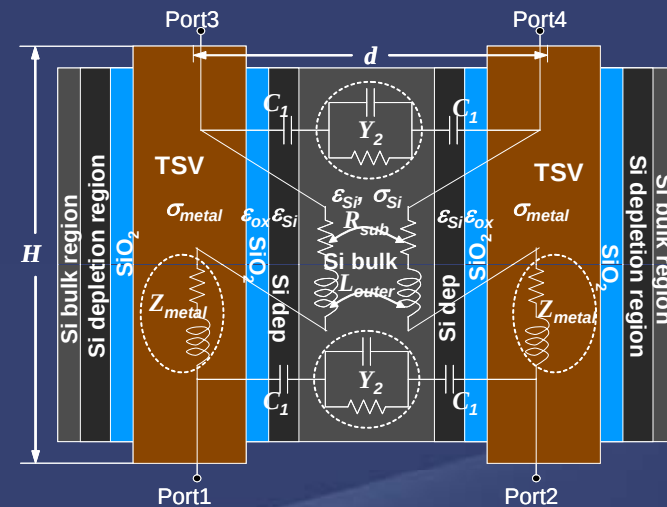
C. Xu et al., *IEDM*, 2009

Summary

Importance of MOS effect



RLGC compact model



Performance among TSV materials; possible application of MWCNTs; CG accuracy more important than RL accuracy

