ECE 225
High-Speed Digital IC Design

Lecture 15

Semiconductor Memories

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Semiconductor Memories

Memory Design...

- **Increasing number of transistors in processors are devoted to cache memories….more than 60%, see ITRS for more details…..**
- **At the system level: high-performance workstations and desktops have several Gbytes of memory**
- **Audio (MP3), Video players (MPEG4) and GPUs require large amount of memory**
- **Can we store Memory using registers? ….yes but the area required will be excessive (need > 10 transistors/bit)**
- **Memory cells are therefore combined into large arrays, which minimizes the overhead caused by the peripheral circuits and increases storage density**
- **Memory design can be classified as high-performance, high density, low-power circuit design**

Memory Classification

- Size
- Timing Parameters
- Function
- Access Pattern

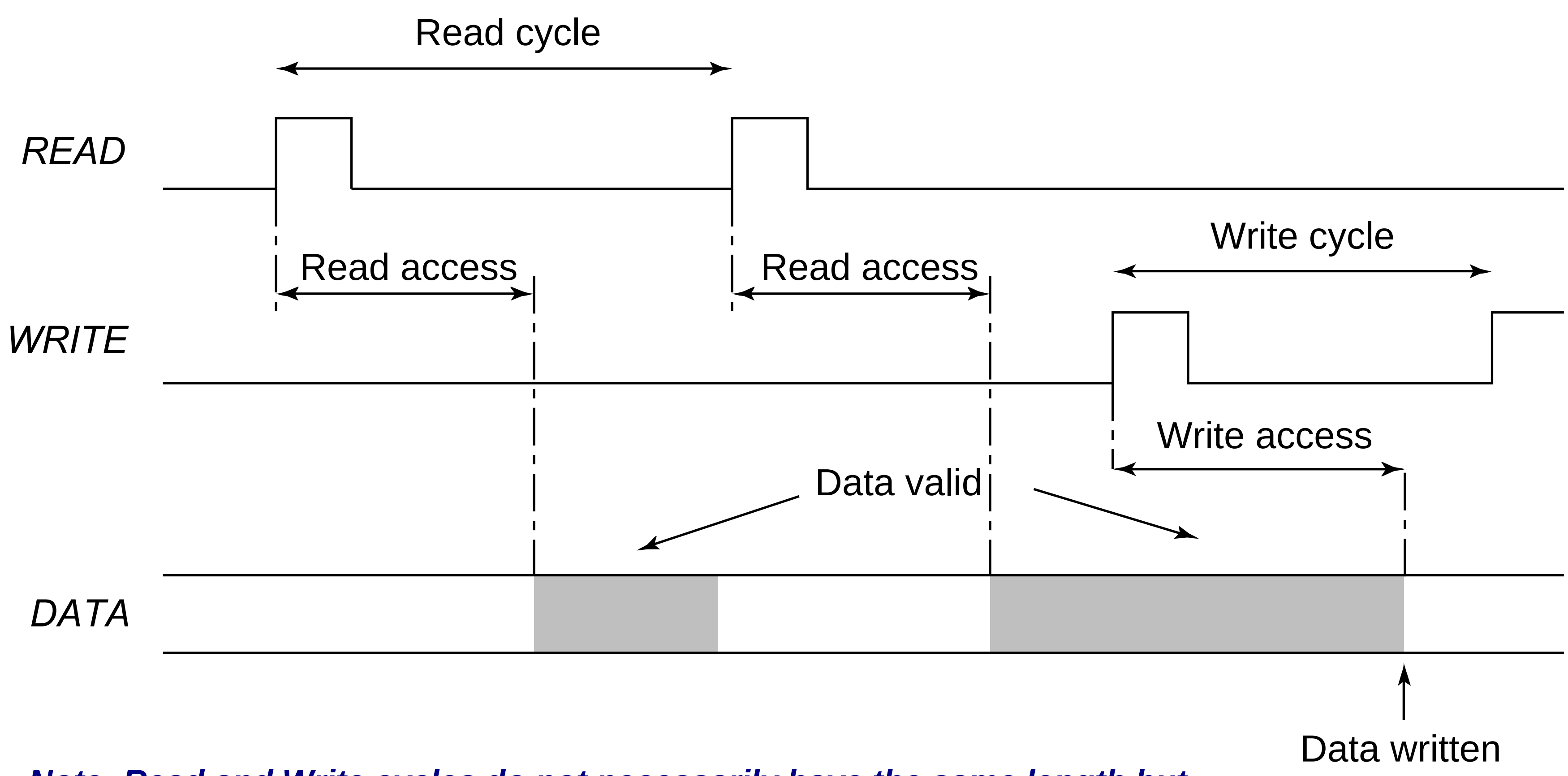
Memory Size

- Depends on the level of abstraction
- **Bits**: (used by circuit designers) are equivalent to the number of individual cells (FFs or Registers) to store data
- **Bytes**: (used by chip designers) are groups of 8 or 9 bits or their multiples: Kbyte, Mbyte, Gbyte, Tbyte
- **Words**: (used by system designers) represent a basic computational entity. For example, a group of 32 bits represent a word in a computer that operates on 32 bit data

Timing Parameters

- **READ-Access Time**: time it takes to retrieve (read) from the memory. This is equal to the delay between the read request and the moment the data becomes available at the O/P.
- **WRITE-Access Time**: time elapsed between a write request and the final writing of the input data into the memory
- **CYCLE Time**: minimum time required between successive reads or writes

Memory Timing: Definitions



Note: Read and Write cycles do not necessarily have the same length but are considered to be equal for simplicity of system design.

Function

- **Read-Only Memory (ROM)**:
  - encode the information into the circuit topology-by removing or adding transistors. The topology is hard wired and the data cannot be modified….can only be read.
  - They belong to the class of **Non-volatile** memories. Disconnection of the supply voltage does not result in a loss of the stored data.
- **Read-Write Memories (RWM)**: called as **RAM** (Random-Access Memories).
  - **Static** (retains data if Vdd is retained): example SRAM
  - **Dynamic** (needs periodic refreshing): example DRAM
  - They use active circuitry to store information and belong to the class of **Volatile** memories.

Function….cont'd

- **Non-Volatile Read-Write (NVRWM):**
  - Recent Non-Volatile Memories can read and write----although write function is substantially slower
  - Novel, cheap and dense: Fastest growing among semiconductor memories
- Examples:
  - EPROM: Electrically Programmable ROM
  - E^2PROM: Electrically Erasable and Programmable ROM
  - Flash memory

Access Pattern

- **Random-Access (RAM):**
  - memory locations can be read or written in a random manner
  - Most ROMs and NVRWMs allow random access….but "RAM" is used for the RWMs only
- **Serial Access:**
  - Restricts the order of access. Results in faster access times, smaller area, or allows special functionality
  - Examples: (Video Memories)
    - FIFO (first-in first-out)
    - LIFO (last-in first-out)
    - Shift Register
- **Content-Addressable Memory (CAM):** (non-random access)
  - Also known as associative memory
  - Doesn't use an address to locate the data…..rather uses a word of data itself as input… when input data matches a data word stored in memory array, a MATCH flag is raised
  - Important component of the cache architecture of most microprocessors

Semiconductor Memory Classification

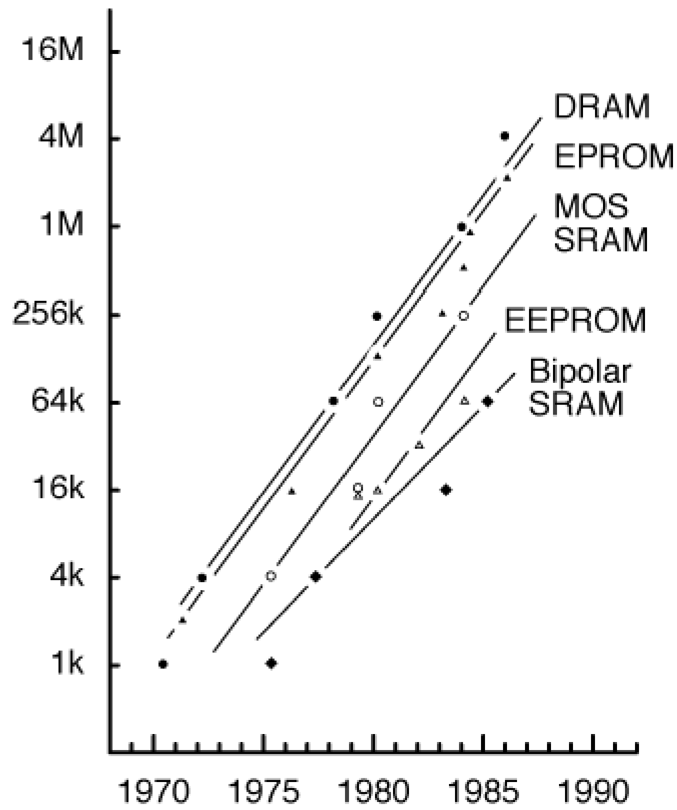
Read-Write Memory		Non-Volatile Read-Write Memory	Read-Only Memory
Random Access	**Non-Random Access**	EPROM E^2PROM FLASH	Mask-Programmed Programmable (PROM)
SRAM DRAM	FIFO LIFO Shift Register CAM		

Where does your brain's memory fit into these classification schemes?

More Classification

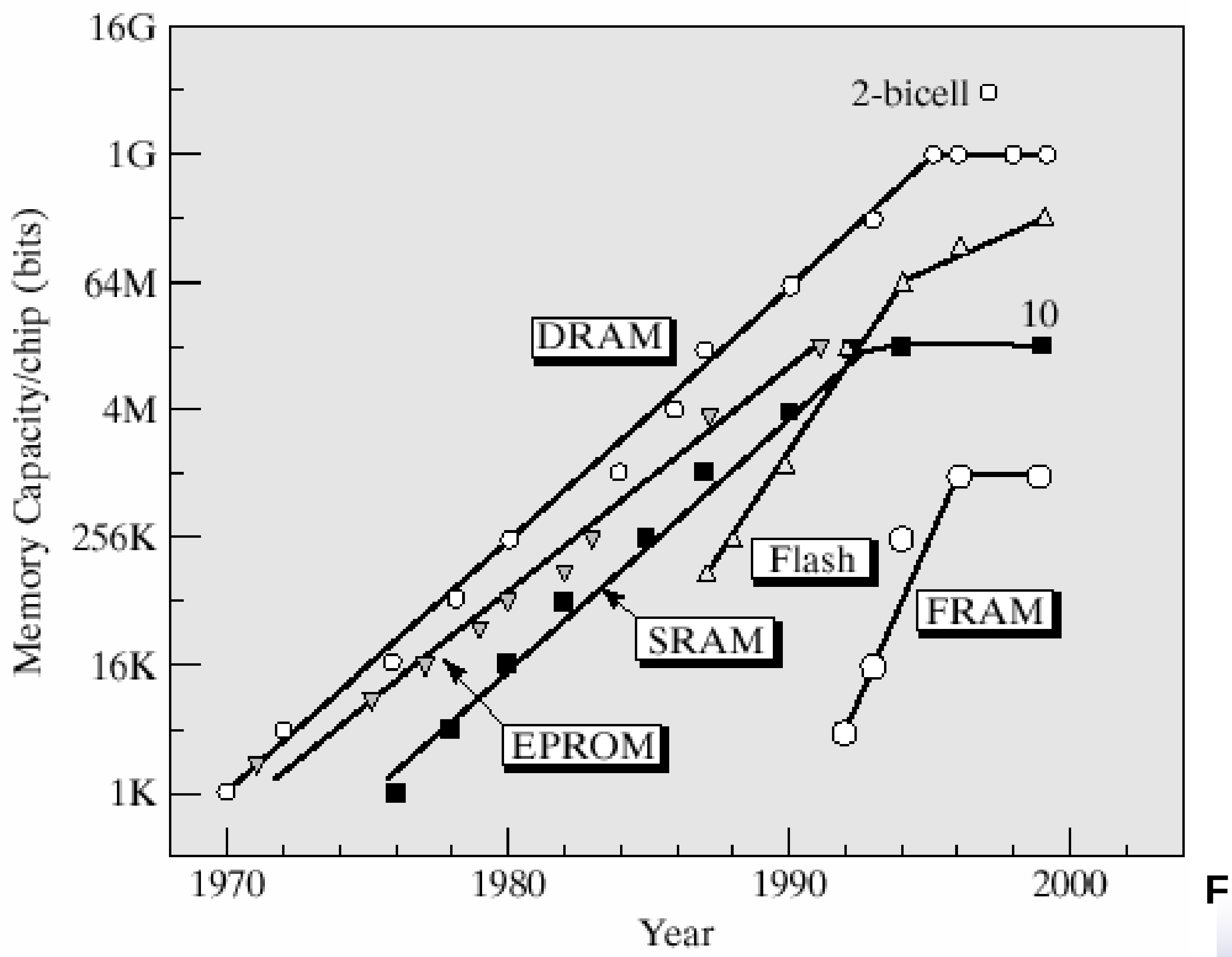
- **I/O Architecture:**
  - Based on the number of data input and output ports
  - Most memories uses a single I/O port
  - **Multiport memories** offer higher bandwidth
    - Example: register files used in RISC processors
    - Adds more complexity to the design
- **Application:**
  - Embedded Memories in SoCs
  - For massive storage (multiples of Gbytes and beyond), more cost effective solutions are to use **magnetic tapes** and **optical disks-**--they however, tend to be slower and provide limited access pattern

Semiconductor Memory Trends (up to the 90's)



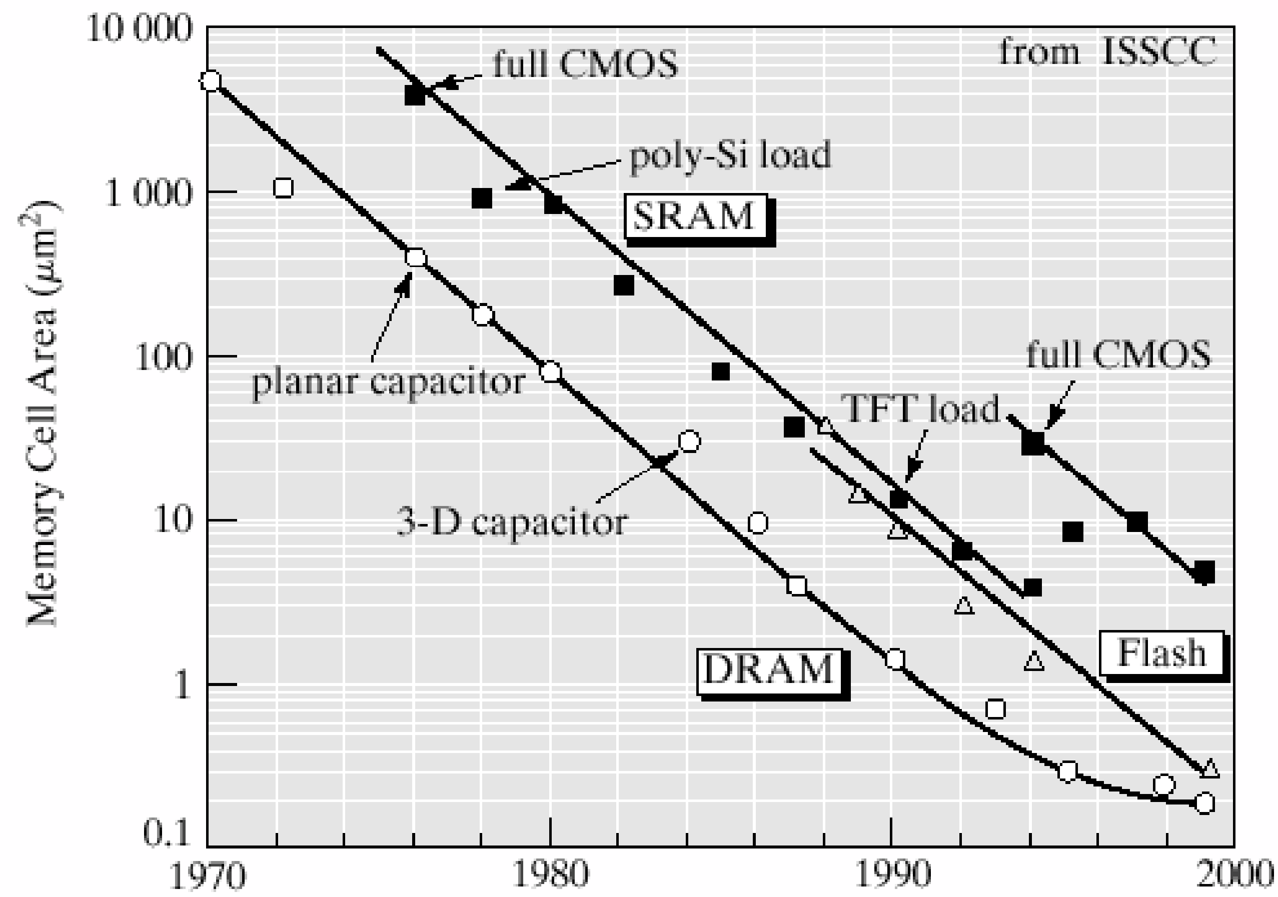
Memory Size as a function of time: x 4 every three years

Semiconductor Memory Trends (recent)



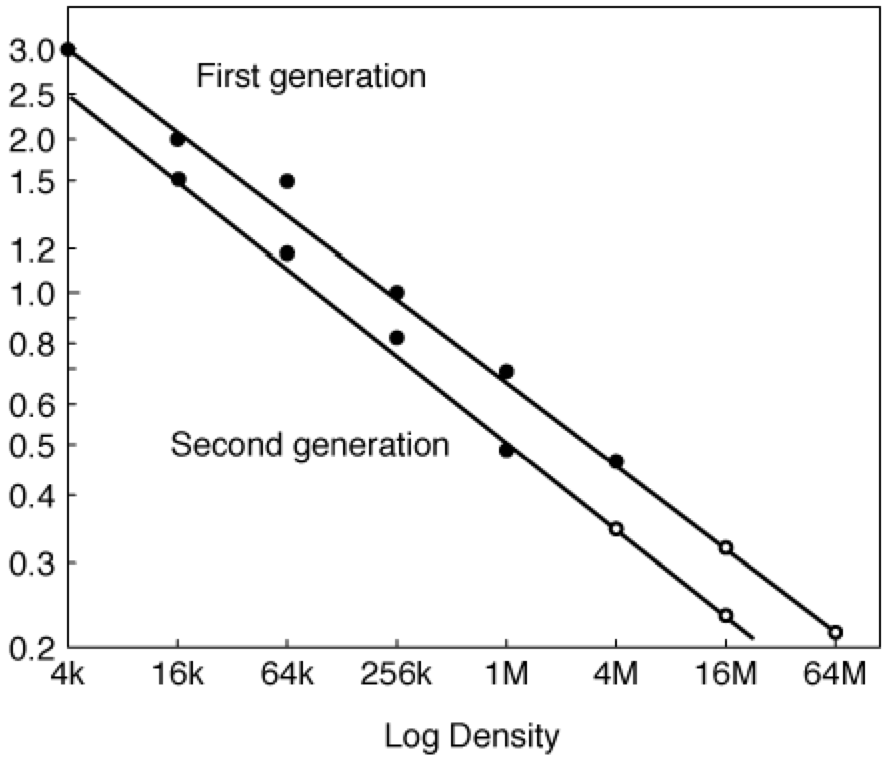
From [Itoh01]

Trends in Memory Cell Area



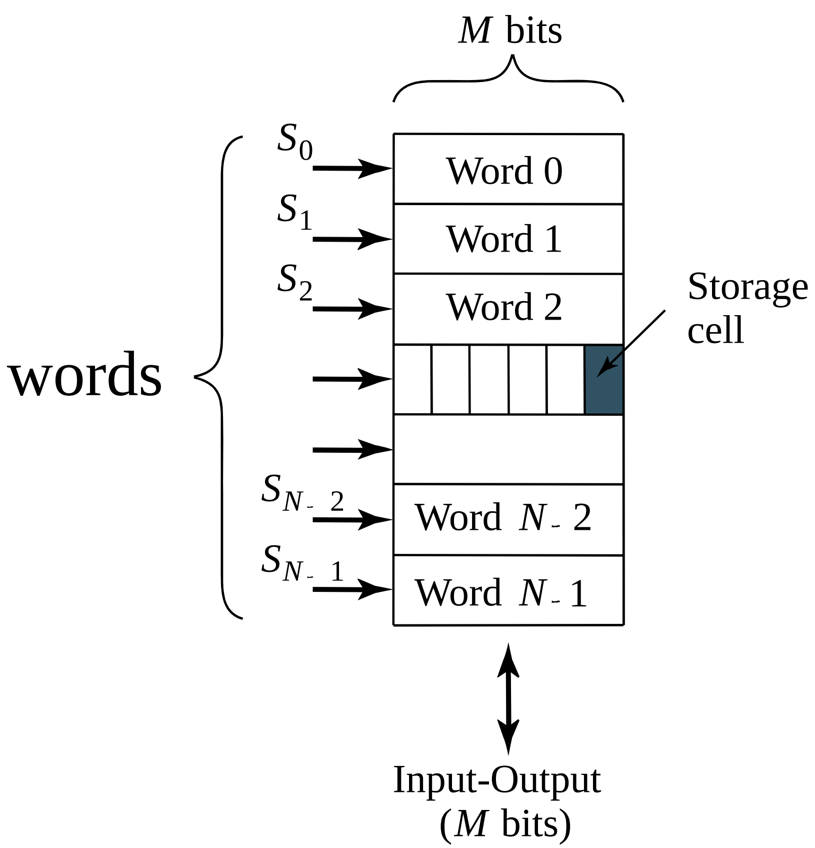
From [Itoh01]

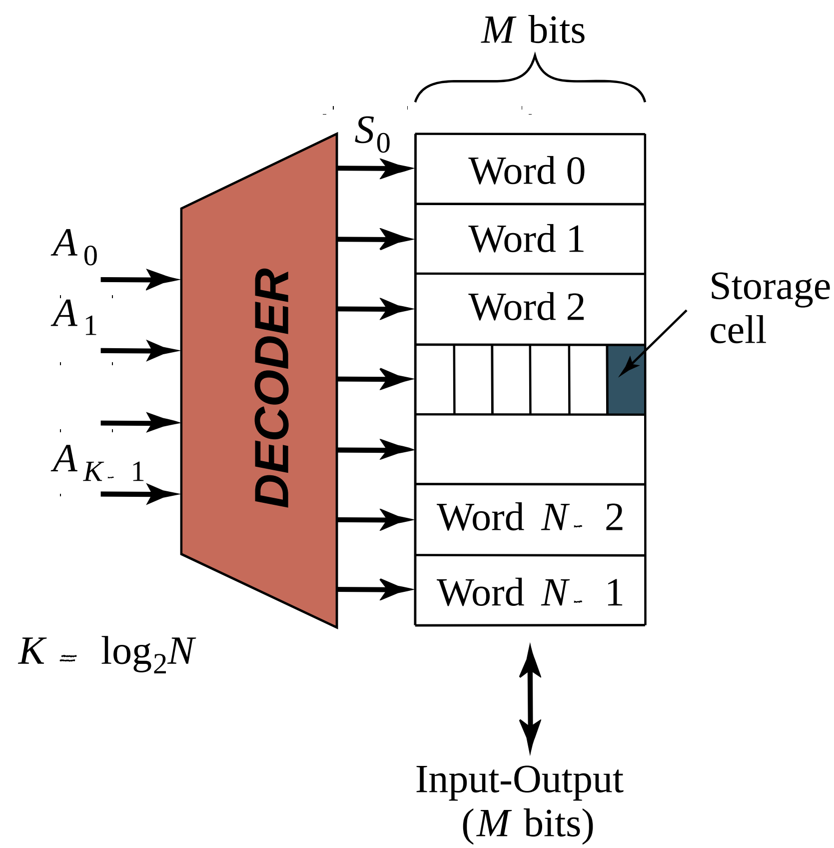
Semiconductor Memory Trends



Technology feature size for different SRAM generations

Memory Architecture: Decoders



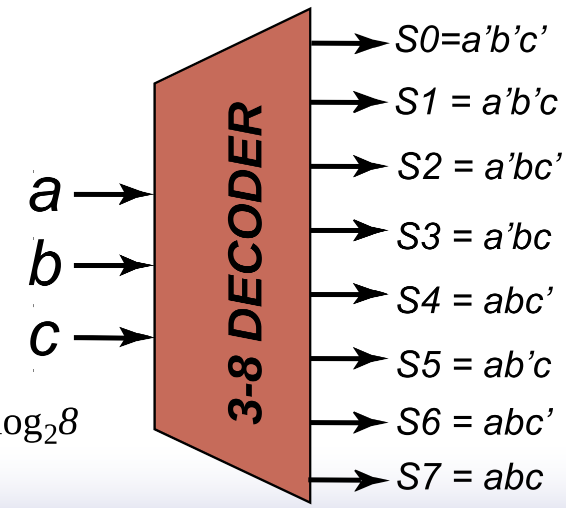


Intuitive architecture for N x M memory
Too many select signals:
N words == N select signals

Decoder reduces the number of select signals
$K = log_2 N$

Decoder Basic

- Recall that a decoder is a combinational circuit with k inputs and at most 2^k outputs.
- Its characteristics property is that for every combination of input values only ONE output =1 at the same time.
- Used to route input data to specific output line.

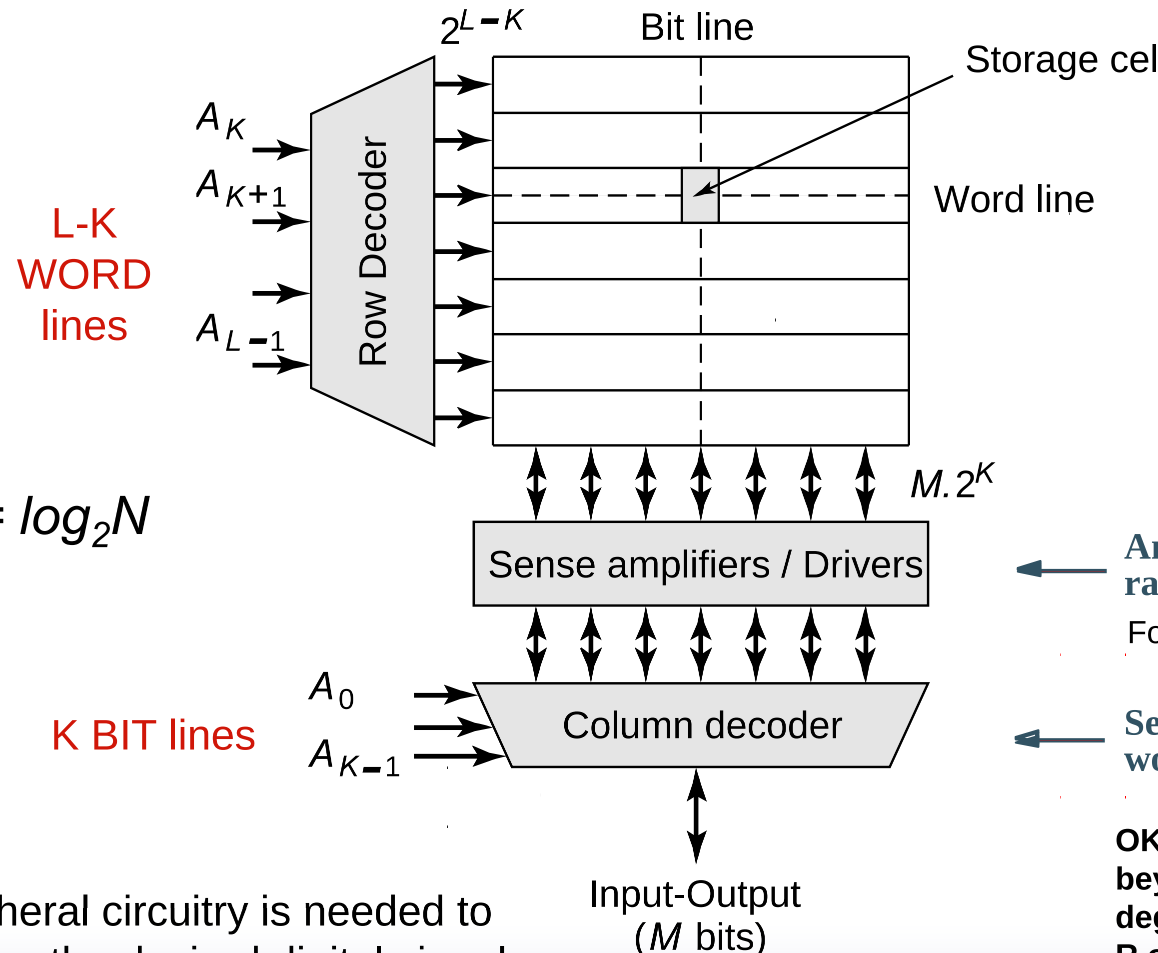


$3 = \log_2 8$

For example: for a=b=c=0, only S0 =1

Array-Structured Memory Architecture

Problem: **consider ~1 million ($N=2^{20}$) 8-bit ($M=2^3$) words, ASPECT RATIO is very large!!! or HEIGHT >> WIDTH, cannot be implemented and will result in very slow design…..**



$K = \log_2 N$

Solution: **Make vertical and horizontal dimensions of the same order of magnitude**

Store multiple words in one row

Use a column decoder to select the correct word

Amplify swing to rail-to-rail amplitude

For interfacing to the external world

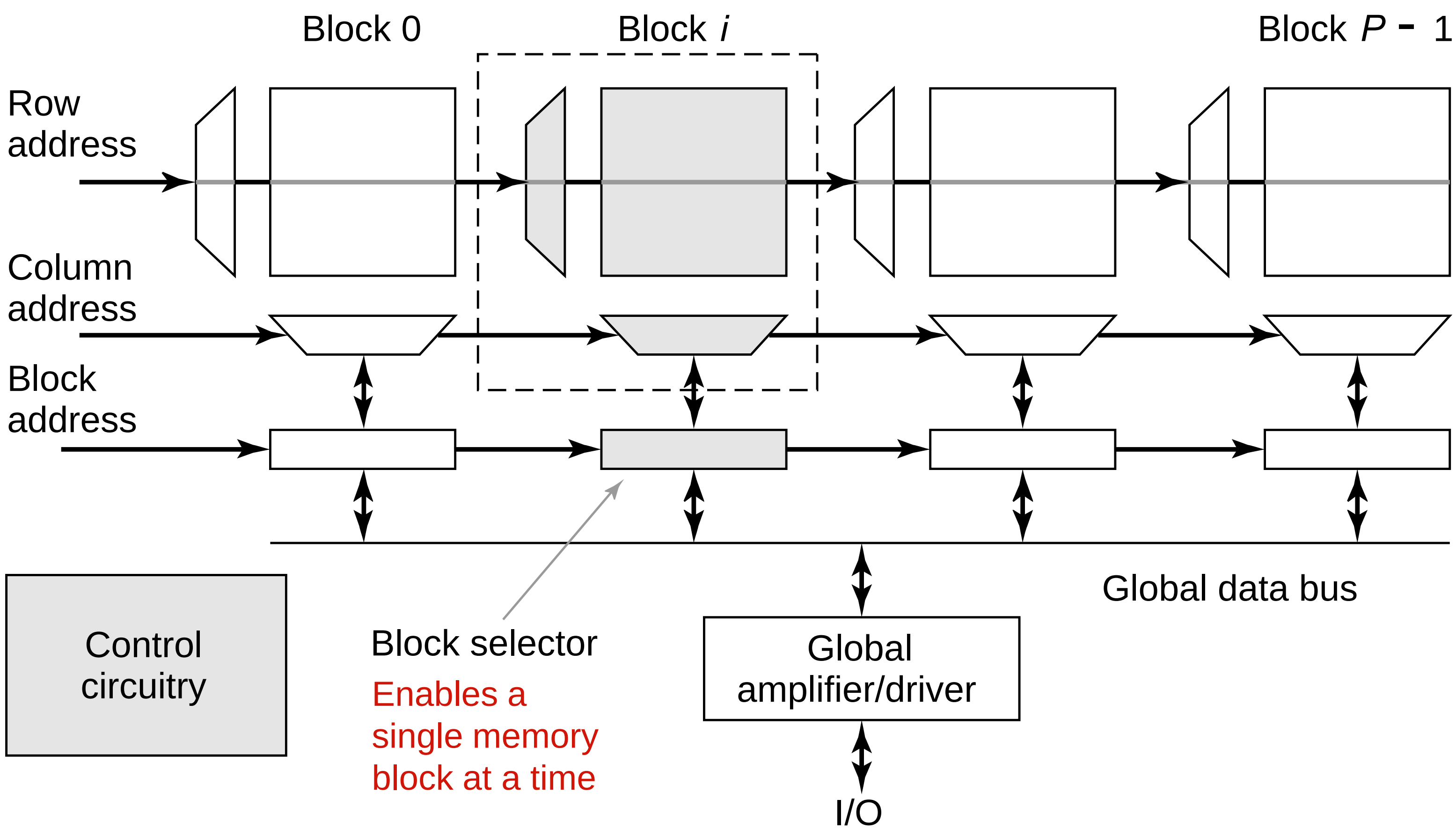
Selects appropriate word

OK for 64 Kbits to 256 Kbits beyond which speed degrades as length, C, and R of word/bit lines increase excessively

Peripheral circuitry is needed to recover the desired digital signal properties

Hierarchical Memory Architecture

For Larger Memories….

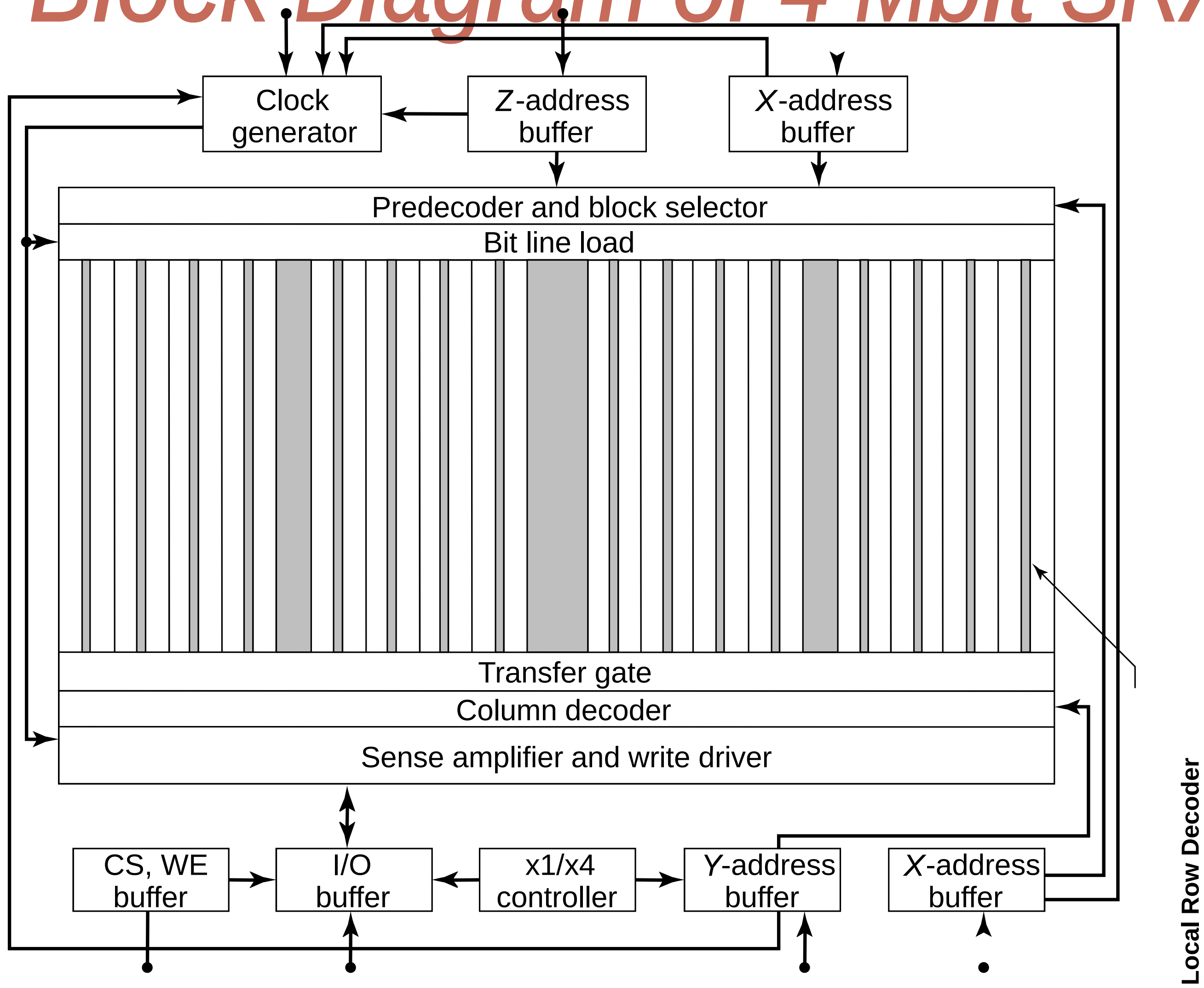


Advantages:

1. Shorter wires within blocks: faster access times

2. Block address activates only 1 block => power savings

Block Diagram of 4 Mbit SRAM



32 blocks, each containing 128 Kbits

Each block is structured as an array of 1024 rows and 128 columns

[Hirose90]

Read-Write Memories (RAM)

- **STATIC (SRAM)**

  Data stored as long as supply is applied
  Large (6 transistors/cell)
  Fast
  Differential

- **DYNAMIC (DRAM)**

  Periodic refresh required
  Small (1-3 transistors/cell)
  Slower
  Single Ended

6-transistor CMOS SRAM Cell

Should be minimum sized to achieve high memory density…..

Major advantage of dual BL: Q is clamped to Vdd by BL and prevents any inadvertent toggling of the INV pair

READ Operation:

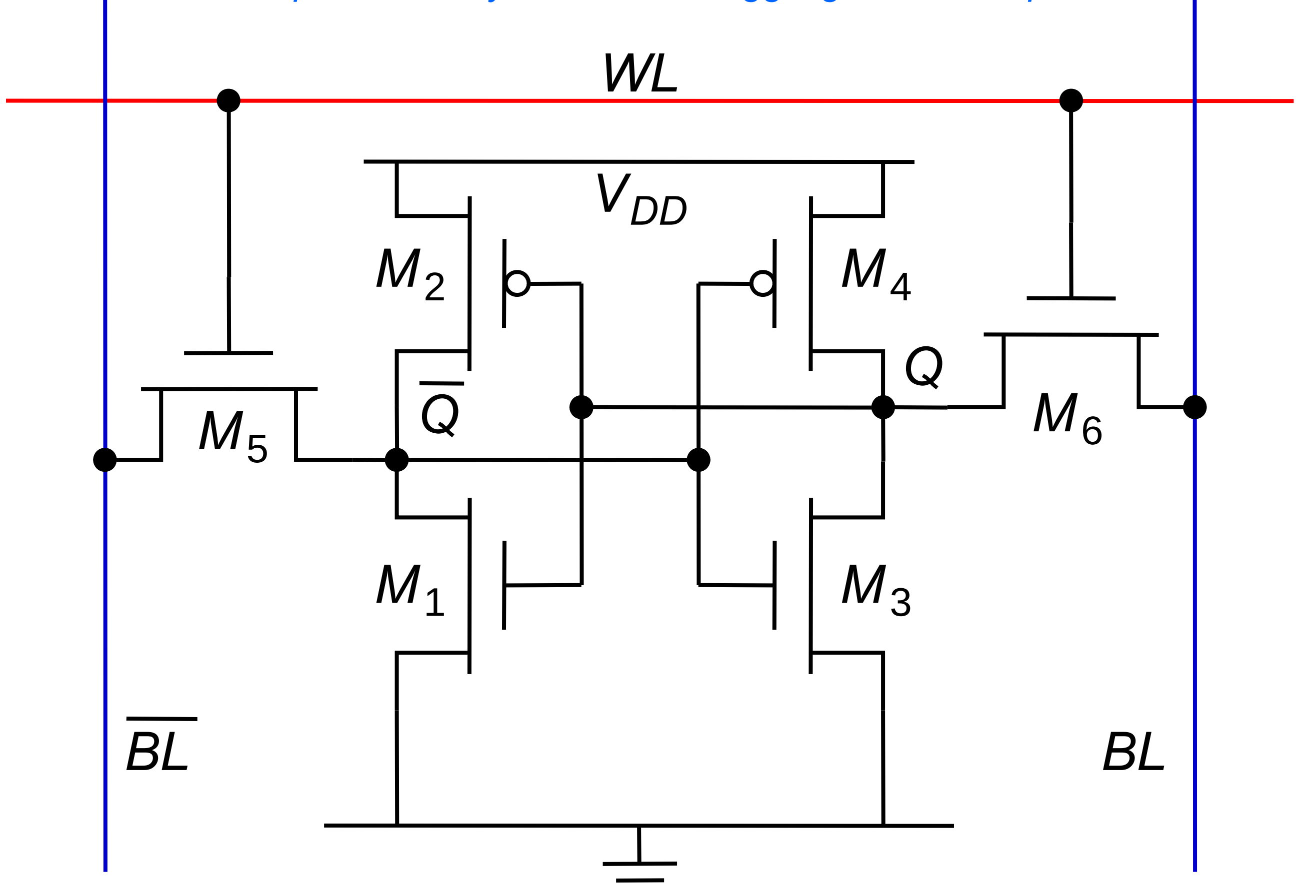
Assume 1 is stored at Q

Assume both BLs are held high before the read.

Read cycle started by asserting the WL, enables PTs M5 and M6

During a correct read operation values stored in Q and $\overline{Q}$ are transferred to the bit lines leaving BL at its precharge value and by discharging $\overline{BL}$ through M1-M5

A "0" can be read in a similar manner (now BL gets discharged through M6 and M3)



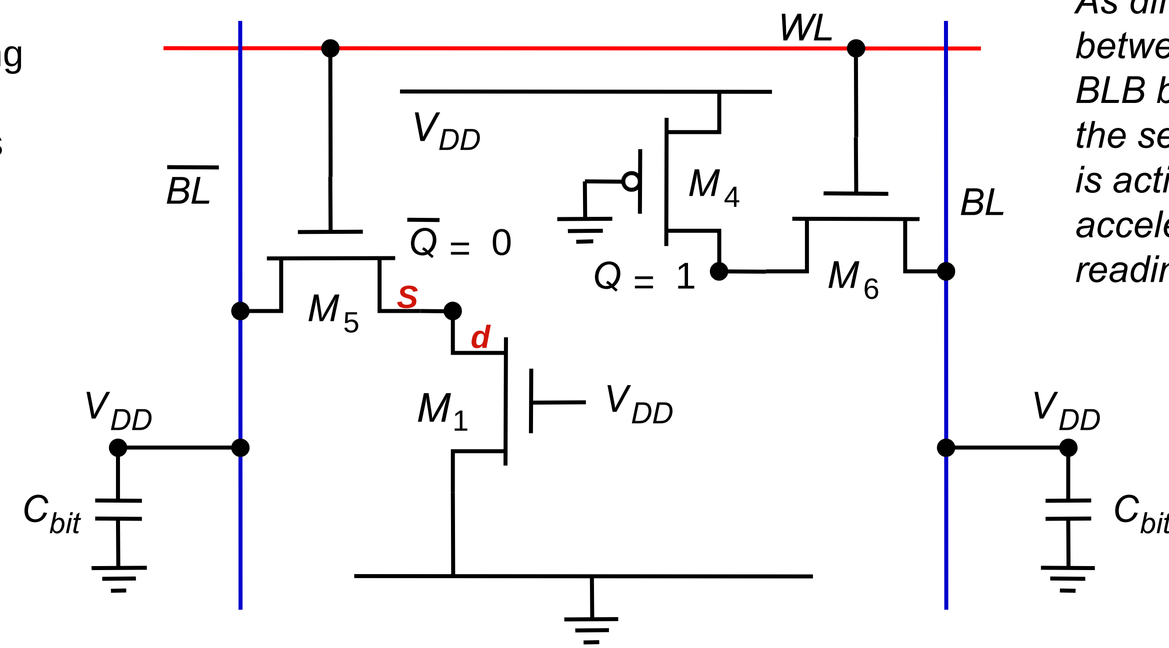
SRAM cell should be as small as possible…..but reliable operation requires careful sizing…

CMOS SRAM Analysis (Read "1" operation)

Transistor sizing is needed to avoid writing 1 accidentally, i.e., voltage at $\overline{Q}$ becomes $> V_M$ of Inv M3-M4

M1 must be stronger than M5

$\overline{Q}$ must stay low enough so that there is no substantial current through M3-M4 INV



As difference between BL and BLB builds up, the sense amp. is activated to accelerate the reading process

$$k_{n,M5}\left((V_{DD} - \Delta V - V_{Tn})V_{DSATn} - \frac{V_{DSATn}^2}{2}\right) = k_{n,M1}\left((V_{DD} - V_{Tn})\Delta V - \frac{\Delta V^2}{2}\right)$$

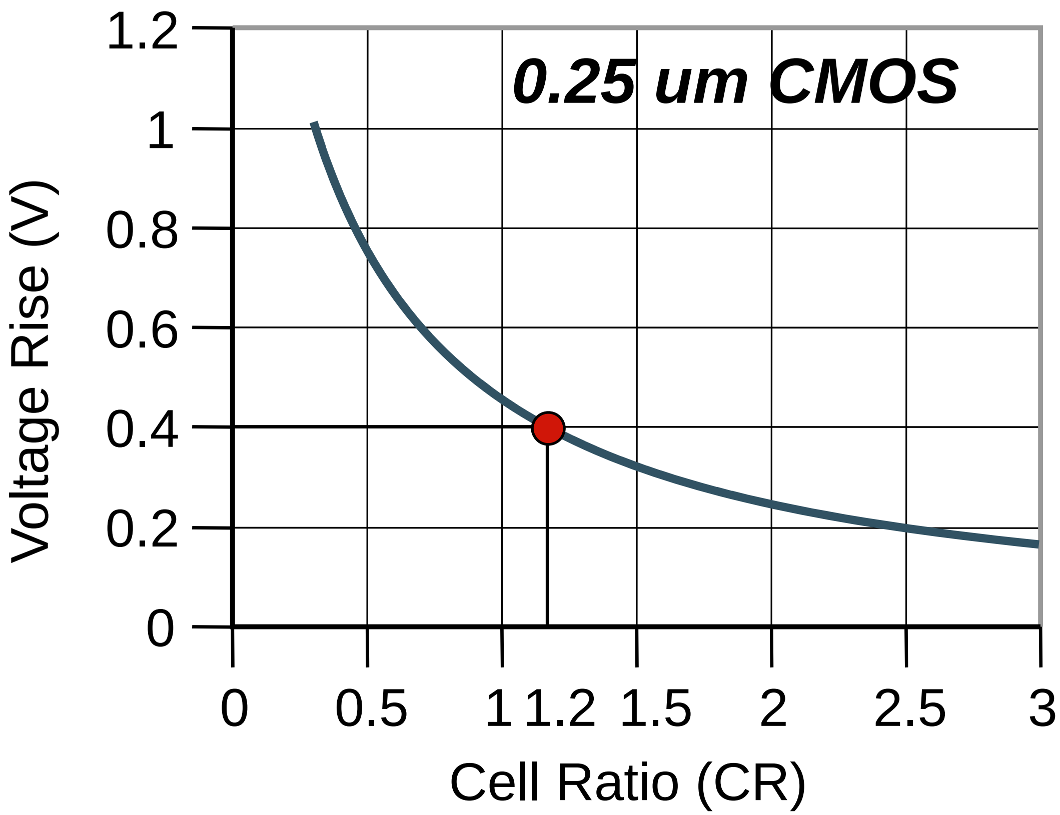
(M5 in saturation) *(M1 in linear)*

$$\Delta V = \frac{V_{DSATn} + CR(V_{DD} - V_{Tn}) - \sqrt{V_{DSATn}^2(1 + CR) + CR^2(V_{DD} - V_{Tn})^2}}{CR}$$

Value of the ripple voltage

CR = cell ratio = M1/M5

CMOS SRAM Analysis (Read)



$$CR = \frac{W_1/L_1}{W_5/L_5}$$

Choose M5 to be minimum size and M1 > M5

Node voltage must stay below the Vth of M3: CR must be >1.2

CMOS SRAM Analysis (Write)

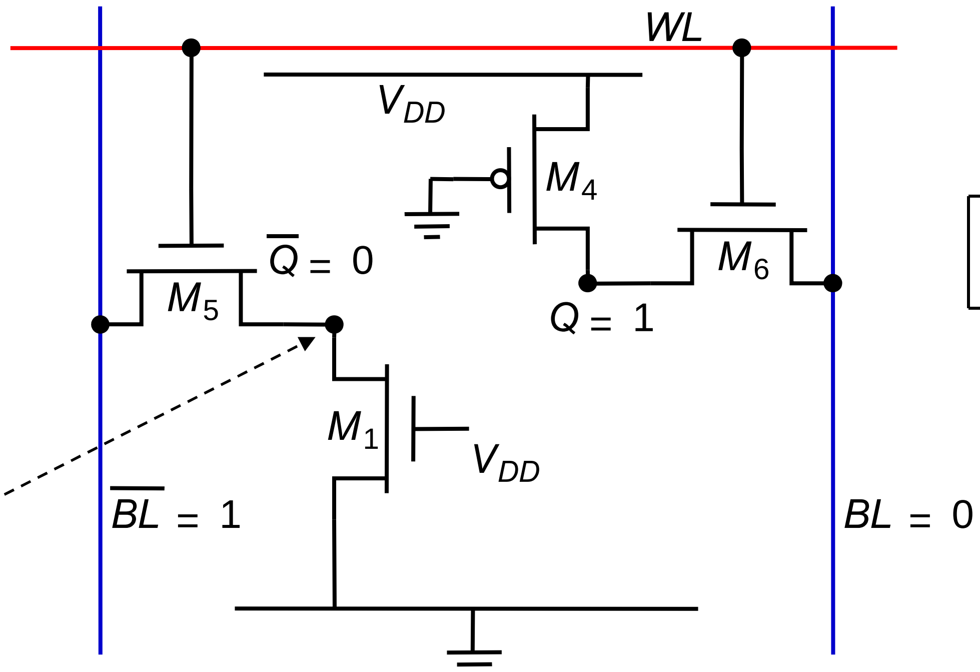
Assume that Q=1

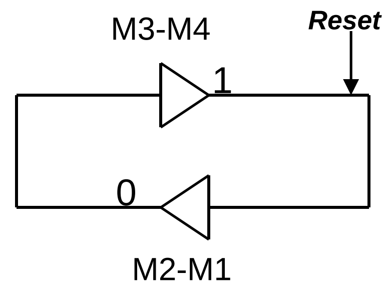
To write a 0 in the cell: set $\overline{BL}$=1 and BL=0

Similar to applying a reset pulse to an SR latch. FF will change state if sized properly

$\overline{Q}$ cannot be pulled high due to the sizing of M5 and M1 already done for reading

New value must be written through M6





Reliable writing of the cell is ensured if we can pull node Q low enough—below the Vth of M1

$$k_{n,M6}\left((V_{DD}-V_{Tn})V_Q-\frac{V_Q^2}{2}\right) = k_{p,M4}\left((V_{DD}-|V_{Tp}|)V_{DSATp}-\frac{V_{DSATp}^2}{2}\right)$$

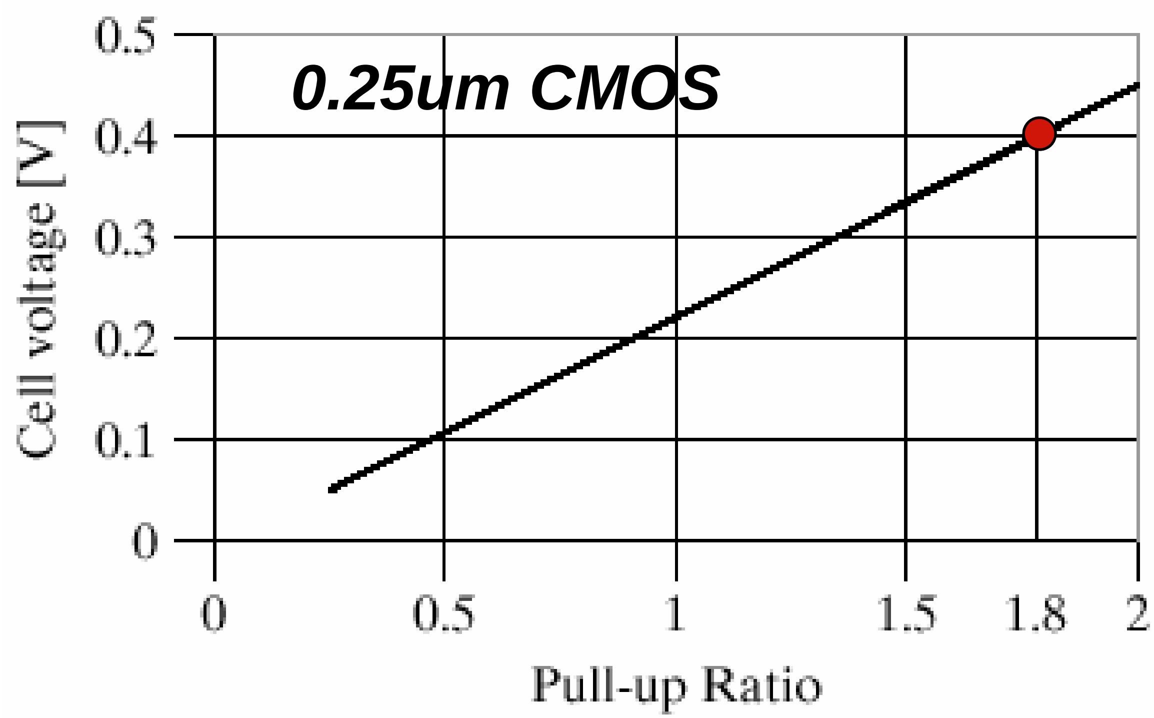
(M6 in linear) *(M4 in saturation)*

$$V_Q = V_{DD}-V_{Tn}-\sqrt{(V_{DD}-V_{Tn})^2-2\frac{\mu_p}{\mu_n}PR\left((V_{DD}-|V_{Tp}|)V_{DSATp}-\frac{V_{DSATp}^2}{2}\right)},$$

PR = pull-up ratio of cell = M4/M6

CMOS SRAM Analysis (Write)

Dependence of V_Q on Pull-up Ratio…..lower PR gives lower V_Q



$$PR = \frac{W_4/L_4}{W_6/L_6}$$

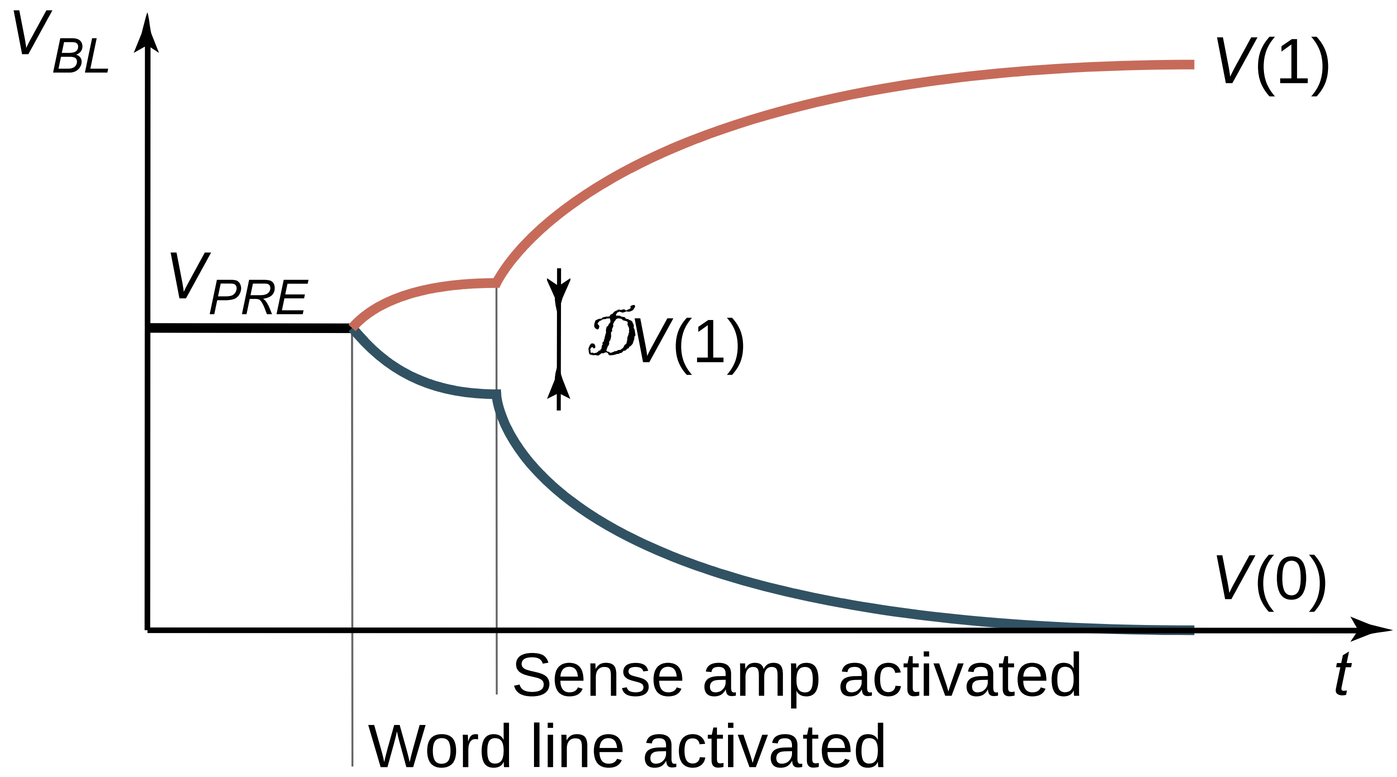
Should be low to keep V_Q low

PR between the PMOS (M4) pull-up and the NMOS (M6) Pass Transistor must be < 1.8 to keep Vtn < 0.4 V

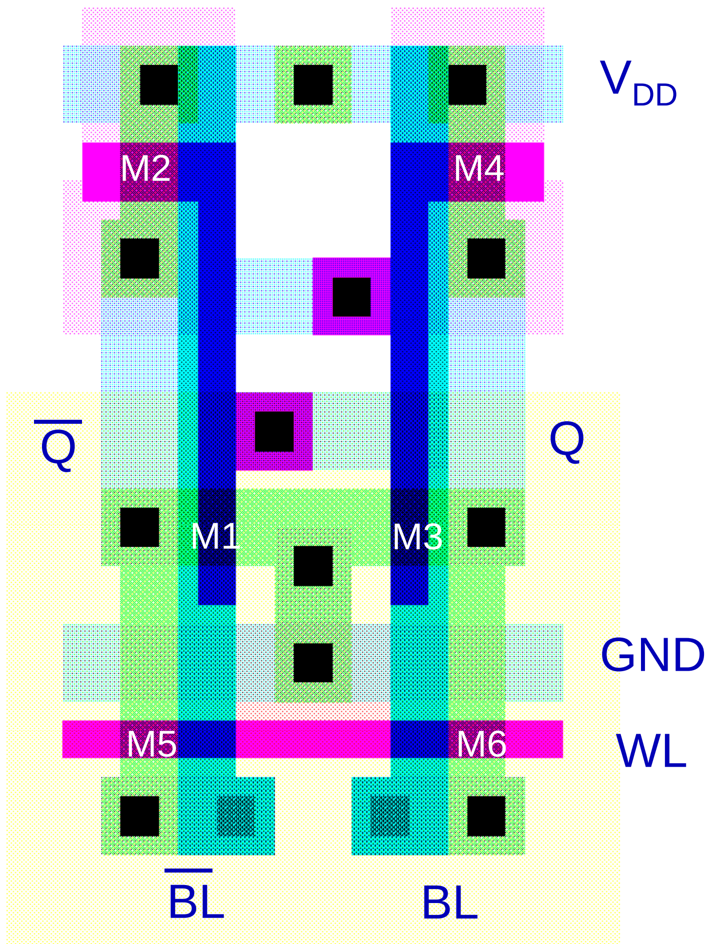
Performance of SRAM

- Read operation is more critical. It requires discharging of the large bit line capacitance through the stack of 2 transistors (M1-M5)
- Write time is dominated by the propagation delay of the cross-coupled inverter pair, since the drivers that set BL and $\overline{BL}$ can be large
- Sense amplifiers used to accelerate Read time….as the difference between BL and $\overline{BL}$ builds up, sense amplifier is activated, and it discharges one of the bit lines

Sense Amp Operation



6T-SRAM — Layout



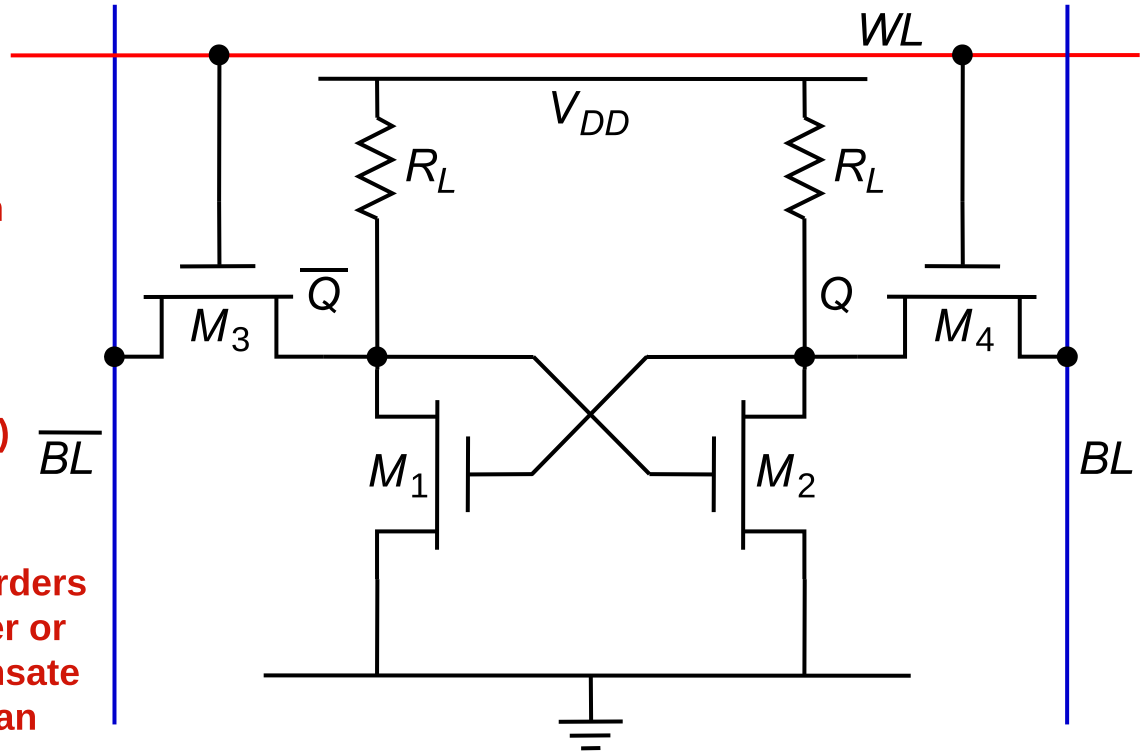
6T SRAM Takes significant area…the two PMOS need n-wells

Resistive-load (4T) SRAM Cell

Reduce area using resistive load inverters…simplifies writing

R_L must maintain the state of the cell, that is compensate for the leakage currents (~10^{-15}A)

I_{load} must be two orders of magnitude larger or > 10^{-13}A to compensate for leakage—puts an upper limit on R_L



Replacing the PMOSs by resistors reduces wiring

SRAM cell size reduced by 1/3

Static power dissipation -- Want R_L large (use undoped poly)
Bit lines precharged to V_{DD} to address t_p problem

SRAM Characteristics

Instead of PMOS devices, use parasitic devices on top of cell structure using thin-film transistors (TFTs)

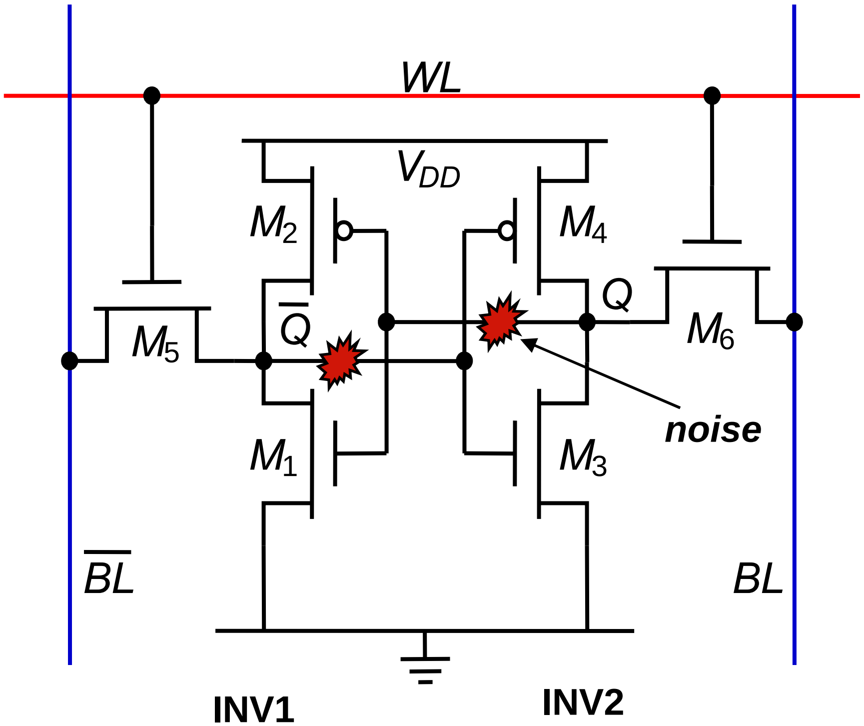
Table 12-2 Comparison of CMOS SRAM cells used in 1-Mbit memory (from [Takada91])

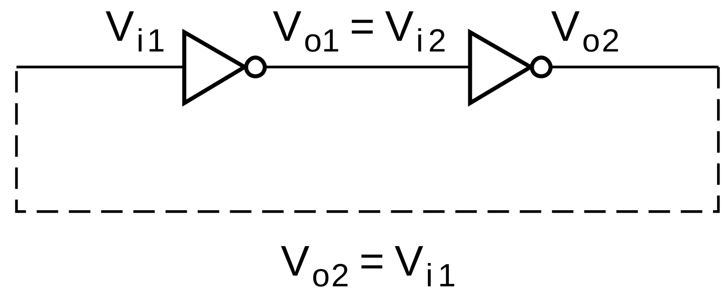
	Complementary CMOS	**Resistive Load**	**TFT Cell**
Number of transistors	6	4	4 (+2 TFT)
Cell size	58.2 μm^2 (0.7-μm rule)	40.8 μm^2 (0.7-μm rule)	41.1 μm^2 (0.8-μm rule)
Standby current (per cell)	10^{-15} A	10^{-12} A	10^{-13} A

Use high Vt

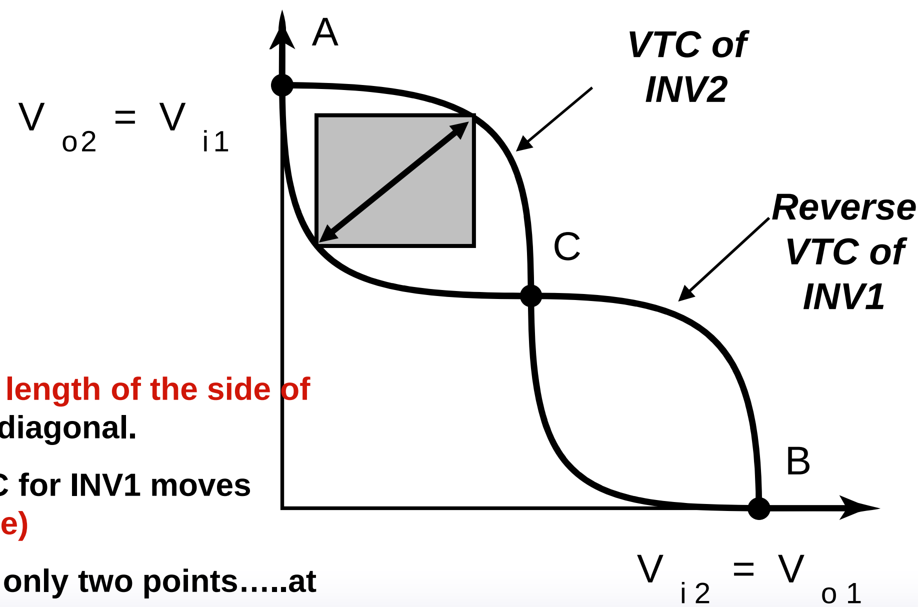
However, embedded SRAM cells---used in processor caches, employ 6T cells.

6-T CMOS SRAM Cell: Static Noise Margin





Butterfly Curve



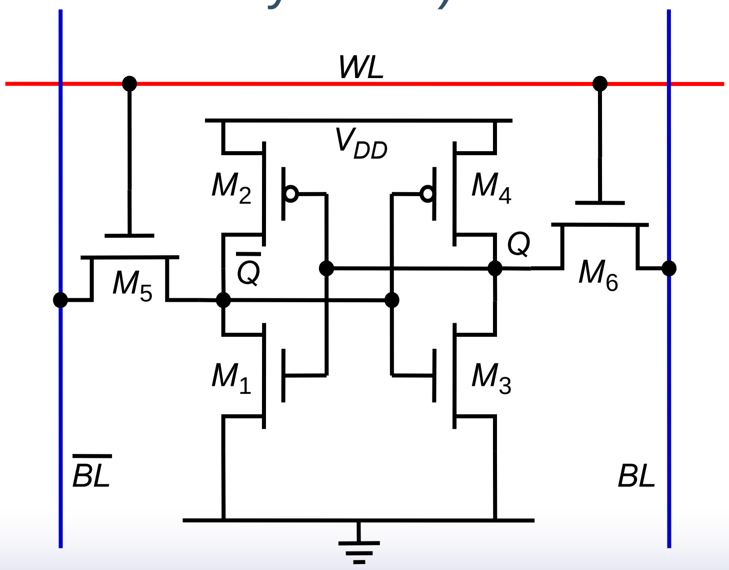
The SNM (hold margin) can be estimated graphically by the length of the side of the square fitted between the VTCs and having the longest diagonal.

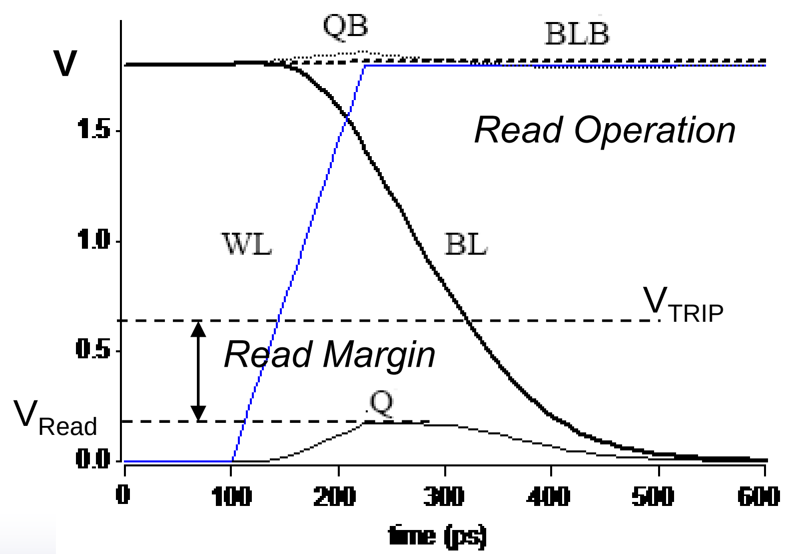
As noise increases at the two nodes above, the reverse VTC for INV1 moves upward, while the VTC for INV2 moves to the left (worst case)

Once they both move by the SNM value, the curves meet at only two points…..at A' and B'…… and any further noise flips the data.

Static Noise Margin (SNM)

- **Hold Margin:** How strongly the node storing ‘1’ and the node storing ‘0’ are coupled to V_{DD} and V_{SS} respectively.
- **Read Margin:** The difference between V_{TRIP} and V_{READ} (max. voltage at Q)
- **Write Margin*:*** The maximum voltage on a bit-line that allows writing to the cell, while the other bit-line is at V_{DD}. (not determined by the butterfly curve)

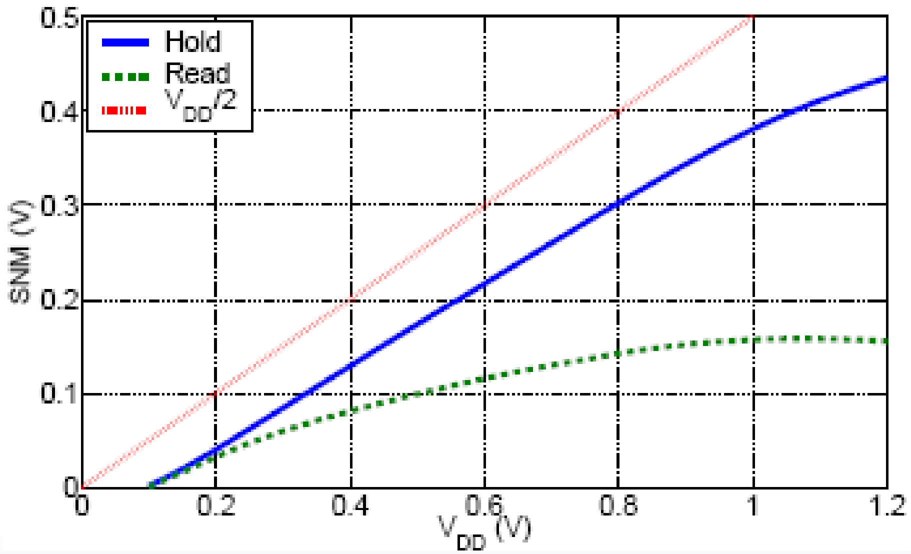


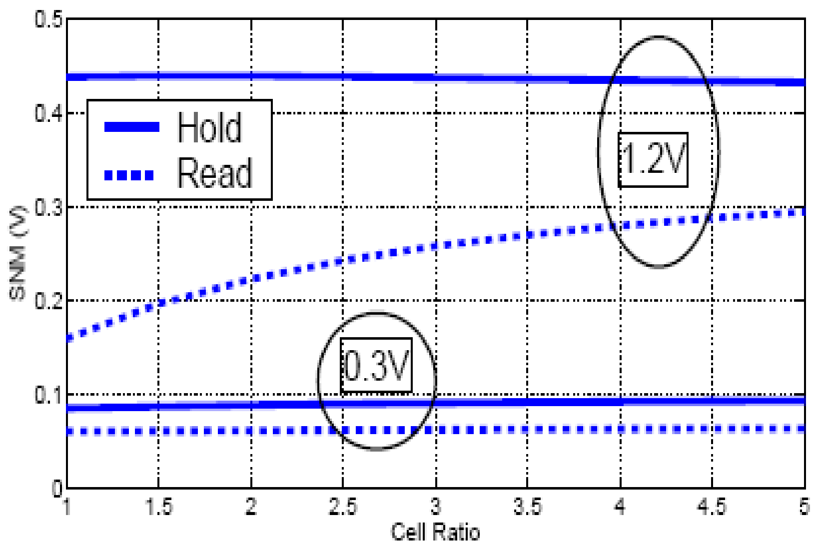


SNM Dependencies

- Dependence on V_{DD} : SNM for a bitcell with ideal VTCs is still limited to VDD/2
- Dependence on sizing

Here, Cell ratio = size of PD device over size of access device

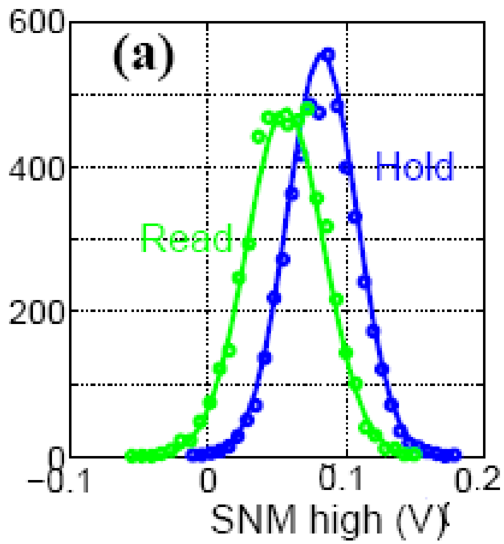




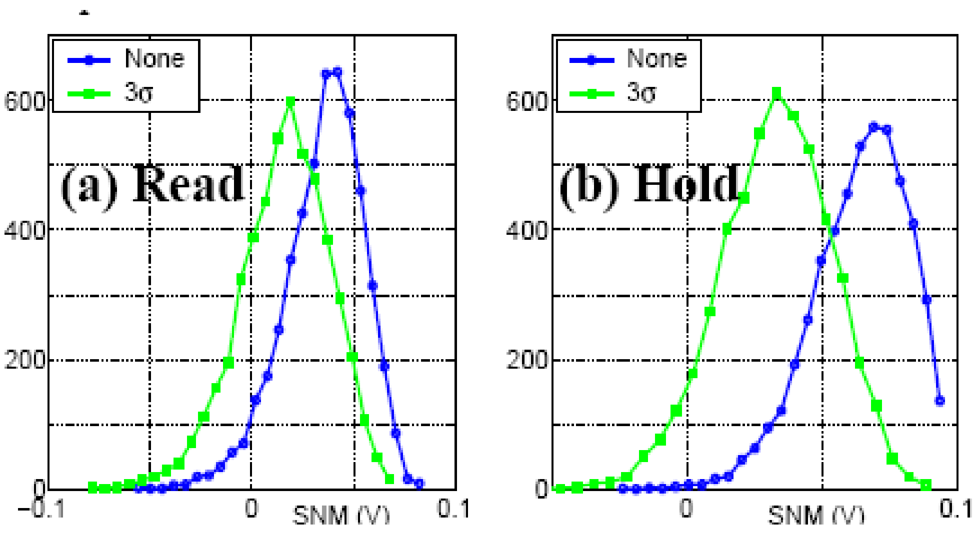
SNM Dependencies

- ❑ Dependence on random doping variation (V_{TH} mismatch)
- ❑ Dependence on global variation

Vth Mismatch

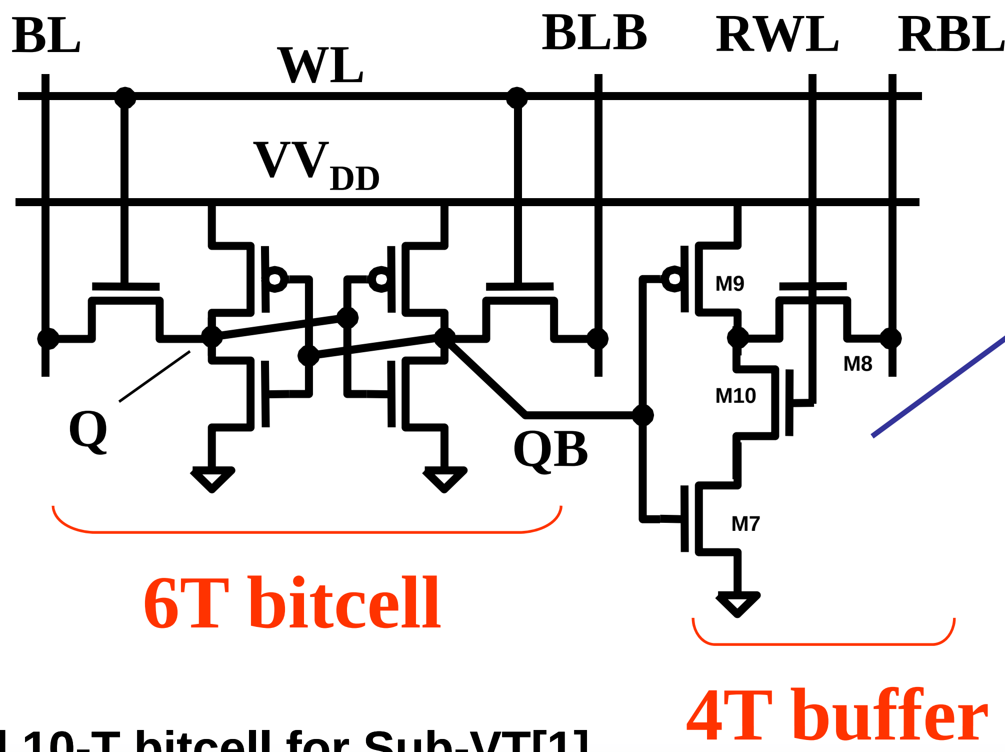


Global Variation



10-T SRAM

❑ The idea is to add a 4T buffer at one side:

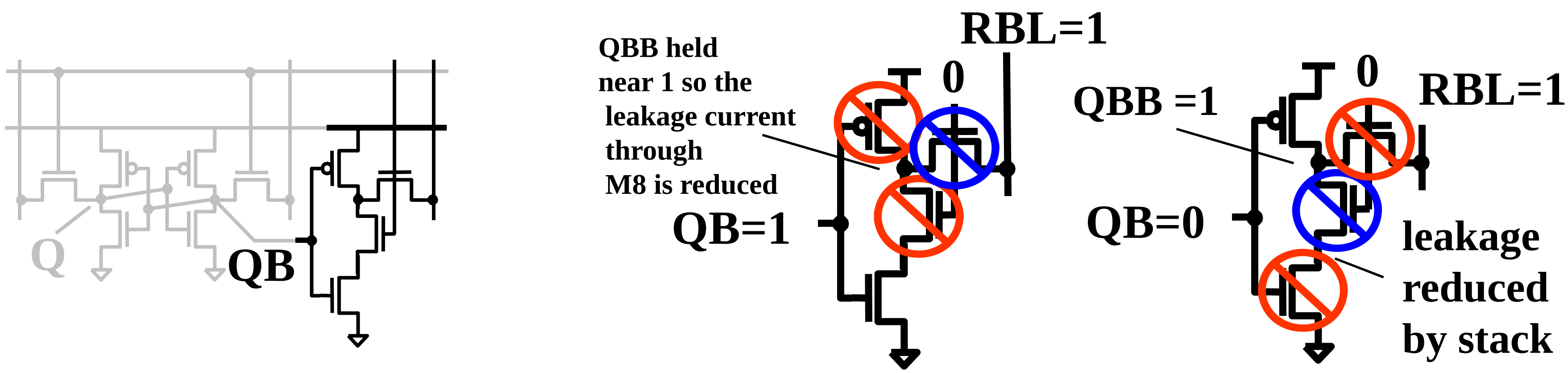


M7 to M10 to remove the problem of Read SNM by buffering thestored data during a read access.

Thus, the worst-case SNM for this bitcell is the Hold SNM related to M1 to M6, which is the same as the 6T Hold SNM for same sized M1 to M6

Proposed 10-T bitcell for Sub-VT[1]

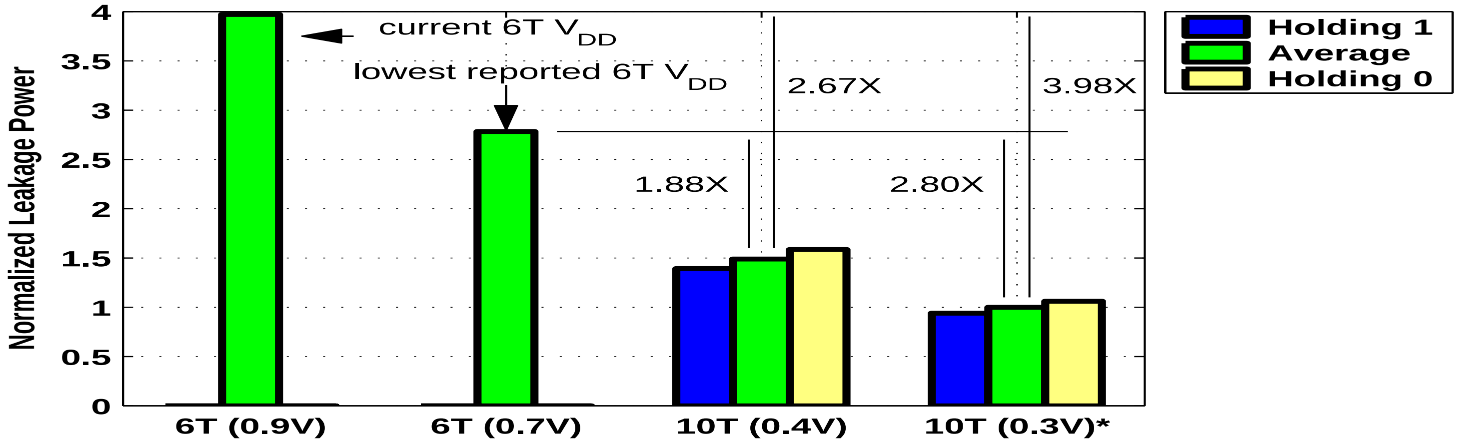
10T Bitcell Reduces Bitline Leakage



[1]

for iso-VDD, the 10T cell without M10 (a 9T cell) has 50% higher leakage current than the 6T, but adding M10 drops the overhead to 16%.

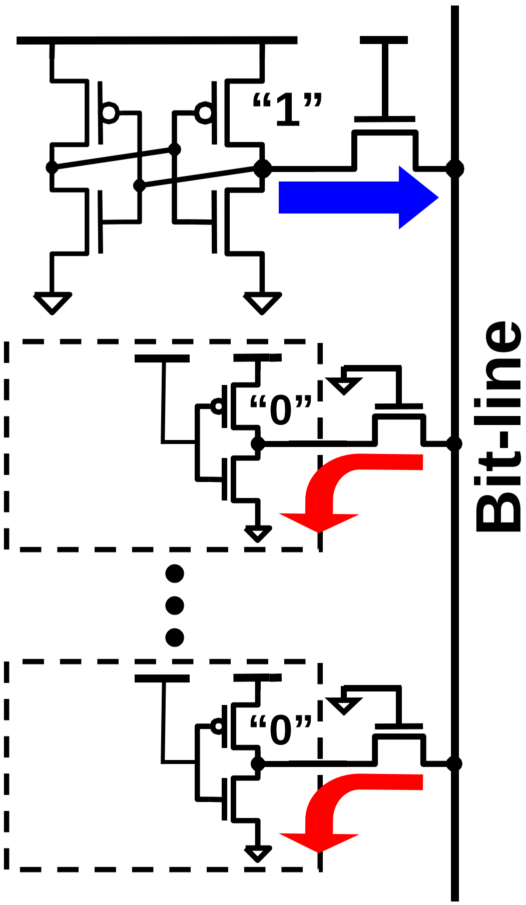
Leakage Power Savings with 10T Bitcell



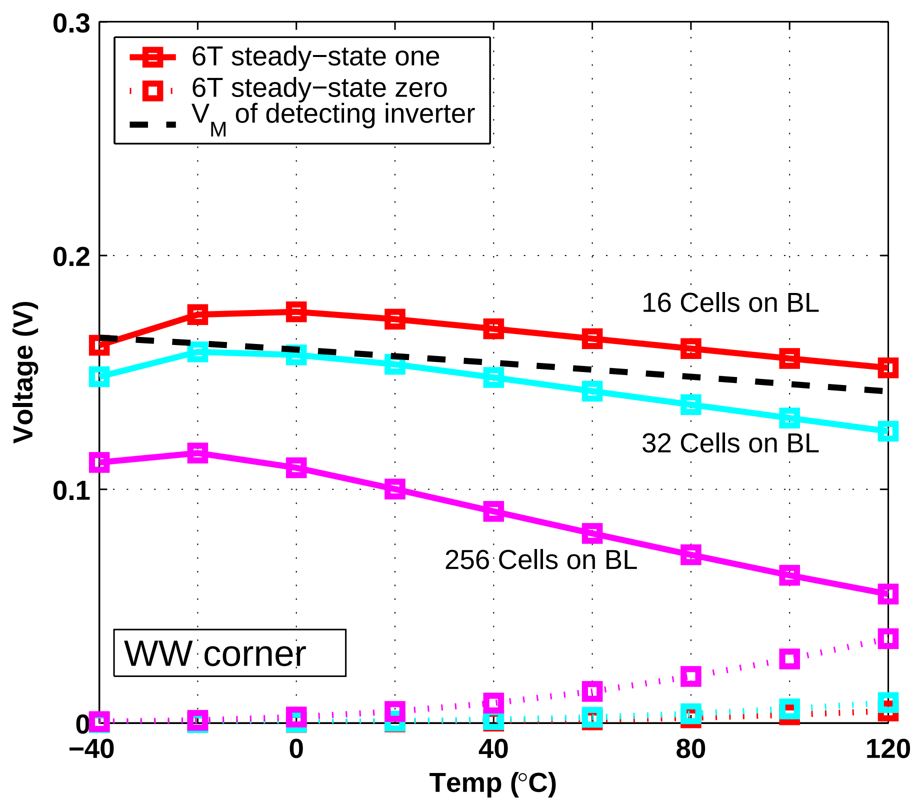
[1]

- 6T memories in 65nm usually at 0.9V or greater (lowest reported is 0.7V)
- 10T bitcell allows scaling to lower voltages
- Lower voltage operation reduces leakage power dramatically for unaccessed cells

Bitline Leakage Limits Integration Level



[1]



16 bitcells on bitline is best can hope for standard 6T

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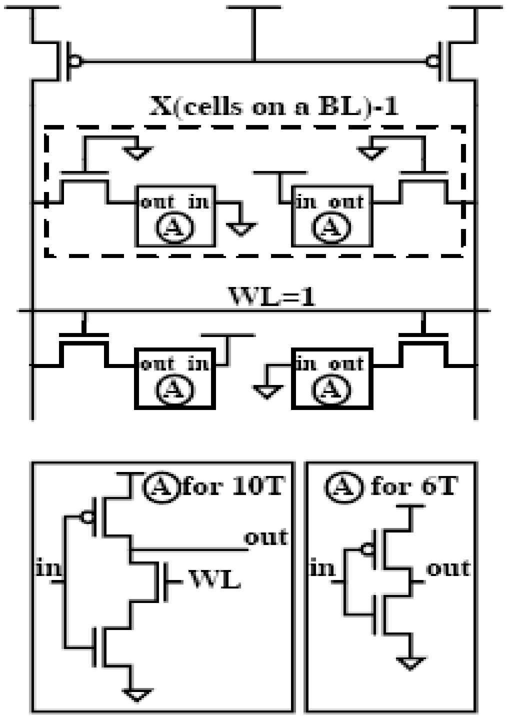
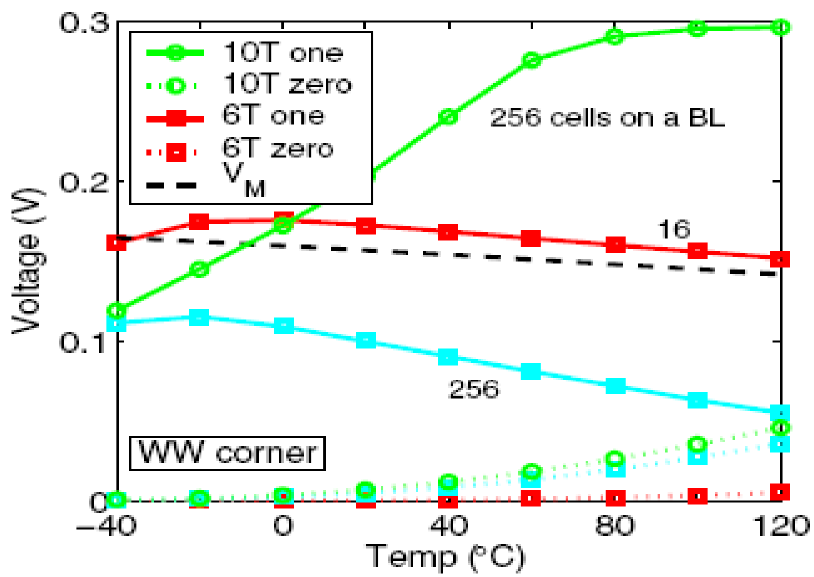
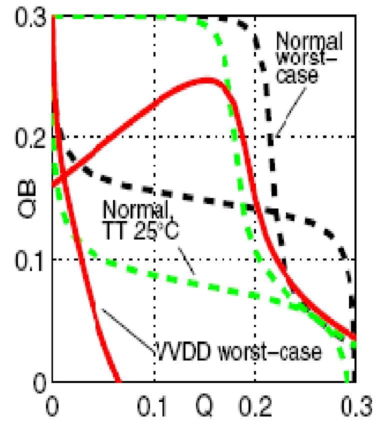




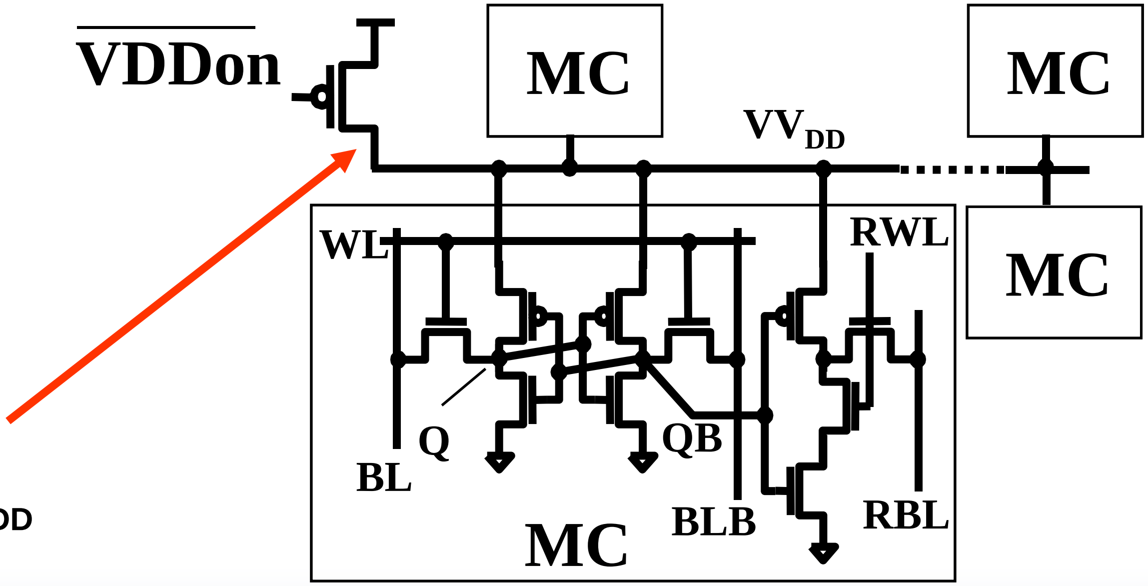
BL leakage limits the number of cells on a BL. The 10T bitcell can sustain 256 cells/BL at 0.3V compared to 16 without M10 (6T or 9T). higher level of integration allowed by the 10T cell reduces the peripheral circuits and slightly mitigates the bitcell area overhead[1].

10T Bitcell Allows Sub-VT Write

To achieve write in sub-threshold, the virtual supply (VVDD) to the selected cells floats during the write operation



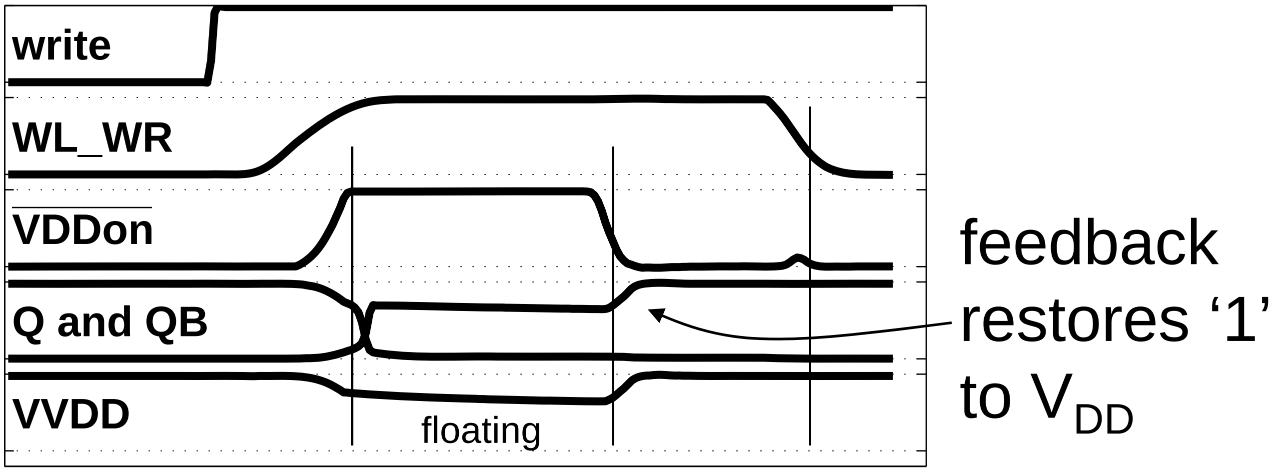
Folded WL shares VV_{DD}



[1]

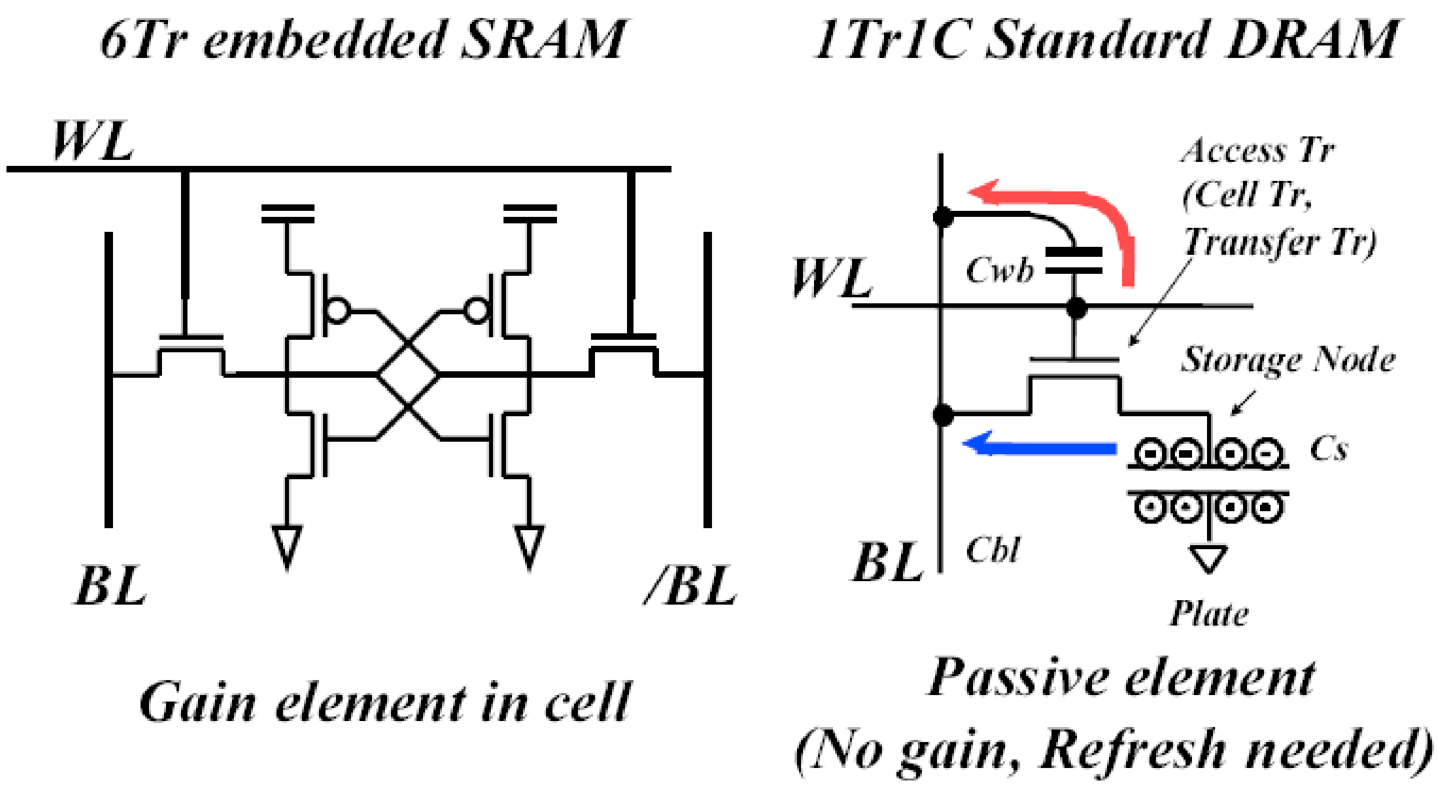
Cont'd

Floating V_{DD} weakens feedback and allows Write.



A virtual supply voltage (VVDD) that floats during write allows robust write operation into sub-VT (mono-stable butterfly curve). VVDD stops floating while WL_WR remains asserted to restore the '1'value to full VDD[1].

DRAM


6Tr embedded SRAM
1Tr1C Standard DRAM
WL
BL
/BL
Access Tr
(Cell Tr,
Transfer Tr)
WL
Cwb
Storage Node
Cs
BL
Cbl
Plate
Gain element in cell
Passive element
(No gain, Refresh needed)

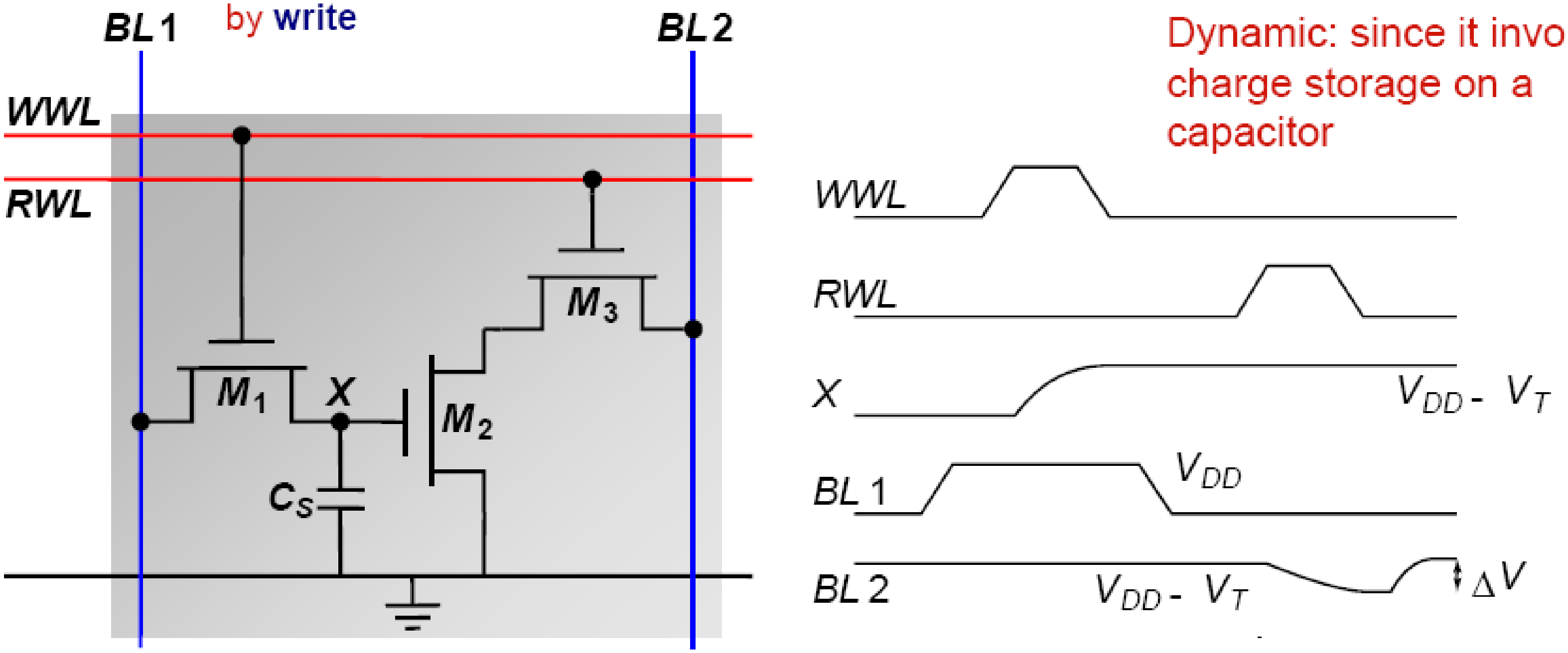
3-Transistor DRAM Cell (Early Days)

Periodic refresh operation consists of read followed by write

1 Kbit memory: Intel

Still used in some ASICs

Dynamic: since it involves charge storage on a capacitor



Cell is written by placing value on BL1 and asserting Write Word Line (WWL=1)

Data retained as charge stored on Cs once WWL=0

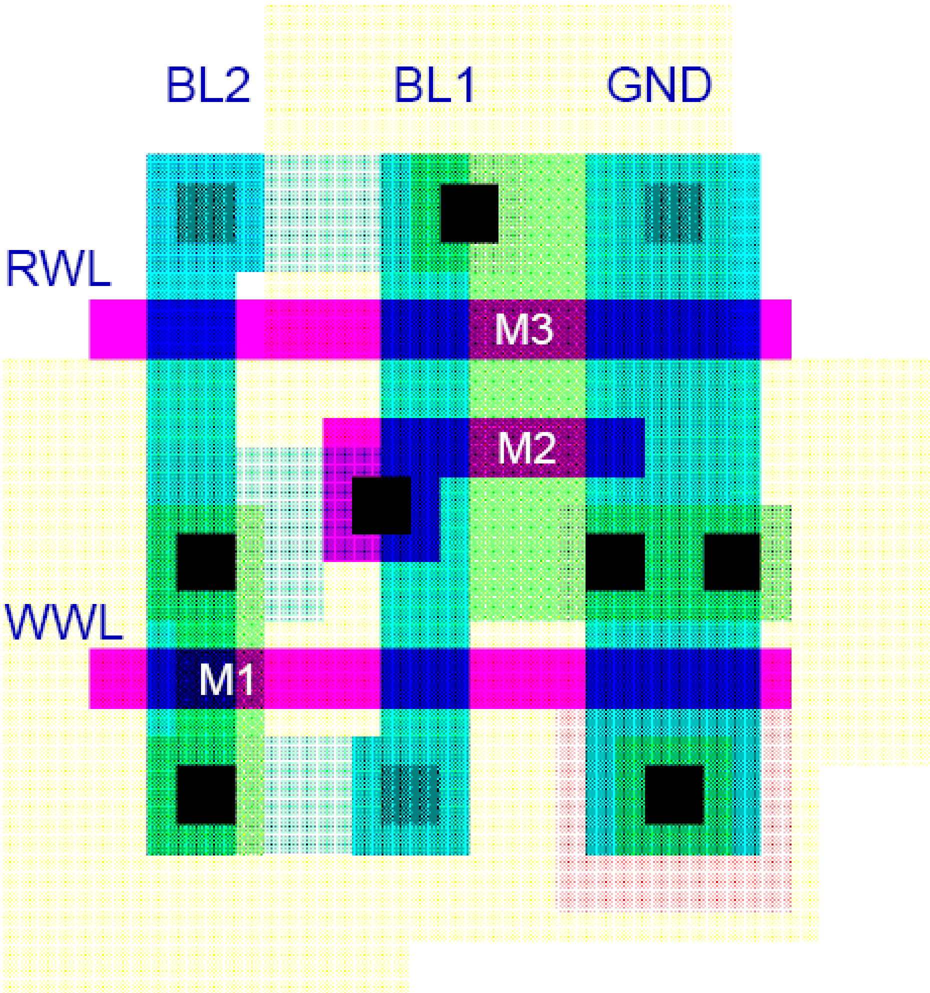
For reading the cell, RWL=1

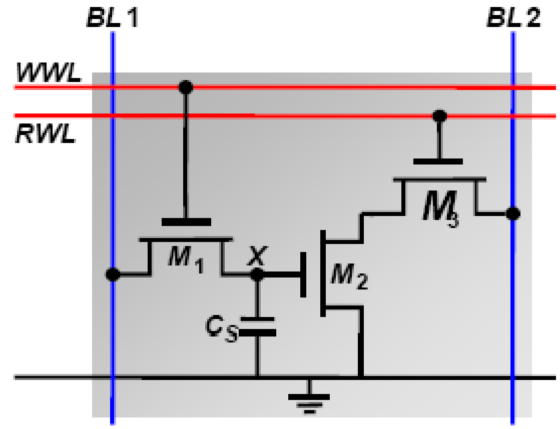
M2 can be on or off depending on stored value

BL2 is either clamped to Vdd or is precharged to either Vdd or Vdd-Vt

M2-M3 pulls BL2 low when X=1, otherwise BL2 remains high (cell is inverting: senses the inverse value of the stored signal)

3T-DRAM — Layout





Unlike SRAM, no constraint on device sizes

Read operation is non-destructive

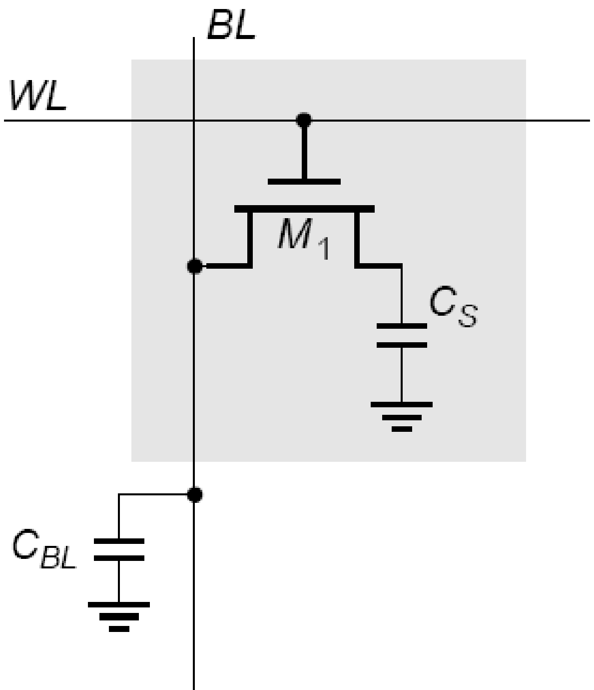
No special process steps needed

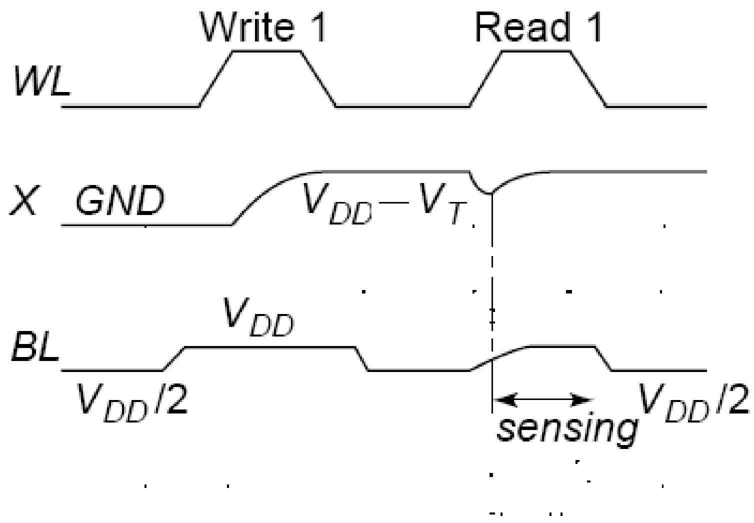
Value at node X = $V_{WWL} - V_{tn}$

This reduces the current through M2 during read operation and increases read access time: can use a higher value of V_{WWL} to avoid this

1-Transistor DRAM Cell

Most pervasive in commercial memory design





Write: Place data on BL and assert WL, depending on data value, Cs is 1 or 0

Read: before read, precharge BL to V_{PRE}

After WL=1, charge redistribution takes places between bit line and storage capacitance resulting in a voltage change on BL

$$\Delta V = V_{BL} - V_{PRE} = V_{BIT} - V_{PRE} \frac{C_S}{C_S + C_{BL}}$$

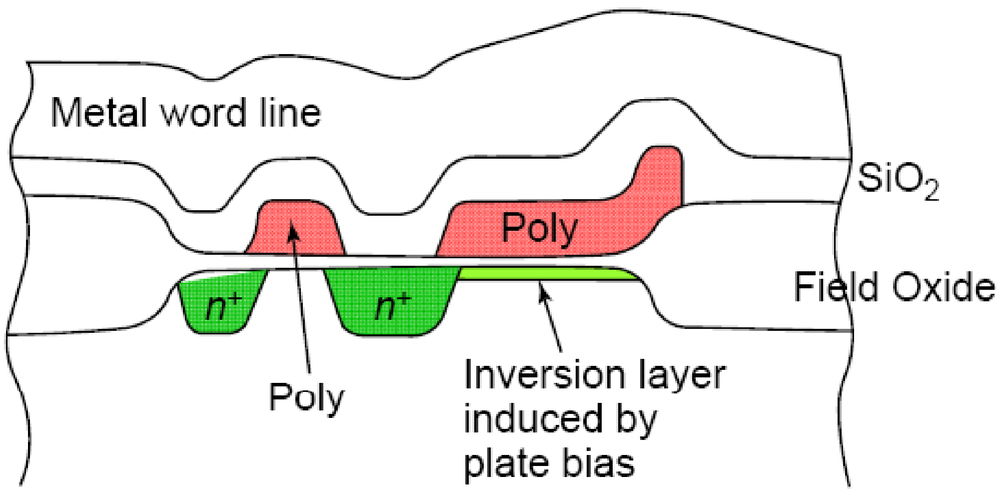
Charge transfer ratio (1-10%)

V_{BIT} is initial voltage on C_s. V_{BL} is final voltage on BL after charge redistribution.
Voltage swing is small since $C_s \ll C_{BL}$; typically around 250 mV.

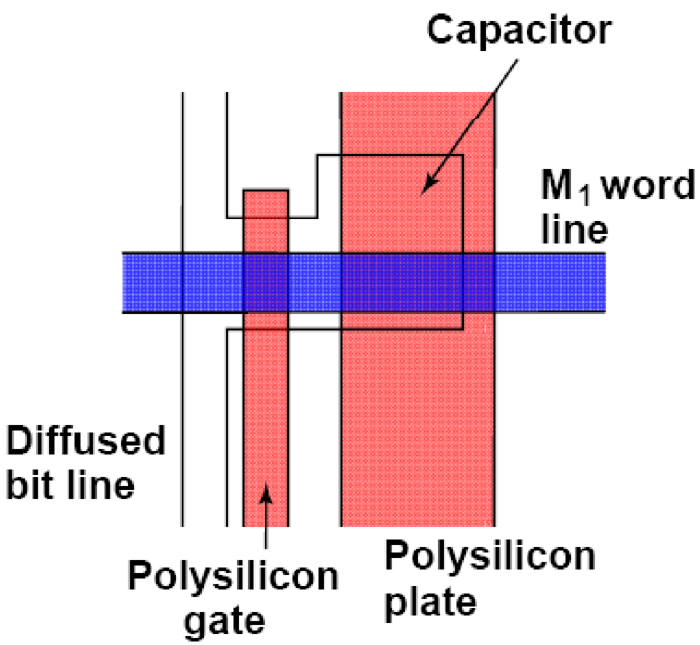
DRAM Cell Observations

- 1T DRAM requires a sense amplifier for each bit line, due to charge redistribution read-out.
- DRAM memory cells are single ended in contrast to SRAM cells.
- The read-out of the 1T DRAM cell is destructive; read and refresh operations are necessary for correct operation.
- Unlike 3T cell, 1T cell requires presence of an extra capacitance that must be explicitly included in the design.
- When writing a "1" into a DRAM cell, a threshold voltage is lost. This charge loss can be circumvented by bootstrapping the word lines to a higher value than V_{DD}

1-T DRAM Cell



Cross-section

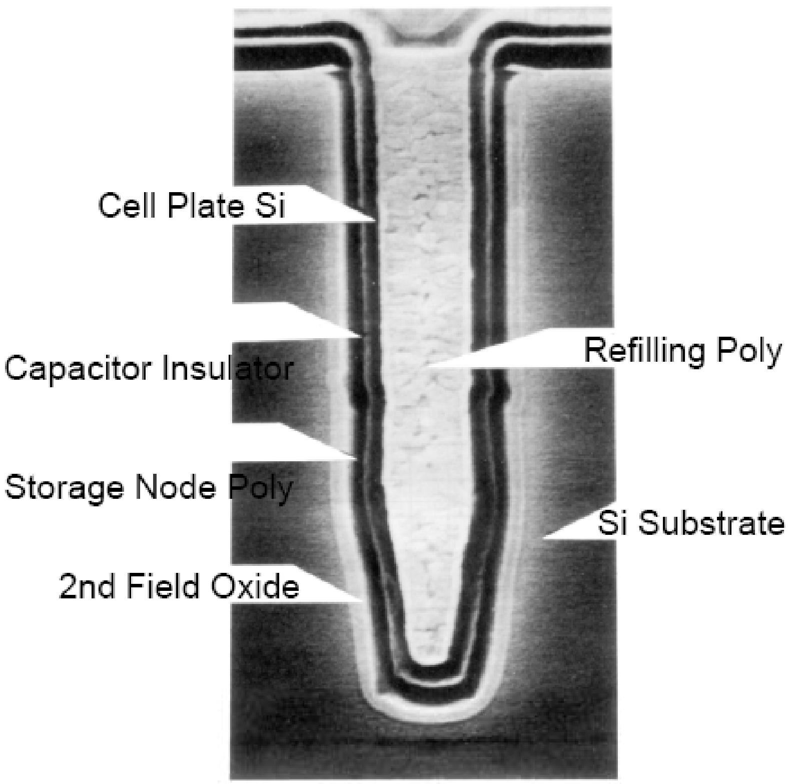


Layout

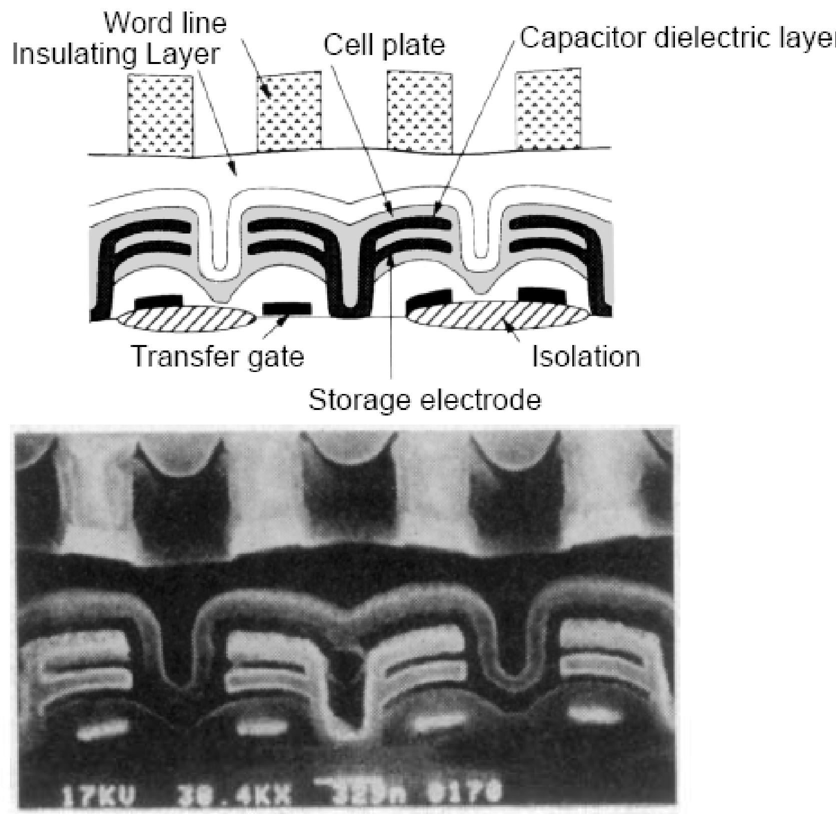
Uses Polysilicon-Diffusion Capacitance

Expensive in Area

Advanced 1T DRAM Cells



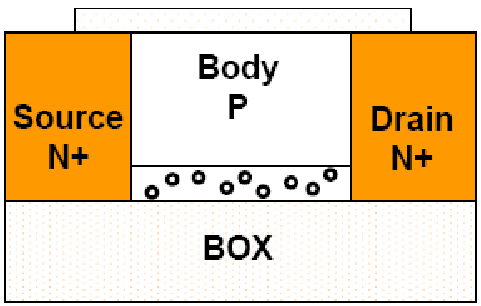
Trench Cell



Stacked-capacitor Cell

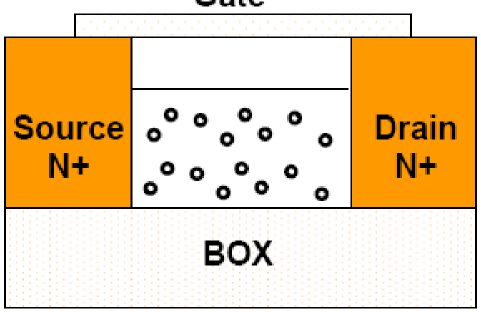
SOI 1T-DRAM Basics

PD SOI MOSFET structure



'0' state

Lack of holes : V_{TH1} ↗ : I_D ↘



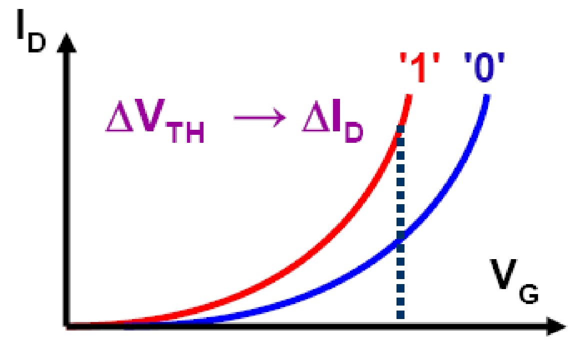
'1' state

Excess of holes : V_{TH1} ↘ : I_D ↗

Z-RAM: Zero-capacitor RAM

Takes advantage of floating body effect

Okhonin S. et al., EDL '02

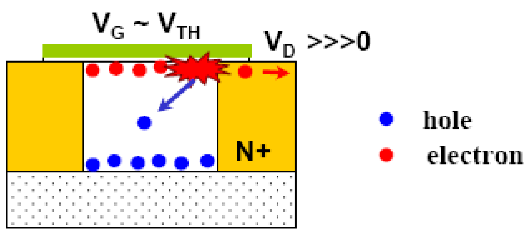


Advantages:

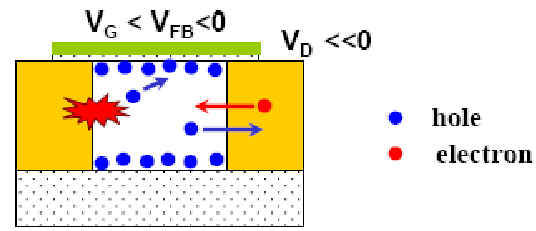
- no capacitor
- smaller surface: easy scaling
- low power
- high speed

Floating Body Effect (FBE) Origin

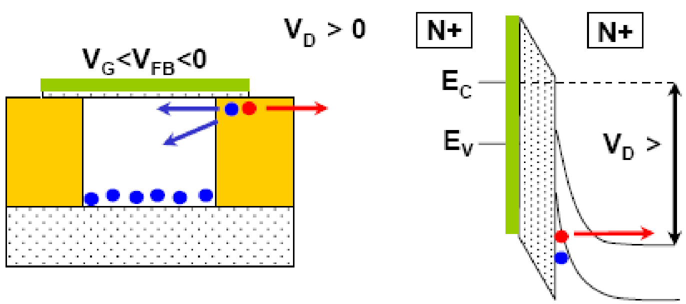
- Impact ionization



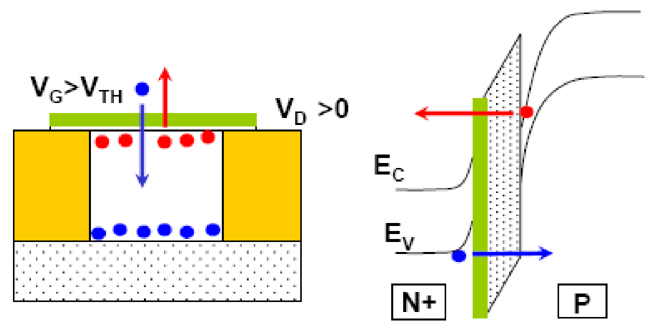
- Bipolar transistor effect



- Band-to-band tunneling (B2B)



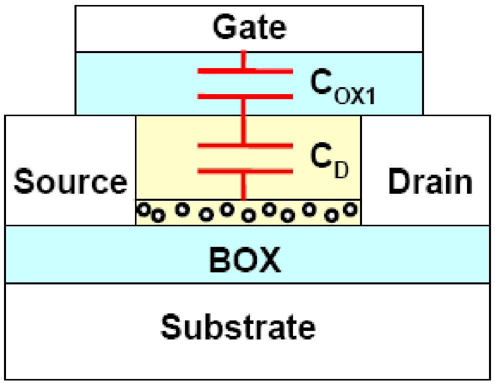
- Gate tunneling current



1T-DRAMs take advantage of these parasitic effects

Scaling and Design Trends

From PD to FD and DG SOI MOSFETs

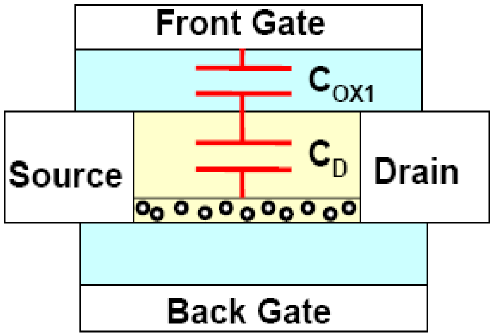


How to increase the threshold voltage shift ΔV_{TH1}?

$$\Delta V_{TH1} \approx \frac{C_D}{C_{OX1}} \cdot \Delta V_B$$

- Increased channel doping – variability issues (RDF)
- Negative back-gate bias
- Higher substrate doping
- Thinner Si film: undoped FD MOSFET

DGFET

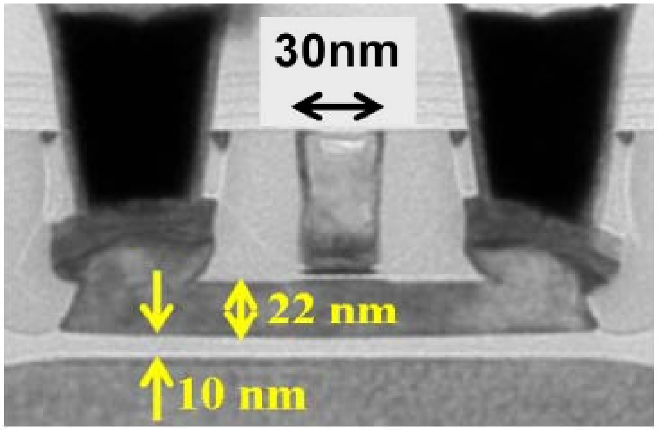


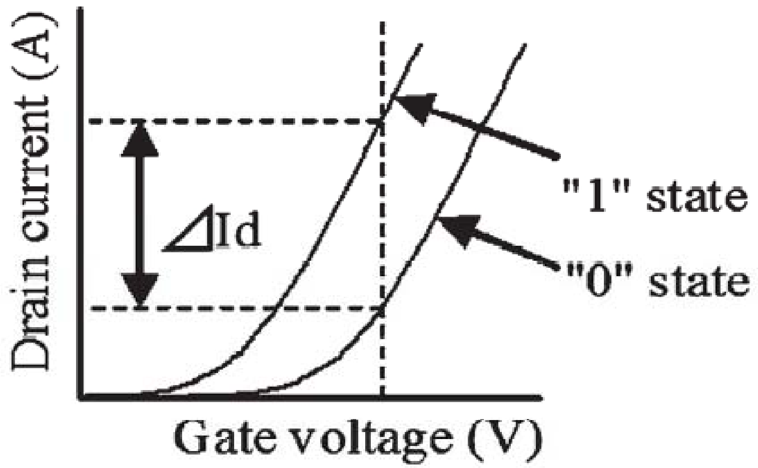
In FD 1T-DRAM, a negative back-gate bias is needed to retain holes.

Then, go to Double-Gate 1T-DRAM !

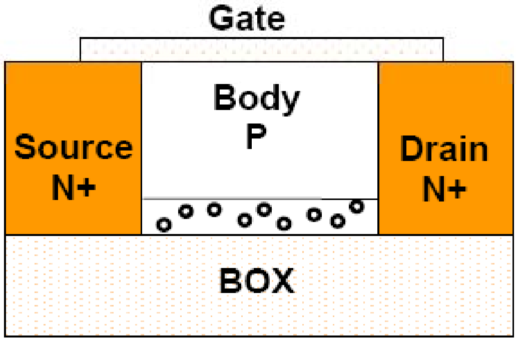
Example of FD SOI 1T-DRAM

Intel & Toshiba





- Prog. Methods: I.I. and FB1
- 45nm, stand alone cell
- LDD and high k dielectric, low doped channel
- T_{BOX}= 10nm (V_{G2}=-2V), T_{SI}= 22nm
- ΔV_{TH} = 400 mV and T_R= 25 ms at 85°C



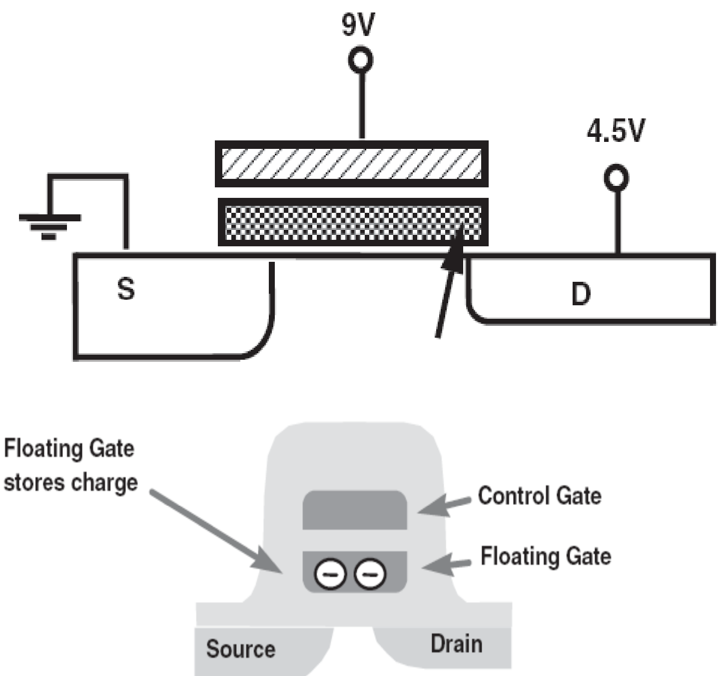
$V_{G2} < V_{FB2} < 0$

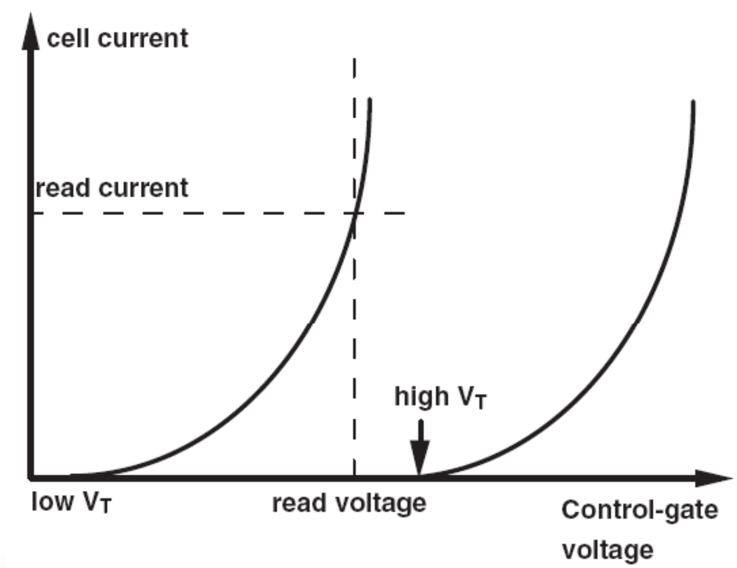
To attract holes

Non-Volatile Memory

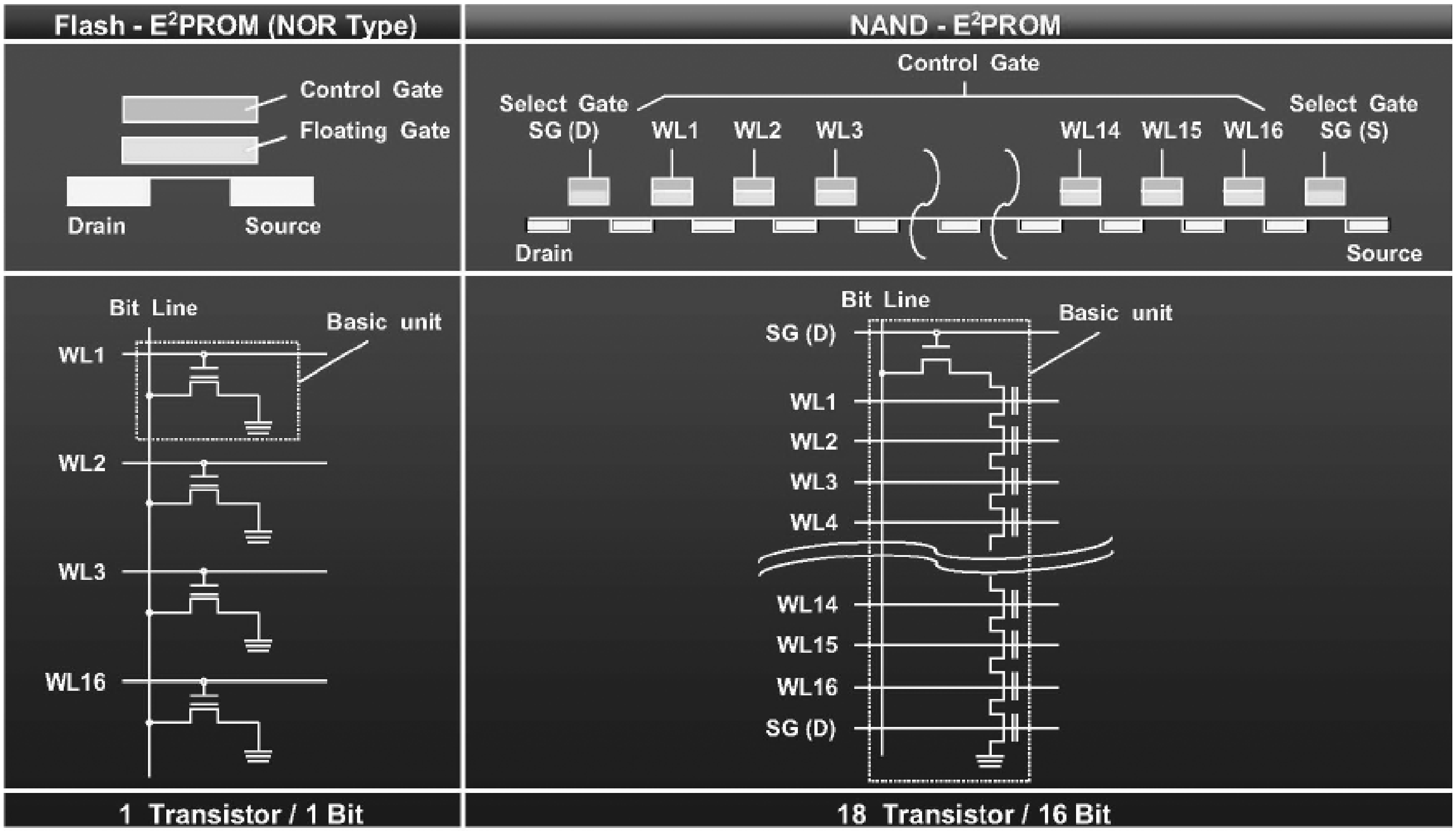
Flash Memory

In practice, a wide variety of memory devices are being used, and depending on the particular device structure, the definition of the *external threshold voltage* has to be refined.





NAND Flash vs. NOR Flash



NAND Flash vs. NOR Flash

Merits of NAND

①High speed programming

②High speed erasing

Merits of NOR

①High speed random access

②Byte programming

Demerits of NAND

①Slow random access

②Byte programming can not be performed

Demerits of NOR

①Slow programming

②Slow speed erasing

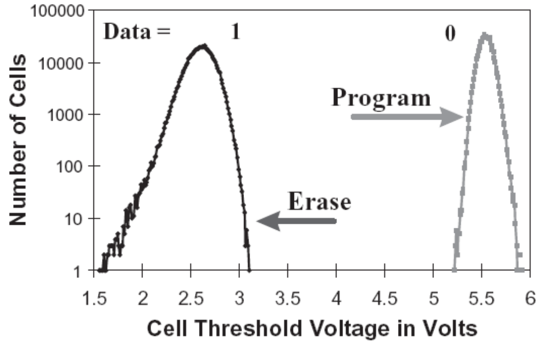
- Applications - (NAND)

・Suitable for Data memory
(Handy terminal,Voice recorder,DSC,Fax modem,etc)

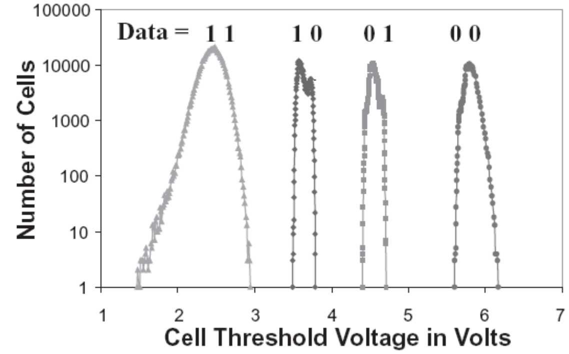
- Applications - (NOR)

・Suitable for replacement of EPROM
・Suitable for control memory
(BIOS,Cellular,HDD,etc)

Multi-Level Cell



1 bit/cell



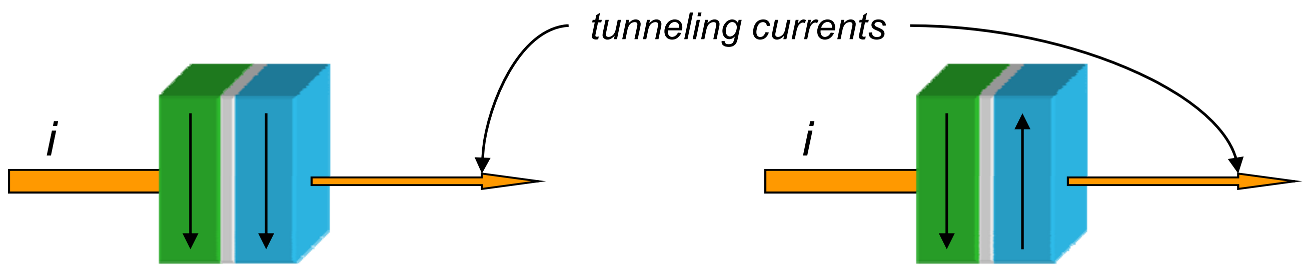
2 bit/cell

TABLE 12.1. Comparison of 1-Bit/Cell and 2-Bit/Cell Product Features

	1-Bit/CellFlash Memory	Intel StrataFlash 2-Bit/Cell Memory	
Density	16 Mbits	32 Mbits	64 Mbits
Read speed	100 ns	120 ns	150 ns
Block size	64 kbytes	128 kbytes	
Architecture	×8	×8 / ×16	
V_{cc} power supply (±10%)	5 V	5 V	
V_{pp} (program/erase voltage)	5 V or 12 V	5 V	
Effective write speed	6 µs/byte	6 µs/byte	
I_{ccr} (read current)	35 mA	55 mA	
$I_{ppw} + I_{ccw}$ (write current)	75 mA	90 mA	
Endurance	100,000 cycles	10,000 cycles	
Operating temperature	Extended	Commercial	

M-RAM – physical principle

- Tunnel MagnetoResistance (TMR)



$R_P \neq R_{AP}$

• *spin conservation in tunneling*

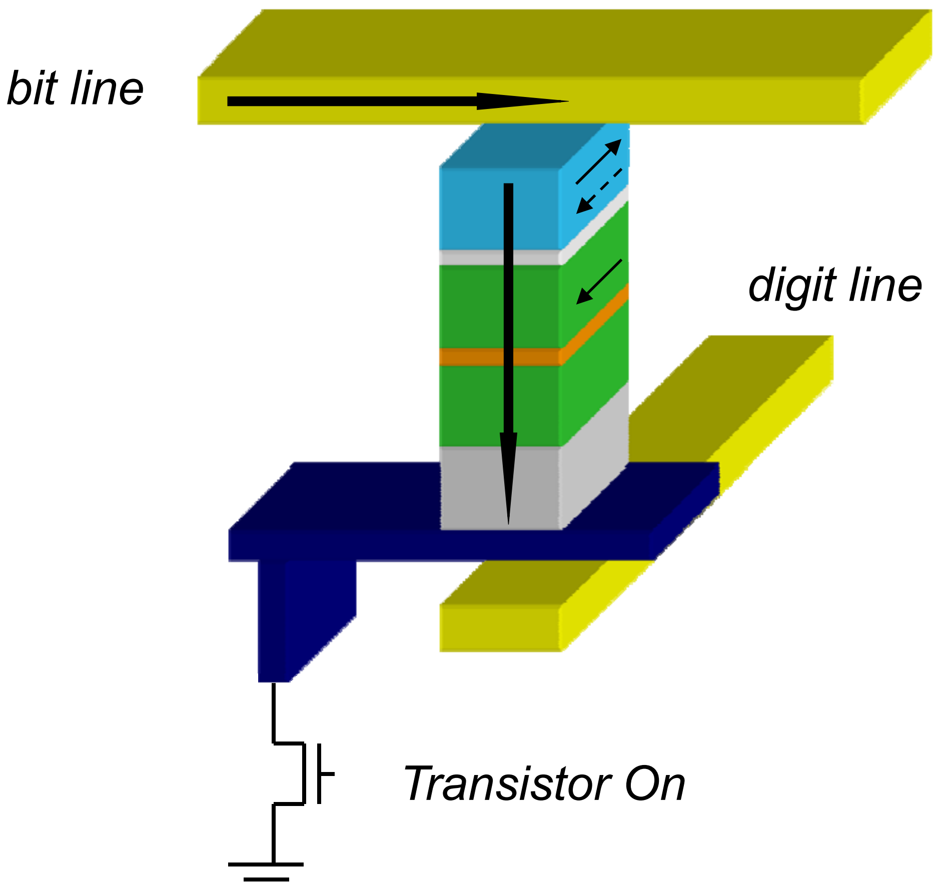
$$P_{L,R} = \frac{N^{\uparrow}_{L,R} - N^{\downarrow}_{L,R}}{N^{\uparrow}_{L,R} + N^{\downarrow}_{L,R}}$$

• *different # of states available for spin-up and spin-down currents in the two different configurations*

Tipically: $R_{AP} > R_P$

$$TMR = \frac{\Delta R}{R_P} = \frac{R_{AP} - R_P}{R_P} = \frac{2P_L P_R}{1 - P_L P_R}$$

M-RAM – real design & operation /1



Read

different orientation of magnetization

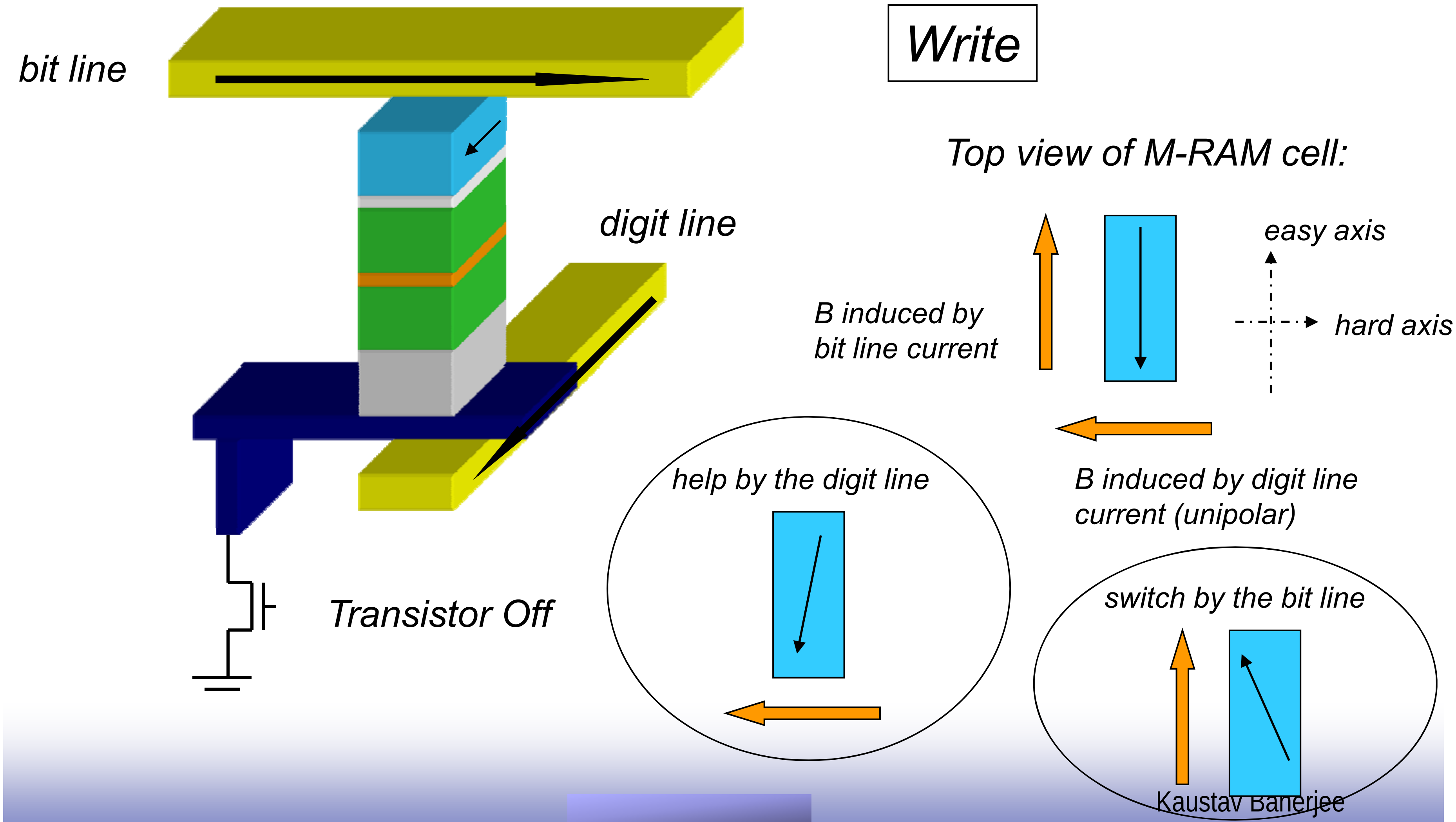
⇓

different current flow

⇓

different voltage read at the CMOS

M-RAM – real design & operation /2



M-RAM – technological issues

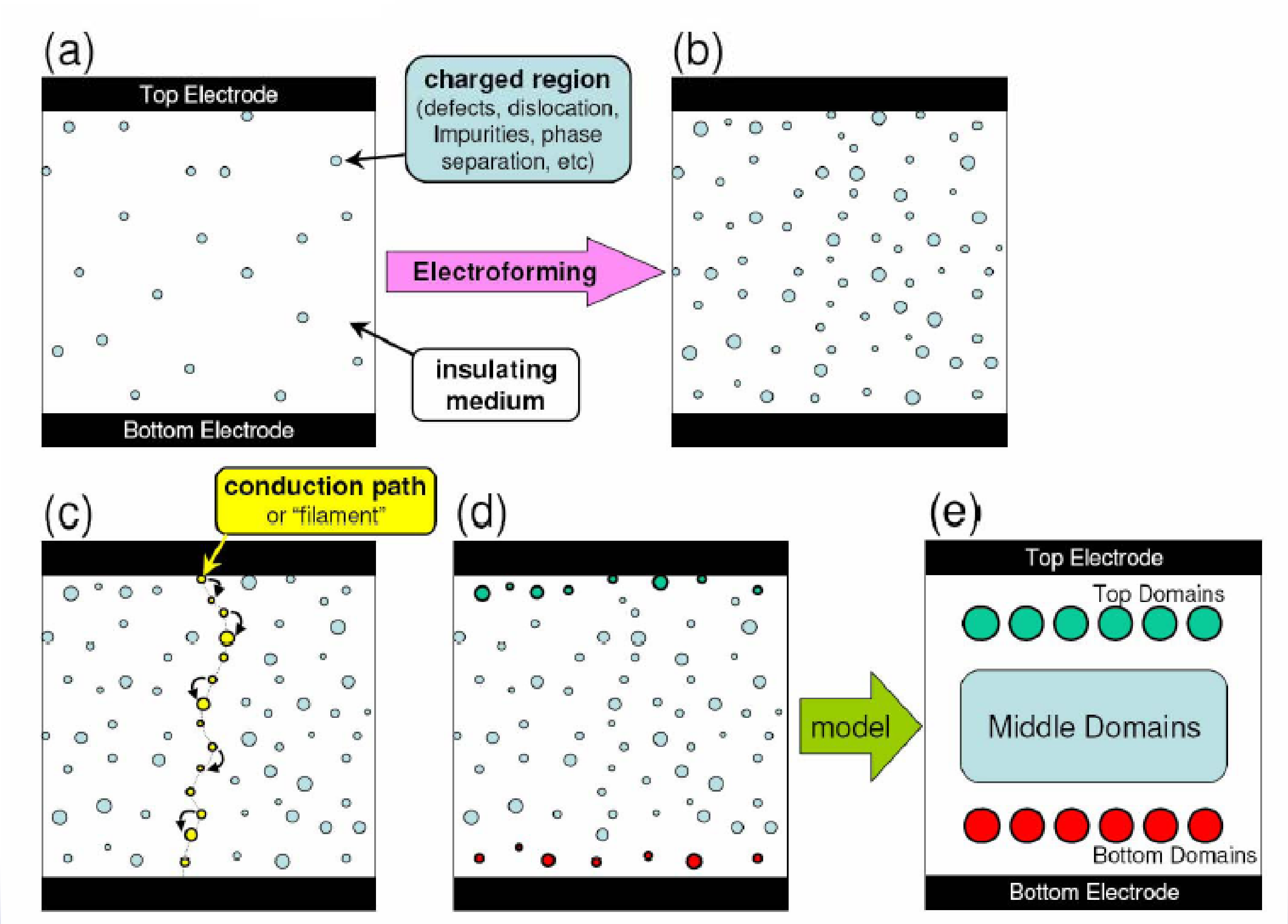
❑ *Accomplished:*

- ❑ sub-micrometric lithography
- ❑ uniform deposition of thin films (<1nm for isolation and RKKY coupling barrier)
- ❑ integration of TMR material with CMOS

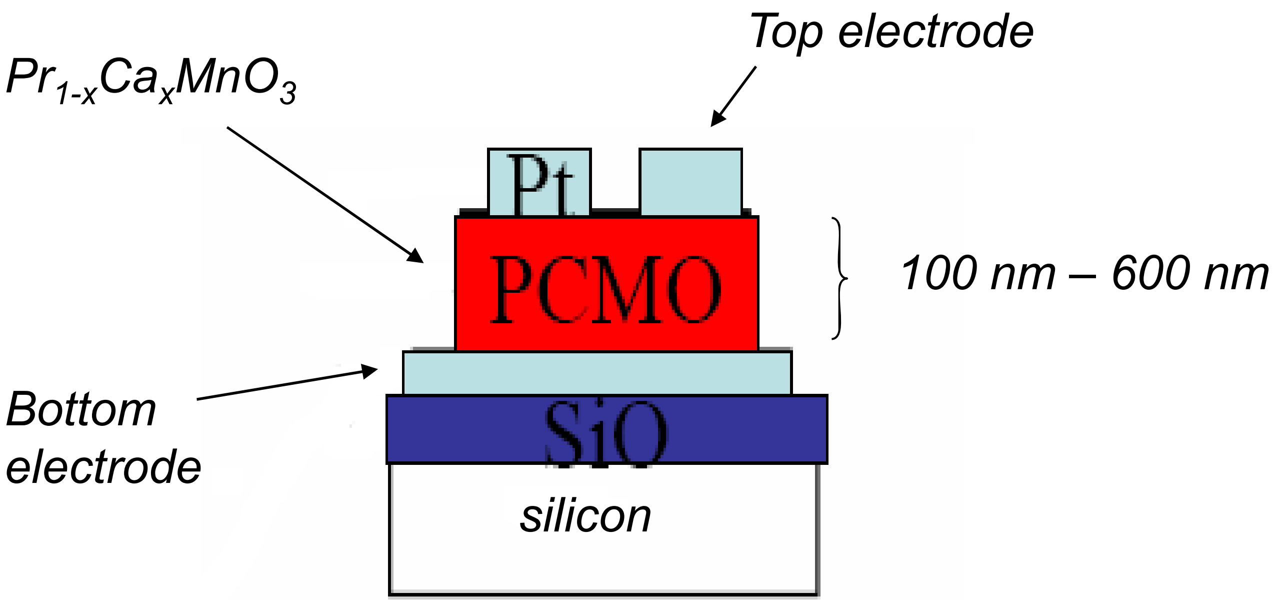
❑ *Challenges in scaling M-RAM techonolgy:*

- ❑ reducing the resistance-area product value (RA) mantaining the MR ratio
- ❑ generating the switching magnetic fields using shrinking metal lines
- ❑ accomodating the increased magnetostatic fields generated by the reduced dimensions

R-RAM – physical principle



R-RAM – simple scheme



- *Size of the top electrode: 100μm in diameter*
- *Typical size of the small domains ~ 10nm*

R-RAM – Basic circuit diagram

High resistance state → "1"

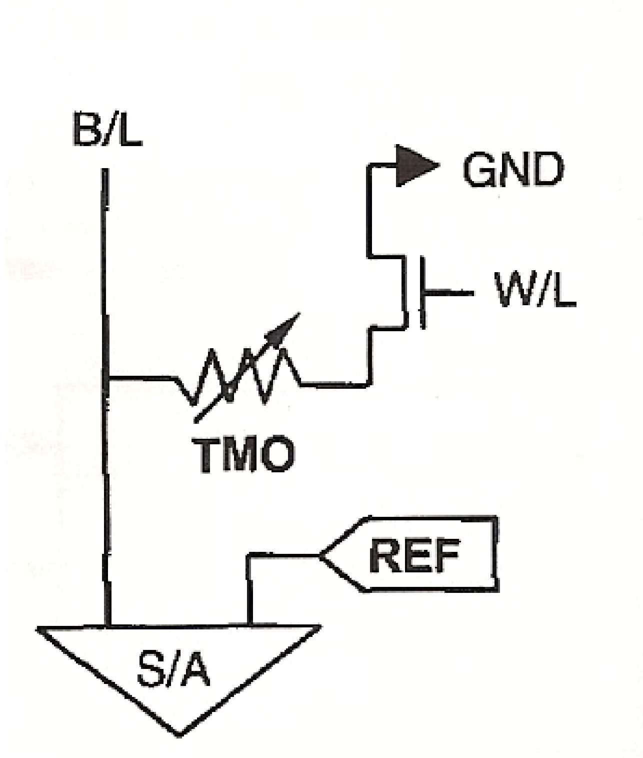
Low resistance state → "0"

If "1" : cell pass-through current lower

If "0" : current higher

Sense amplifier senses the current → determines if 1 or 0 stored

Alt. Voltage sense amplifier



R-RAM – technological aspects

RRAM - promising candidate for next generation non-volatile memory.

- *TMO RRAM integrated with CMOS technology.*
- *Stable high temperature programming possible up to 300 °C.*
- *The memory resistor can be switched between high- and low resistance state over a large number of cycles without memory degradation.*
  (10^6 times of set/reset and 10^{12} times of reading cycles confirmed)
- *Cell resistance can be read without affecting stored data.*