

ECE 225
High Speed Digital IC Design
Lecture 2

Discussion of Project Topics

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Project Topics....with focus on Circuit Design

1. Nanometer Scale CMOS Design Issues:

- a. Variation/error tolerant design
- b. Aging resilient design
- c. Ultra low power design under noise margin, performance and area considerations:
- d. **Ultra low-voltage design/Sub-threshold circuit design**

2. Emerging Technologies for VLSI and More-than-Moore Technologies:

- a. Non-classical CMOS – SOI, FinFET, GAAFET.
- b. Non-Si Devices – CNFET, NWFET, Graphene-FET, NEMFET, SpinFET.
- c. Novel memory technologies like MRAM, FRAM, STT-RAM, PCM etc.
- d. **Sub-kT/q devices – Tunnel FETs, IMOS, Fe-FET, NEMFET etc.**
- e. **Renewable energy with Nanoelectronics: energy conversion, storage, scavenging**
- f. **Bioelectronics: biosensors, drug delivery using nanotechnologies**

3. Interconnect System and Passive Device Design:

- a. Variation aware design – signal, clocking, P/G (power / ground) Networks.
- b. Interconnect variations: parasitic (R,L,C) extraction, modeling and optimization
- c. Modeling of VHF (Very High Frequency) signals....substrate effects.
- d. Optimal on-chip inductor design
- e. **Emerging interconnect technologies: Carbon nanotubes, graphene nanoribbons, optical, RF interconnects**
- f. **Interconnects design and modeling for 3-D ICs: TSV design, alternate interconnection schemes (via C or L coupling)**

Project Deadlines....

- ❑ Preliminary report due: Feb 7 (~ 2 pages)
 - At least complete literature review and identify problems to be addressed within a given topic.
 - Show some initial analysis....if possible
 - Preliminary presentations of proposed projects (early Feb...)
- ❑ Final project presentations: during the last week of class (~ 30 mins per student)
- ❑ Final project report due in March (end of last week of class--- ~ March 19)