ECE 225
High-Speed Digital IC Design

Lecture 6

Interconnect Technology and Scaling Issues-2

(Inductive Effects, High-Frequency Effects, and Voltage Drop Issues)

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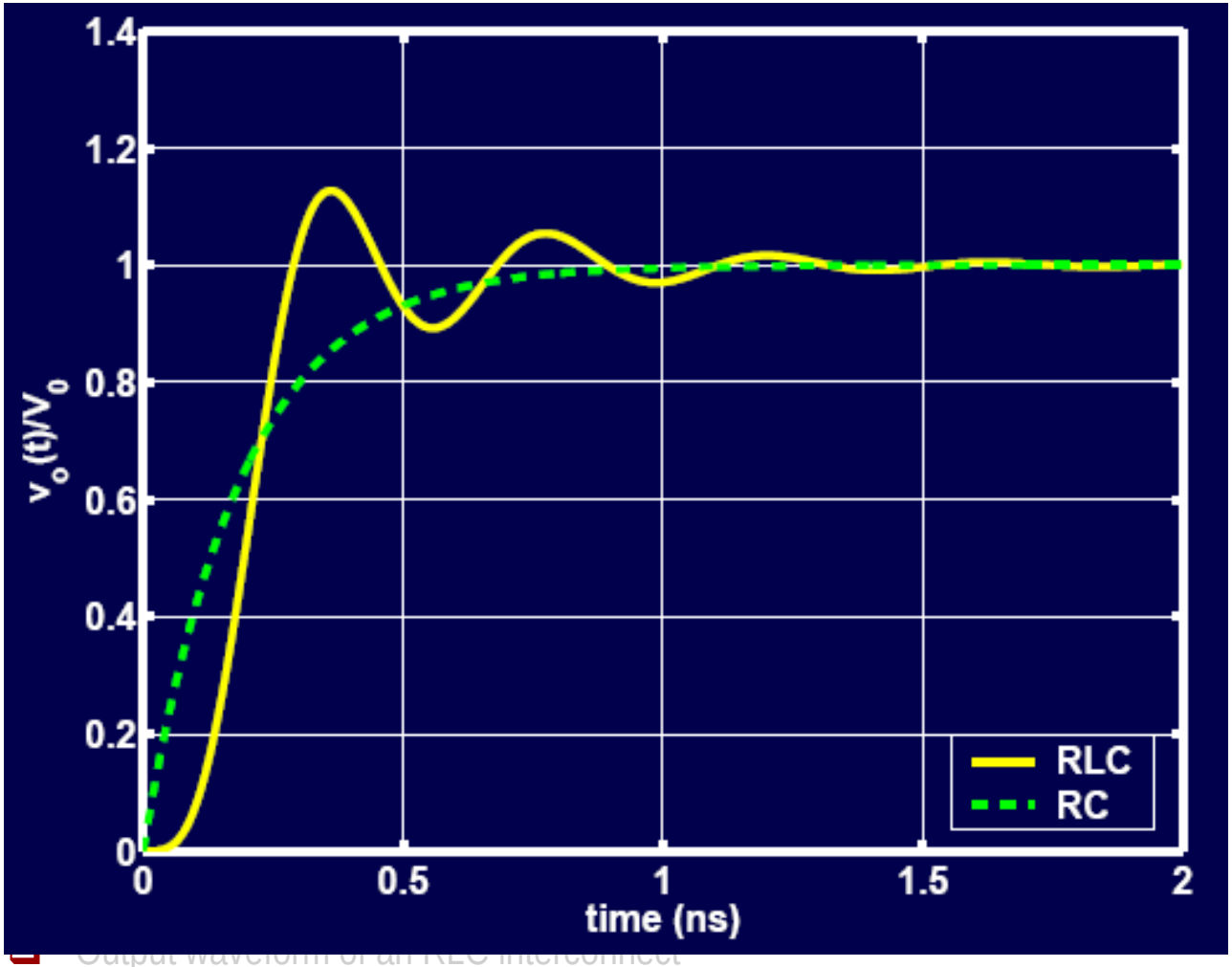
On-Chip Inductance Effects

K. Banerjee and A. Mehrotra, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 21, No. 8, pp. 904-915, August 2002.

On-Chip Inductance Effects

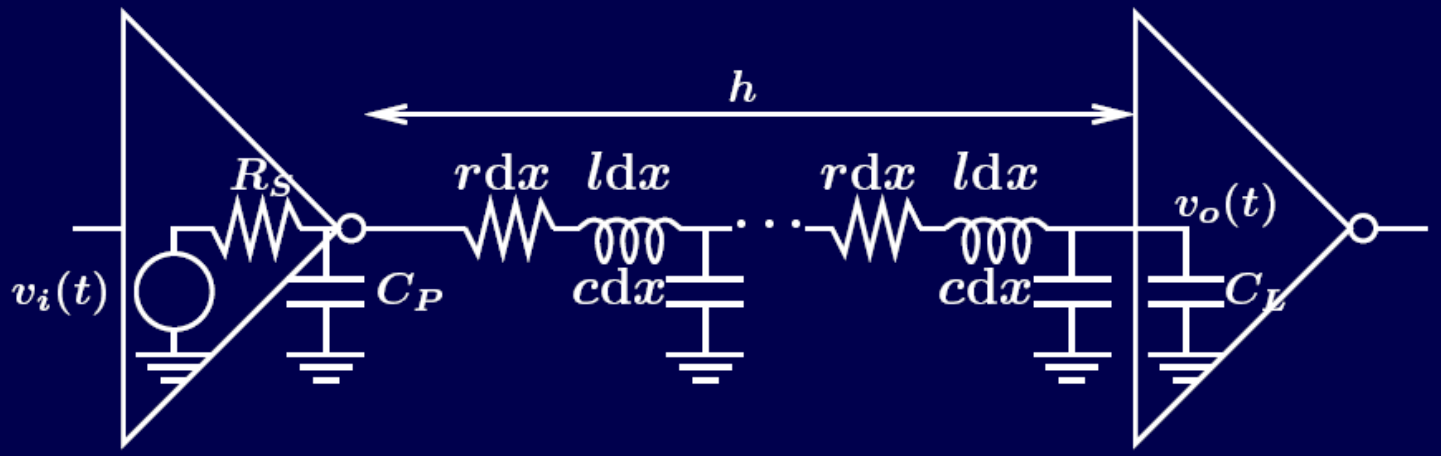
- Increasing clock speeds and decreasing rise times cause inductive effects
- Low resistance wires more susceptible to inductive effects
  - Global wires that are usually wide
  - introduction of Cu: lower resistivity
- Line inductance depends on current return path
  - strongly dependent on circuit topology
  - difficult to extract accurately
  - large variations

Step Response of an RLC Line



- Output waveform of an RLC interconnect

Time-Domain Response of RLC Segment



$$H(s) = \frac{1}{[1+sR_S(C_P+C_L)]\cosh(\theta)+\left[\frac{R_S}{Z_0}+sC_LZ_0+s^2R_SC_PC_LZ_0\right]\sinh(\theta)}$$

$$\approx \frac{1}{1 + sb_1 + s^2b_2 + s^3b_3 + s^4b_4}$$

$$Z_0 = \sqrt{\frac{r+sl}{sc}} \qquad \theta = \sqrt{(r+sl)sch}$$

Critical Inductance

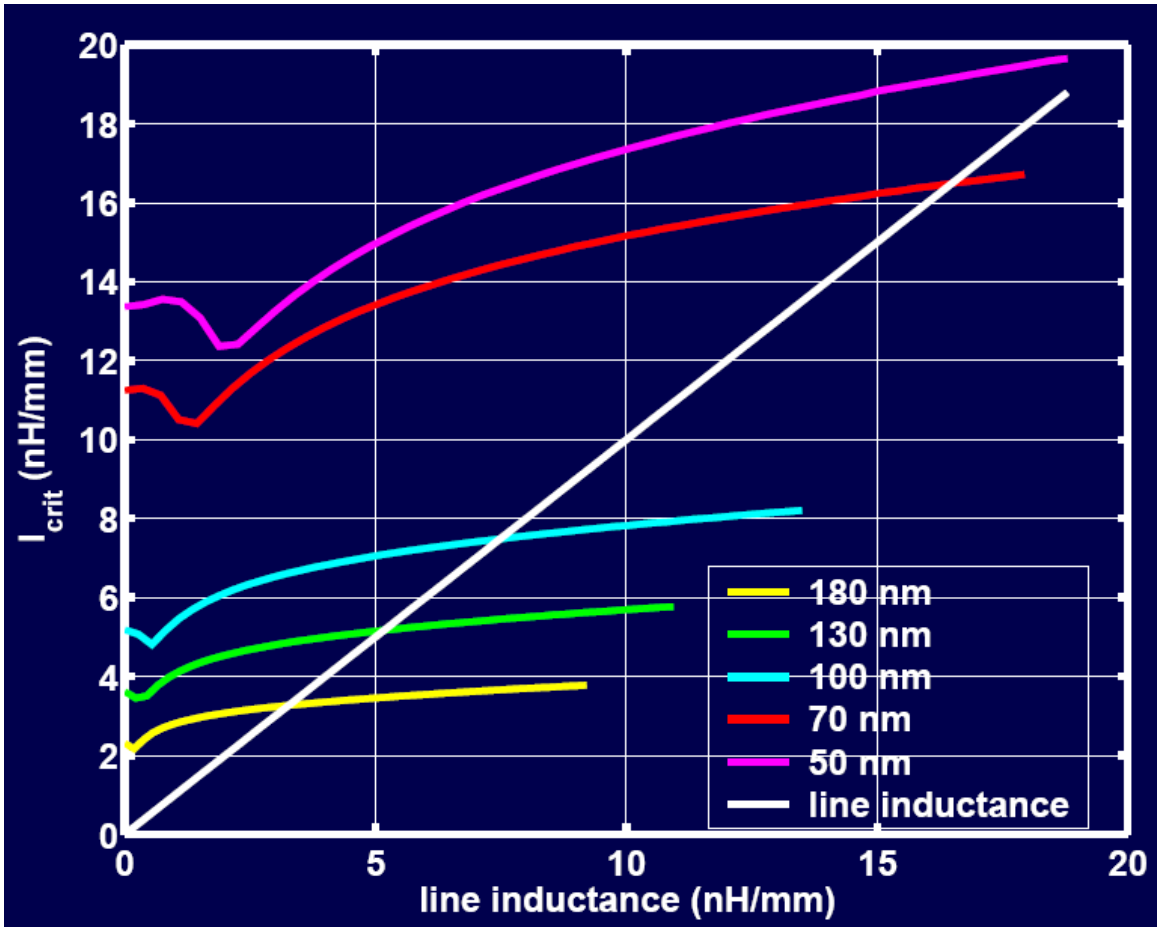
- Second order Padé expansion of $H(s)$

$$H(s) \approx \frac{1}{1 + b_1 s + b_2 s^2}$$

- System overdamped, critically damped or underdamped when $b_1^2 - 4b_2$ is $>, =, < 0$.
- At optimum buffer size and interconnect length, find l_{crit} for which the system is critically damped.
- For l $<, =, >$ l_{crit}, the system is overdamped, critically damped or underdamped

Impact of Scaling: Case 1

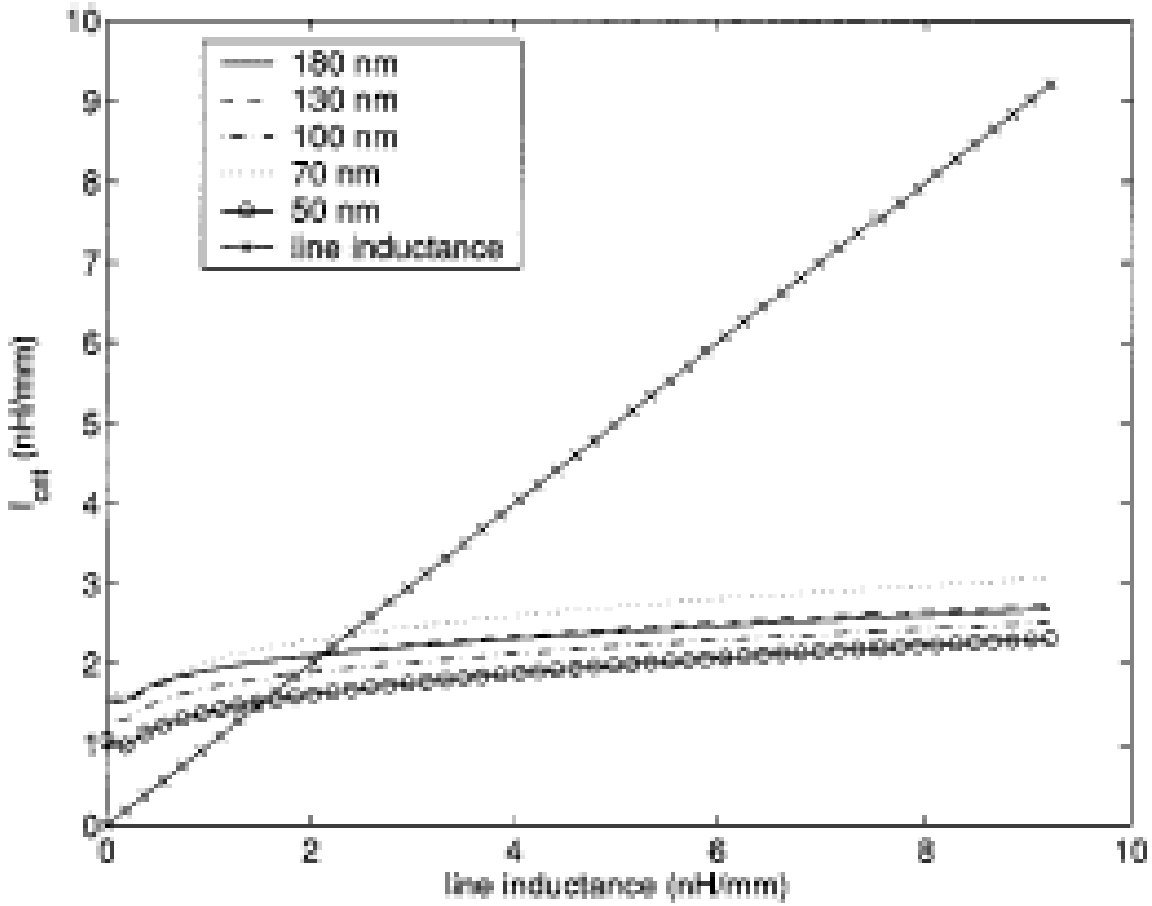
Minimum Width Global Wires



- As technology scales, $l < l_{crit}$ over larger range of line inductance
- Hence, impact of inductance reduces with scaling

Impact of scaling: Case 2

Unscaled Global Wires



- As technology scales, $l > l_{crit}$ over larger range of line inductance
- Hence, impact of inductance increases with scaling

High-Frequency Issues

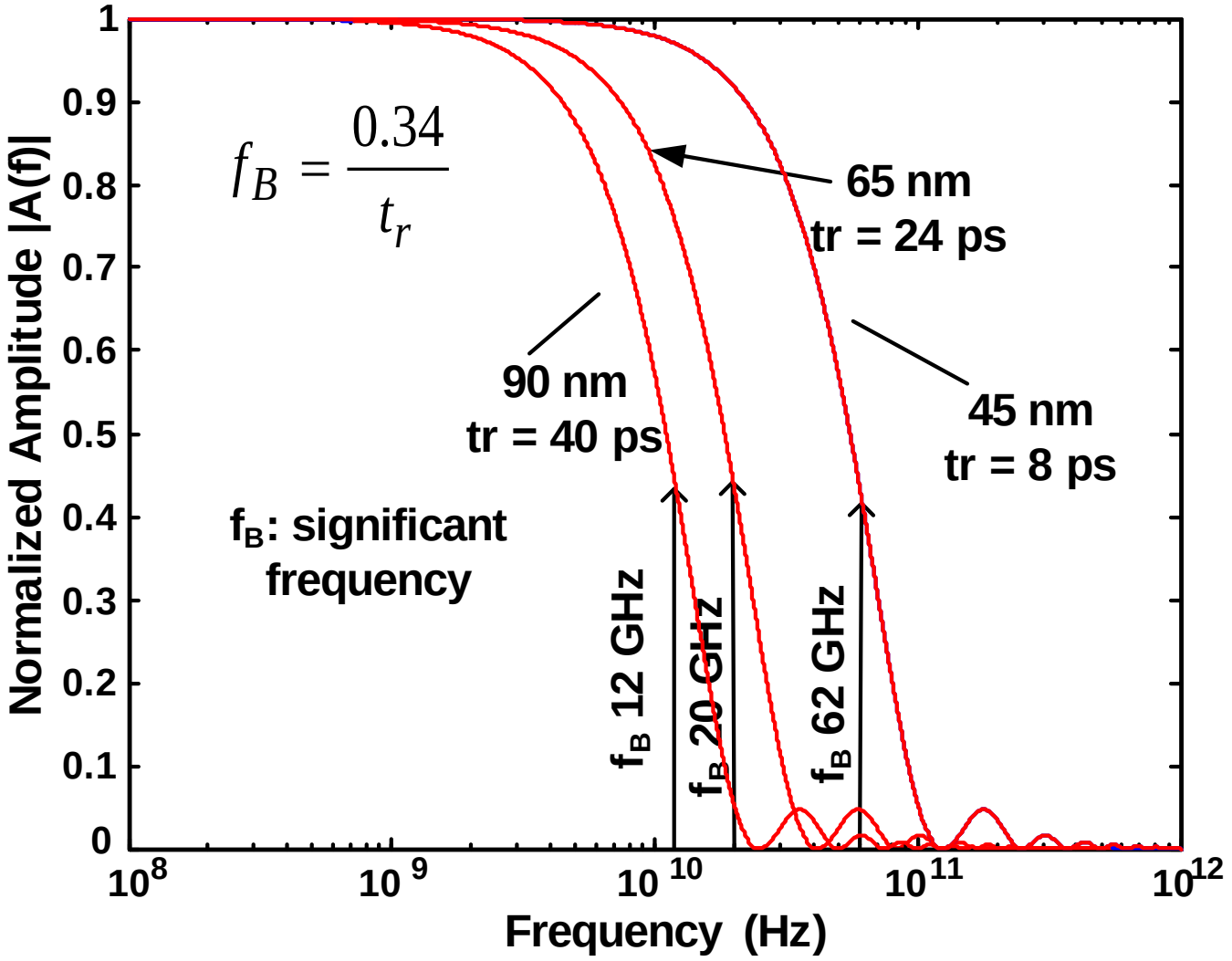
K. Banerjee, S. Im and N. Srivastava, Proc. Advanced Metallization Conf., 2005.

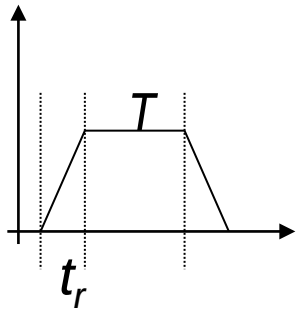
S. Suaya, R. Escovar, S. Ortiz, K. Banerjee and N. Srivastava, Proc. Advanced Metallization Conf., 2006.

High-Frequency Effects

- Frequency of signals on interconnects is rising rapidly
- Frequency dependent impedance extraction is a major hurdle
  - Field solvers are unable to handle the complexity of VLSI interconnects
- Need to develop models for interconnect geometry dependent calculation of high frequency impedance

Signal Frequency on Interconnects





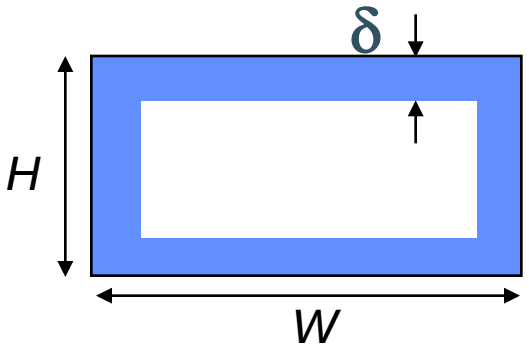
Digital signal composed of various frequency components.

Significant Frequency:

Frequency used for interconnect analysis

Frequency Dependence of R

- At high enough frequencies, R can increase due to *skin effect*
- Current flow constrained in a thin layer along the surface of the conductor: R increases
- The current falls off exponentially with depth into the interconnect
- Skin depth, δ is defined as the depth at which current falls of to a value of 1/e of its nominal value



$$\delta = \sqrt{\frac{\rho}{\pi f \mu}}$$

μ is the permeability of the surrounding dielectric

Resistance per unit length:

$$r(f) = \frac{\sqrt{\pi f \mu \rho}}{2(H+W)}, \quad for \ W, H >> \delta$$

Skin Effect

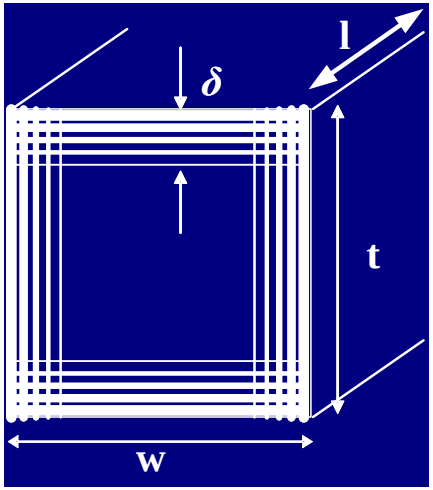
- Onset of skin effect: at $f=f_s$, δ =1/2 x smallest dimension

$$f_s = \frac{4\rho}{\pi\mu\left(\min\left(W,H\right)\right)^2}$$

- For Cu wires:

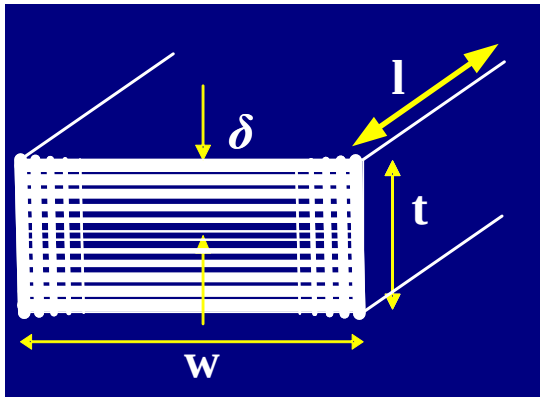
Freq	1 GHZ	5 GHZ	10 GHZ	15 GHZ	20 GHZ
Skin depth (μm)	2.08	0.93	0.66	0.53	0.46

Skin and Proximity Effects



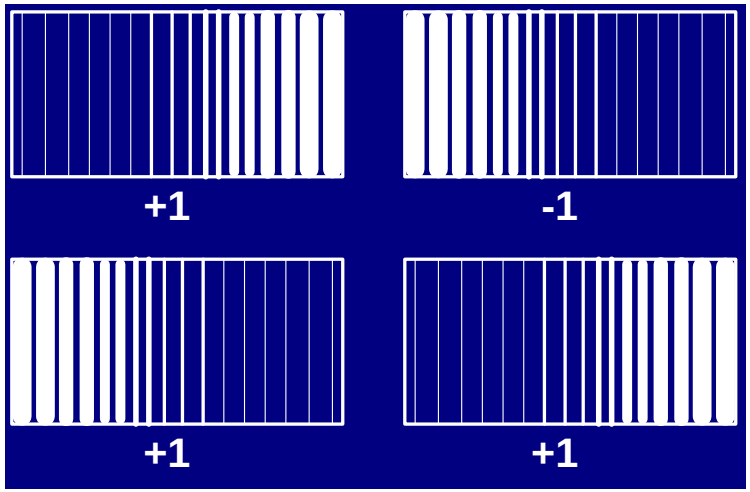
Isolated Wire 5um x 5um

Skin Effect in Isolated Conductors

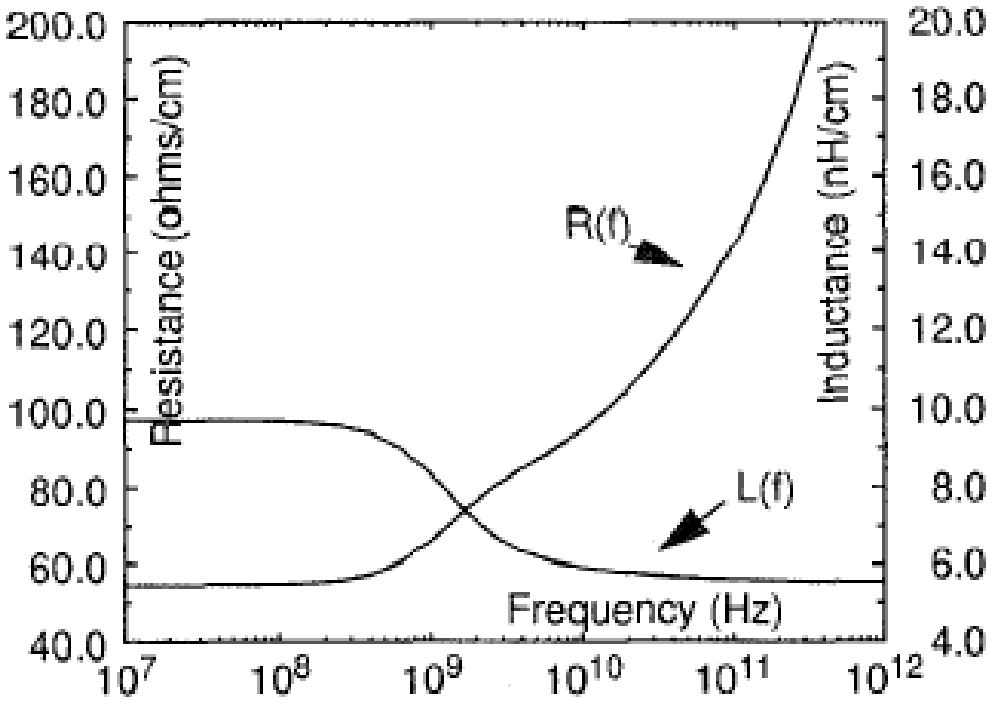


Isolated Wire 5um x 1um

Proximity Effect in Coupled Conductors



Frequency Dependence of R and L

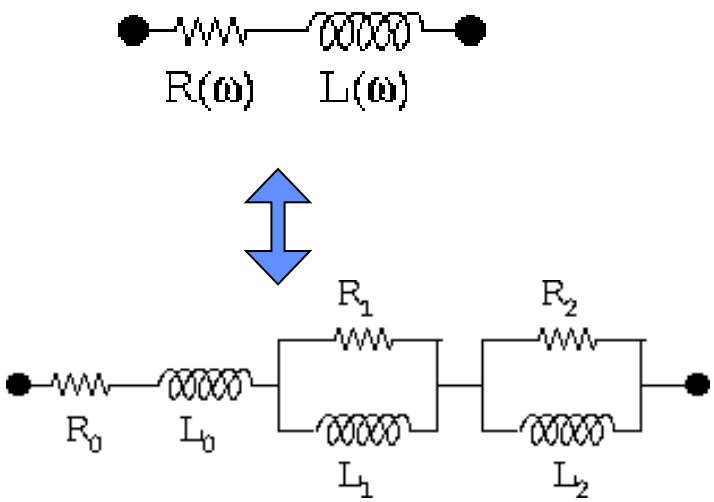


B. Krauter and S. Mehrotra, DAC, 1998.

- Resistance increases due to skin effect
- For lower frequencies, current return path is distributed between all ground lines---thus loop inductance is higher and return path resistance is smaller…..
- For higher frequencies, current returns through closest ground paths---thus loop area is smaller, hence loop inductance reduces and return path resistance increases

Modeling Frequency Dependent Behavior

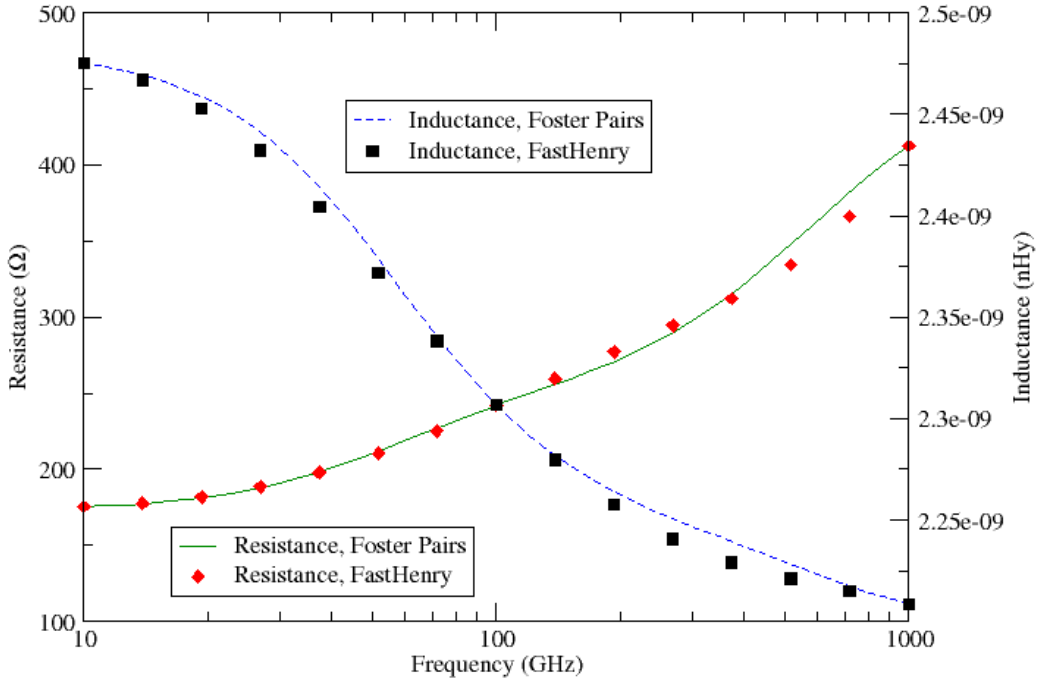
Replacing $R(\omega), L(\omega)$ with Foster Pairs



Note that at smaller frequencies L_1 ($Z=j\omega L$) will short R_1

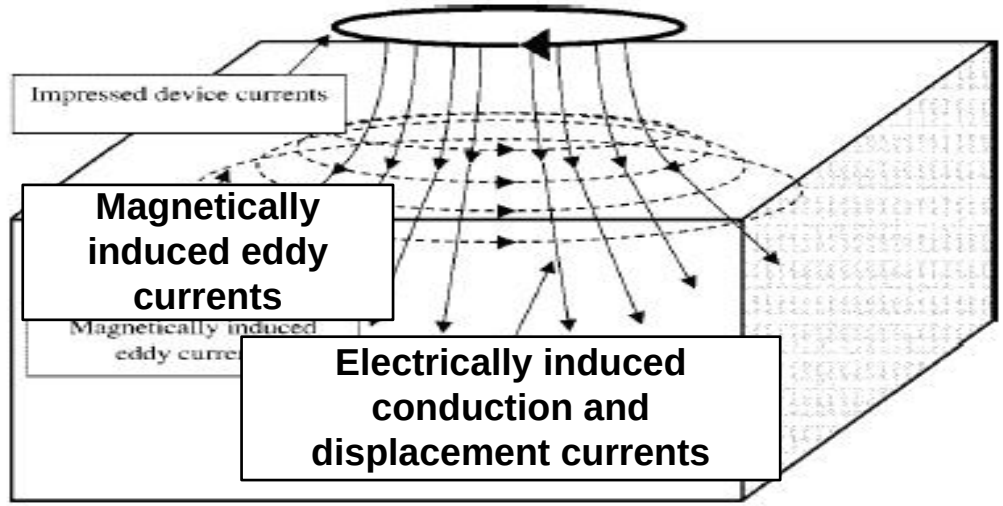
R_0 and $L_0+L_1+L_2$ are low-frequency values of R and L

At higher frequencies some current flows through R_1 and R_2, hence R increases with frequency and effective inductance decreases



Suaya et al., Advanced Metallization Conf. 2006

Substrate Effects



Impacts interconnect impedance extraction

A. M. Niknejad and R. G. Meyer, IEEE Trans. on Microwave Theory and Techniques, 2001

Voltage Drop Effects in Power Distribution Networks

A. H. Ajami, K. Banerjee and M. Pedram, International Journal of Analog Integrated Circuits and Signal Processing, Vol. 42, No. 3, pp. 277-290, Springer, 2005.

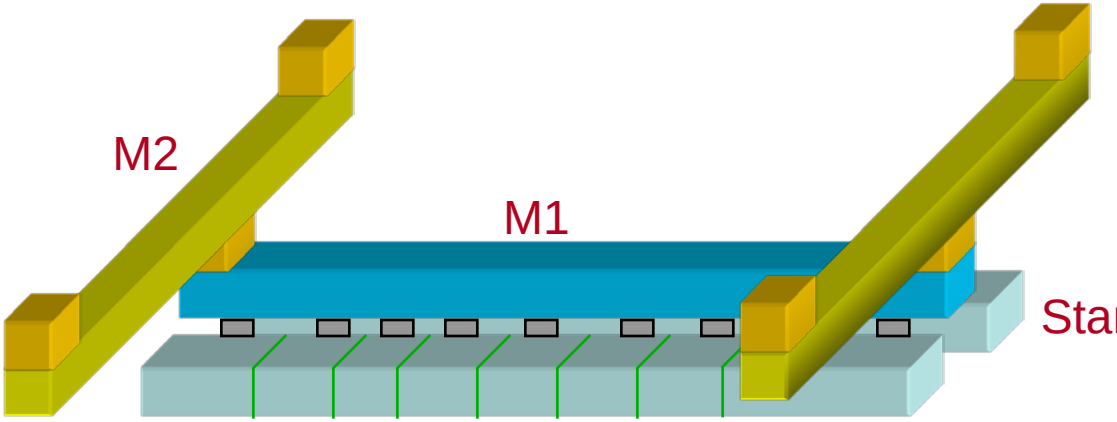
Voltage Drop Effects

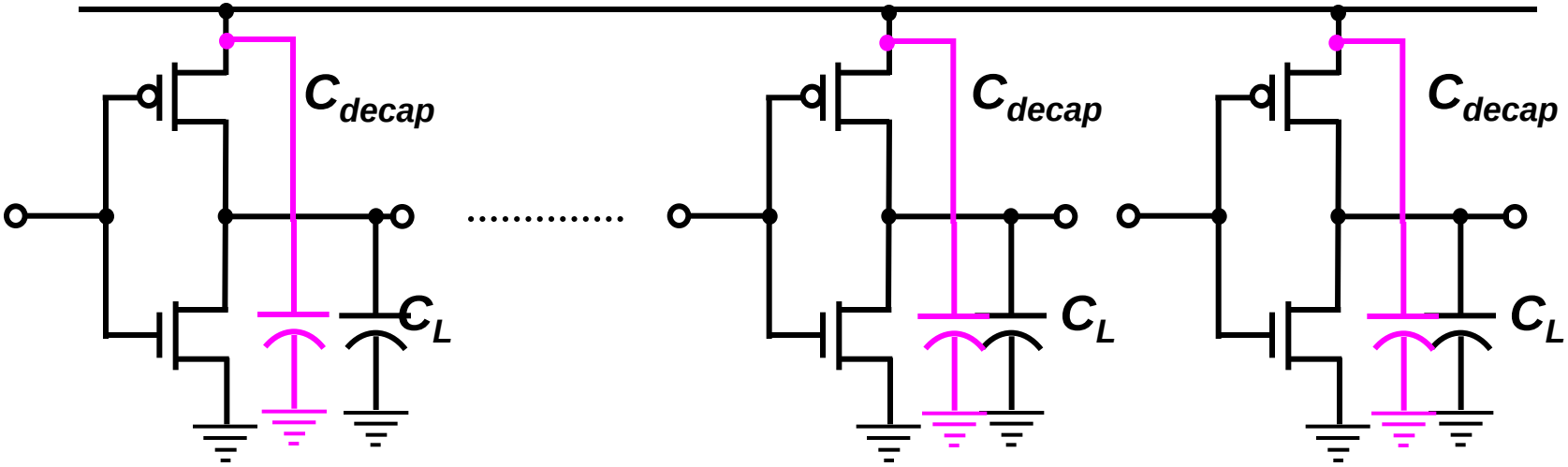
- Voltage-drop is an inseparable aspect of DSM power distribution network (PDN)
  - resistive voltage drop ΔV (on-chip resistance)
  - switching noise, $L di/dt$ (off-chip inductance)
- Degrades device switching speed and *DC* noise margins
- Can cause functional failure in dynamic logic and timing violation in static logic
- 10% voltage-drop → 8% increase in device propagation delay (0.18μm tech.)

Challenges in P/G Network Design

- Satisfying the electromigration (EM) rules for each power routing segment
- Minimizing the area consumed by PDN
- Limiting the worst-case voltage-drop (~10% of *Vdd* for current technology)
  - Power network wire-sizing (↑ routing area)
  - Decoupling-cap insertion (↑ substrate area)

Local Power Distribution



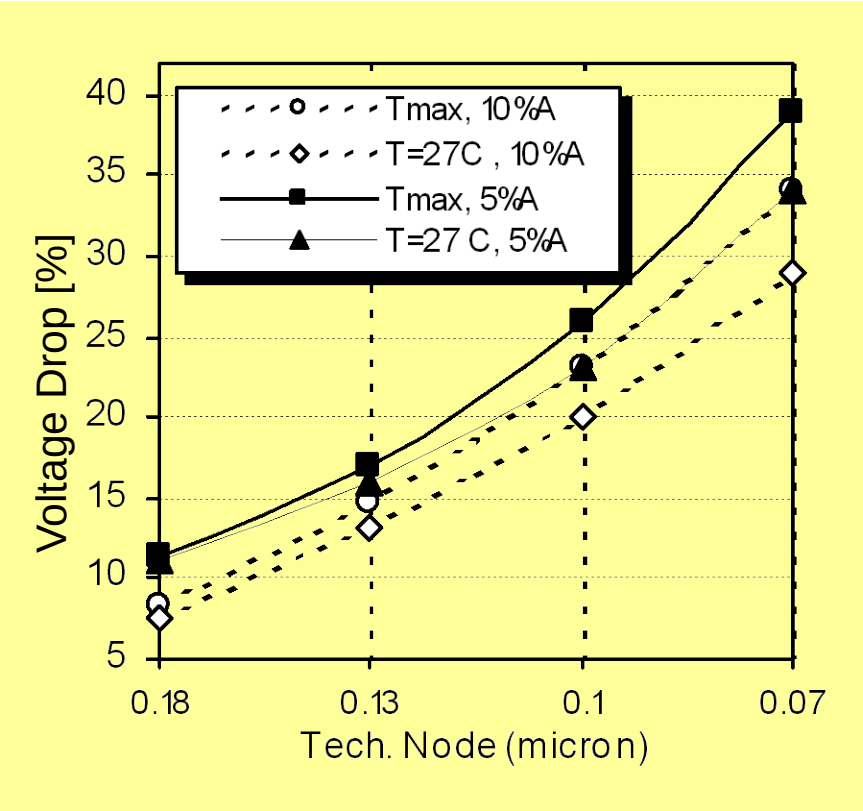


Technology Scaling Impacts

- Scaling of line dimension (*R, L, C*)
- Scaling of chip frequency, power, and # of power pads
- Interconnect thermal effects
  - Electromigration rules
  - R
- Thin-film scattering and barrier thickness effects in DSM interconnects
  - R

Global/Semi-global PDN IR-Drop

Allocation of 5% and 10% of the routing area for wire sizing to minimize the voltage-drop:

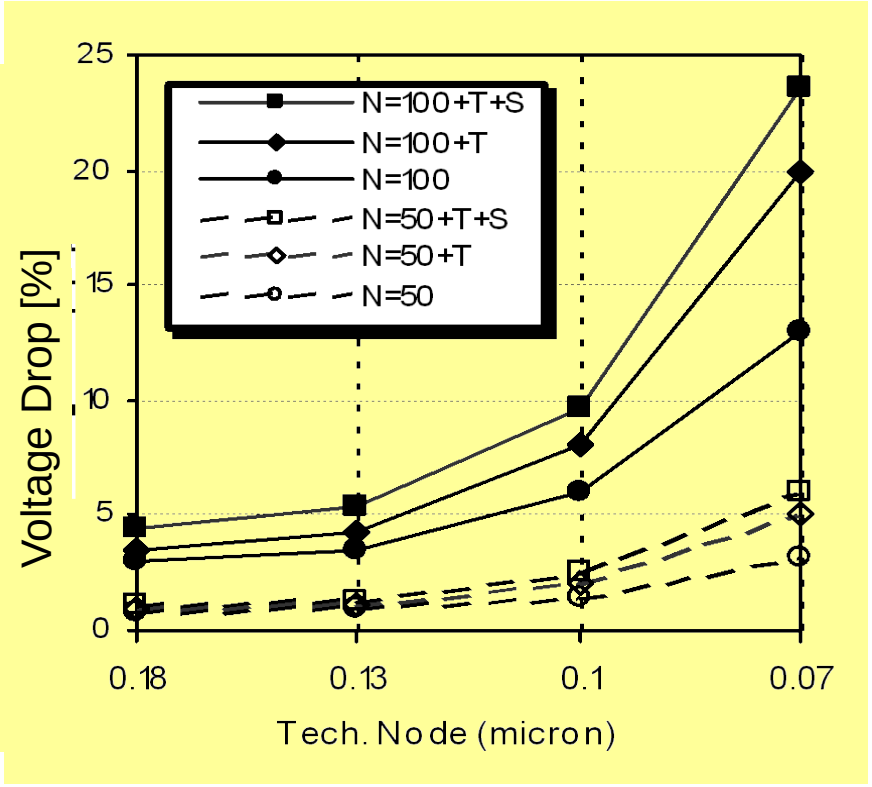


Voltage-drop increases rapidly with technology scaling….

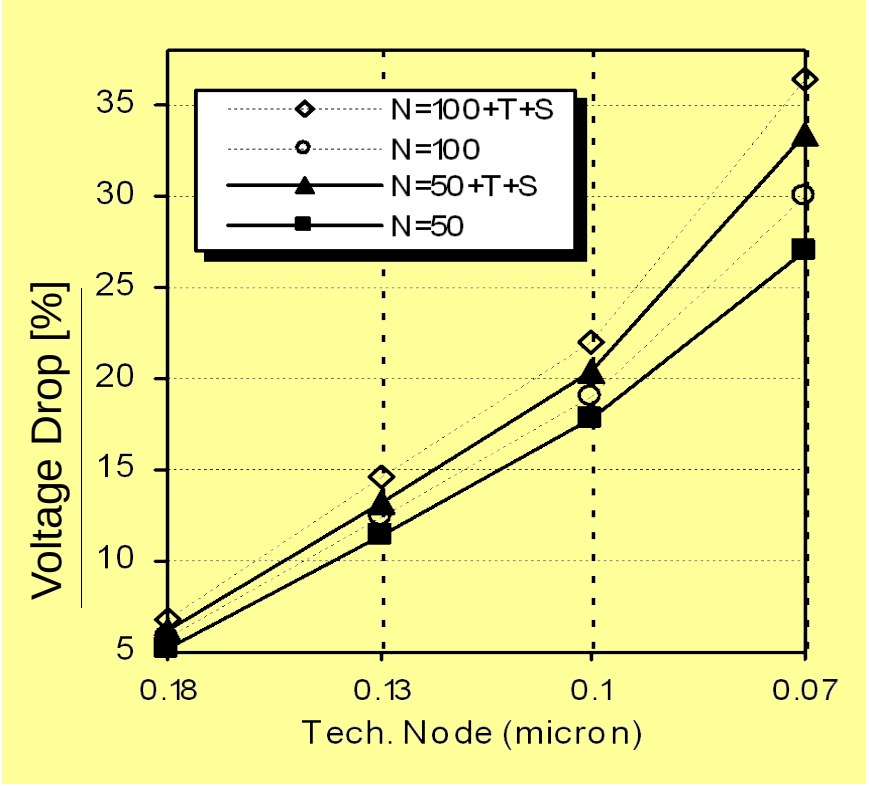
Interconnect temperature has a major impact on the voltage-drop of global segments…..

Full Chip IR-Drop

Local worst-case IR-Drop
for 50 and 100 switching cells

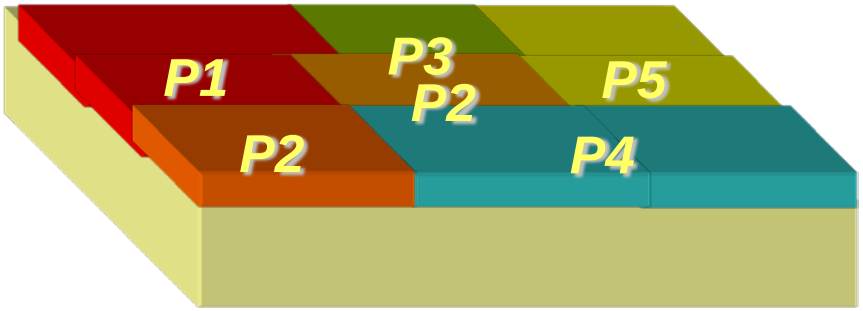


Total chip worst-case IR-Drop
10% routing, 5% chip area



T– considering temperature effect **S—considering thin-film effects**

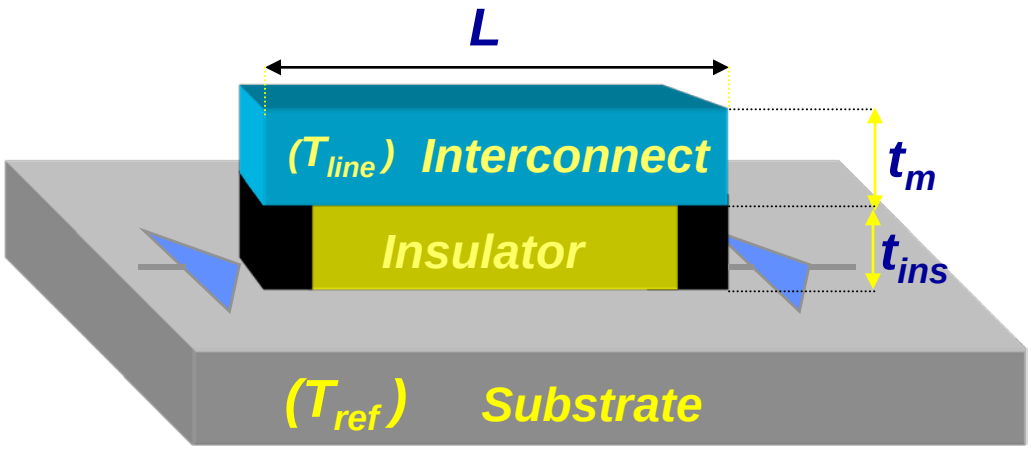
Within-Die Temperature Variations

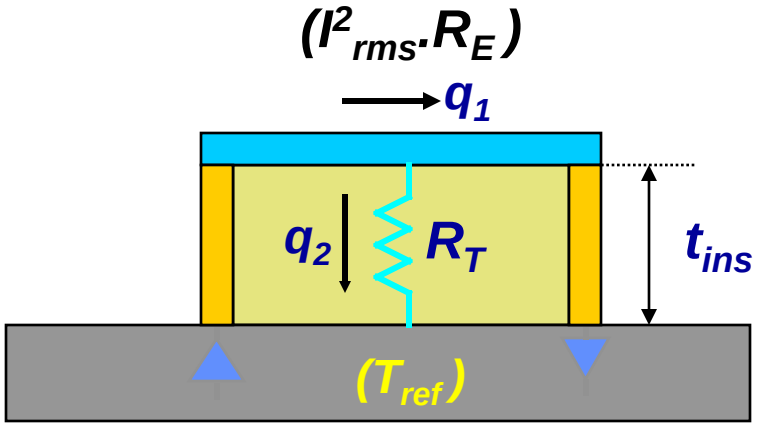


- Substrate power generation distribution is generally non-uniform
  - Functional block clock gating
  - System-level power management
  - Non-uniform distribution of gate sizing and switching activities in different blocks
- Substrate thermal profile is non-uniform
  - Thermal time constant is of the order of *ms*
  - Switching activities at the block level are more important
  - Introduces non-uniformity in the global interconnect thermal profile

Interconnect Thermal Profile

A. Ajami et al., DAC 2001





$$\frac{d^2T_{line}}{dx^2} = -\frac{Q}{k_m}$$

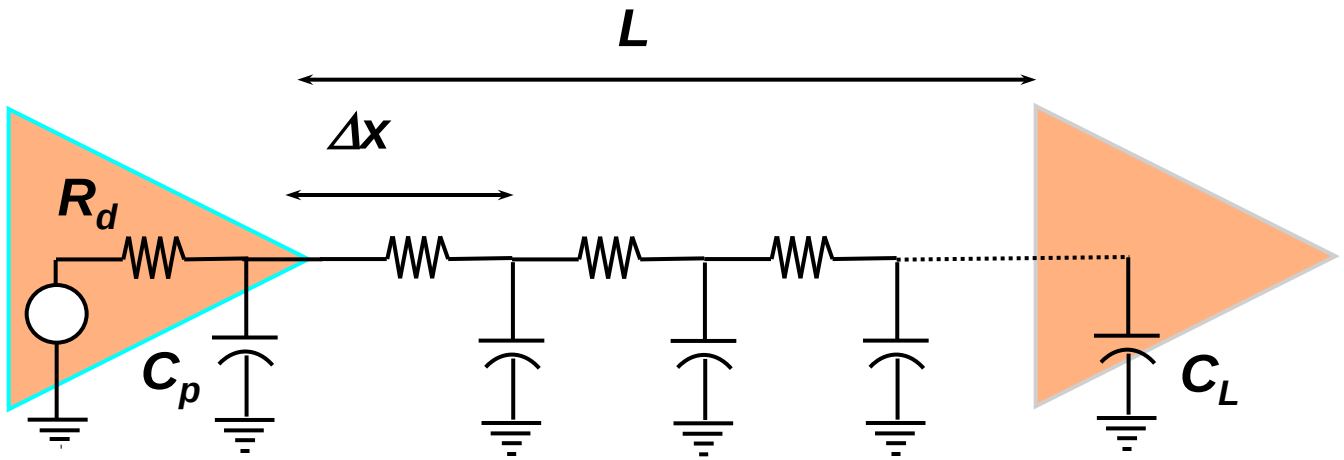
$$Q = q_1 - q_2$$

$$\frac{d^2T_{line}(x)}{dx^2} = \lambda^2 T_{line}(x) - \lambda^2 T_{ref}(x) - \theta$$

λ and θ are constants

$$f(L, t_m, k_m, t_{ins}, k_{ins}, I_{rms}, R_E)$$

Non-Uniform Temperature-Dependent Delay



$$D = R_d(C_P + C_L + \int_0^L c_0(x)dx) + \int_0^L r_0(x)(\int_x^L c_0(\eta)d\eta + C_L)dx$$

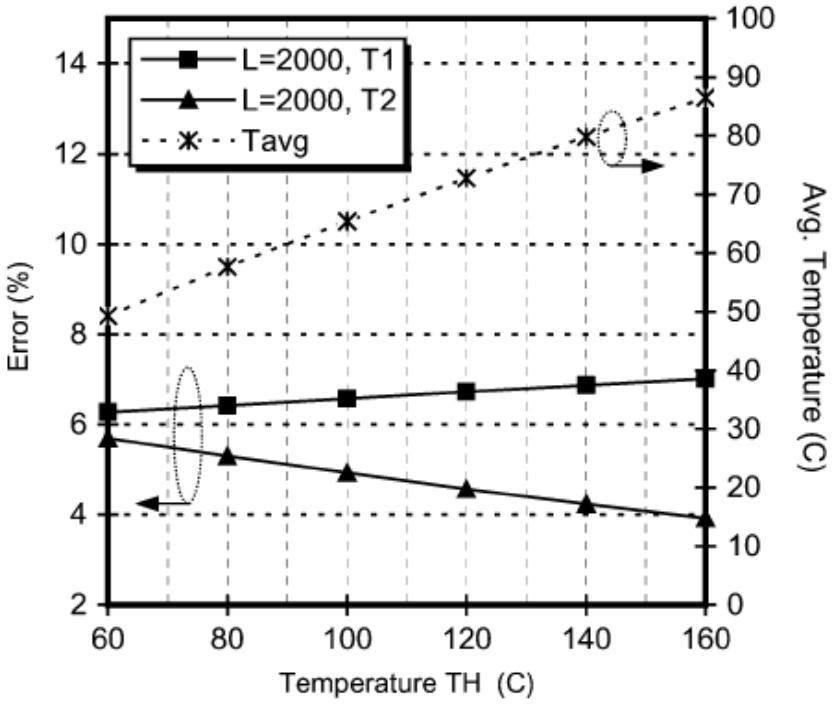
$$D = D_0 + (c_0 L \rho_0 C_L \beta_0) \int_0^L T_0(x)dx - c_0 \rho_0 \beta_0 \int_0^L x T_0(x)dx$$

D_0 is the Elmore delay model at reference temp.

Implications for Delay and IR-Drop

Impact on delay estimation…..

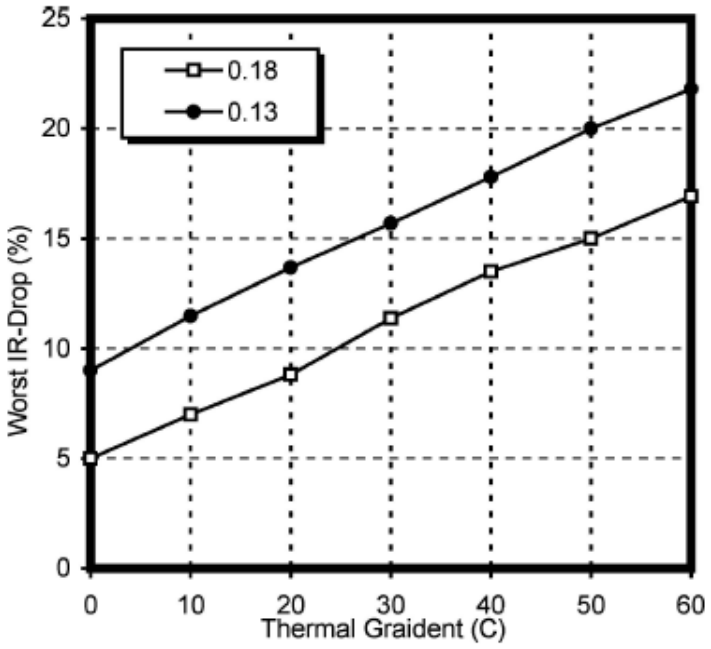
T1: positive exponential gradient
T2: negative exponential gradient
For a fixed T_Low



Ajami et al., TCAD 2005

Impact on IR-drop analysis…..

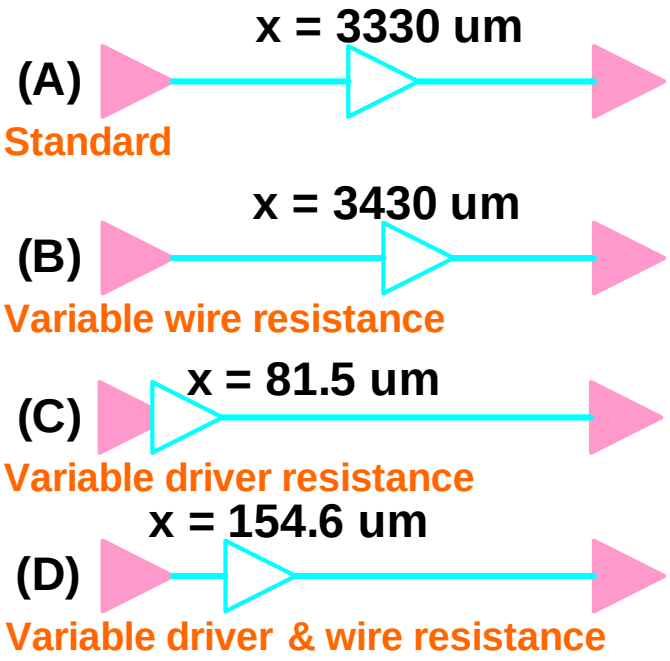
Worst-case voltage-drop (V_{IR}/V_{dd}) increases in the presence of thermal gradients



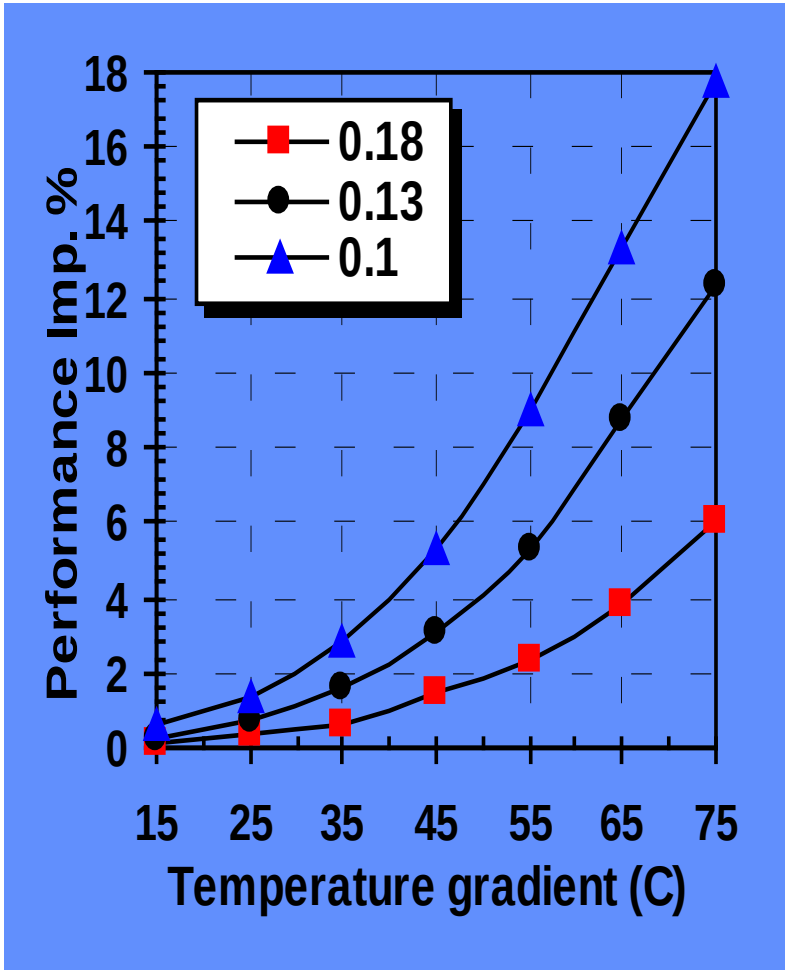
Ajami et al., JAICSP, 2005

Impact on Buffer Insertion

Buffer movement in a 6660 um line (180 nm node)



Delay improvement after thermally-aware buffer insertion



Ajami et al., ICCAD 2001