
ECE 225

High-Speed Digital IC Design

Lecture 8

Power Dissipation in ICs

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Forms of Power Dissipation

- **Dynamic Power**

- Due to charging/discharging of capacitors....

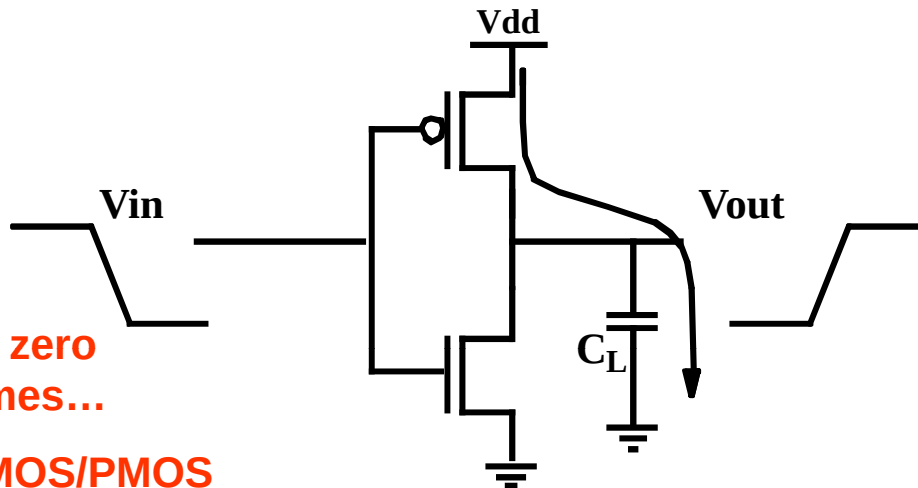
- **Leakage Power**

- Subthreshold leakage
- Gate leakage
- Junction leakage
- other mechanisms...

- **Short-Circuit Power**

- When NMOS and PMOS are both turned ON....

Dynamic Power Dissipation



Assuming zero
rise/fall times...

So that NMOS/PMOS
are never ON
simultaneously...

$$\text{Energy/transition} = C_L * V_{dd}^2$$

Low-to-High transition:

- C_L is charged through PMOS and discharged through NMOS
- During charging, voltage of C_L rises from 0 to V_{dd} ... energy is drawn from the power supply
- Part of this energy is stored in C_L while rest gets dissipated in the PMOS

Note: Here C_L is
an external
capacitor....

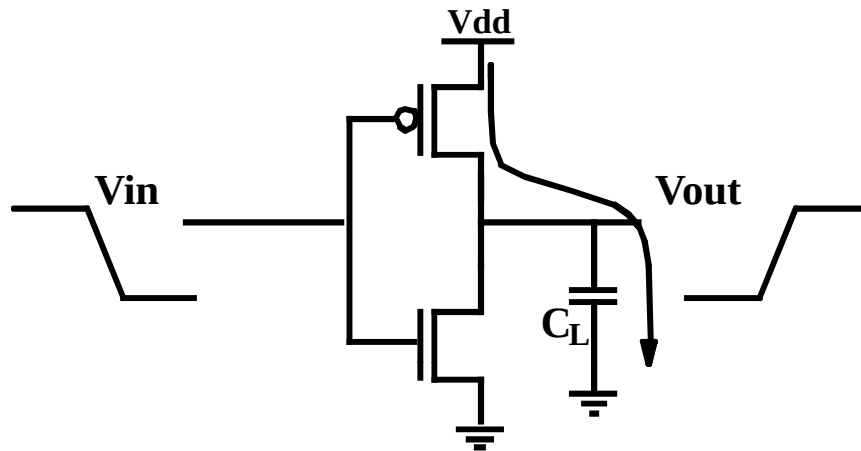
- Energy/transition is not a function of transistor sizes!

Need to reduce C_L , V_{dd} , and f to reduce power.

Energy taken from supply during transition:

$$E_{V_{DD}} = \int_0^{\infty} i_{V_{DD}}(t) V_{DD} dt = V_{DD} \int_0^{\infty} C_L \frac{dv_{out}}{dt} dt = C_L V_{DD} \int_0^{V_{DD}} dv_{out} = C_L V_{DD}^2$$

Dynamic Power Dissipation



High-to-Low transition:

- During the discharge phase, charge is removed from C_L and its energy is dissipated in the NMOS
- Each switching cycle consists of a L-H and H-L transition and takes a fixed amount of energy = $C_L V_{dd}^2$

Energy taken from supply during transition:

$$E_{V_{DD}} = \int_0^{\infty} i_{V_{DD}}(t) V_{DD} dt = V_{DD} \int_0^{\infty} C_L \frac{dv_{out}}{dt} dt = C_L V_{DD} \int_0^{V_{DD}} dv_{out} = C_L V_{DD}^2$$

Energy stored in the capacitor:

$$E_C = \int_0^{\infty} i_{V_{DD}}(t) v_{out} dt = \int_0^{\infty} C_L \frac{dv_{out}}{dt} v_{out} dt = C_L \int_0^{V_{DD}} v_{out} dv_{out} = \frac{C_L V_{DD}^2}{2}$$

Where is the other half of the energy?Dissipated in the PMOS

Dynamic Power Dissipation

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

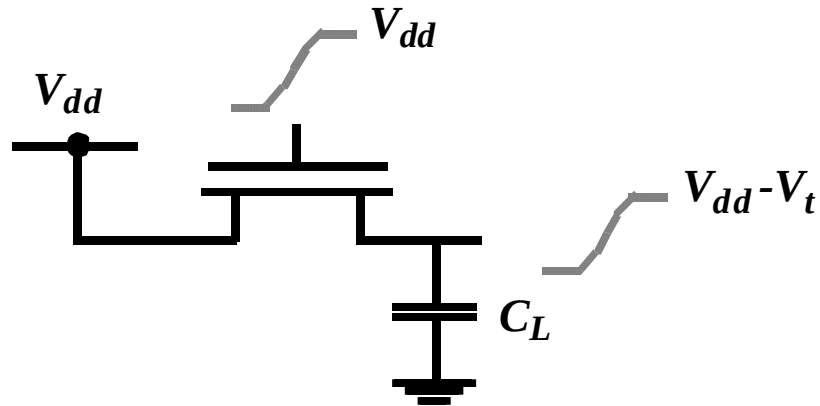
- “f” accounts for how often the gate is switched ON and OFF...
- f increases with scaling...since gate delay decreases

Consider a 0.25 um CMOS technology with a clock-rate of 500 MHz and average load capacitance of 15 fF/gate assuming a fan-out of 4: the power consumption per gate = 50 μ W (for $V_{dd} = 2.5$ V)

One-million such gates would result in a power consumption of 50W! (fortunately, not all gates are switching at the clock frequency...)

Power dissipation in a complex gate is more complex to estimate...since the switching frequency depends on the nature and statistics of the input signals. This is accommodated by replacing “f” with “p.F”, where p is the probability that a clock event results in a 0 to 1 transition and F is the maximum possible event-rate (or clock rate) of inputs

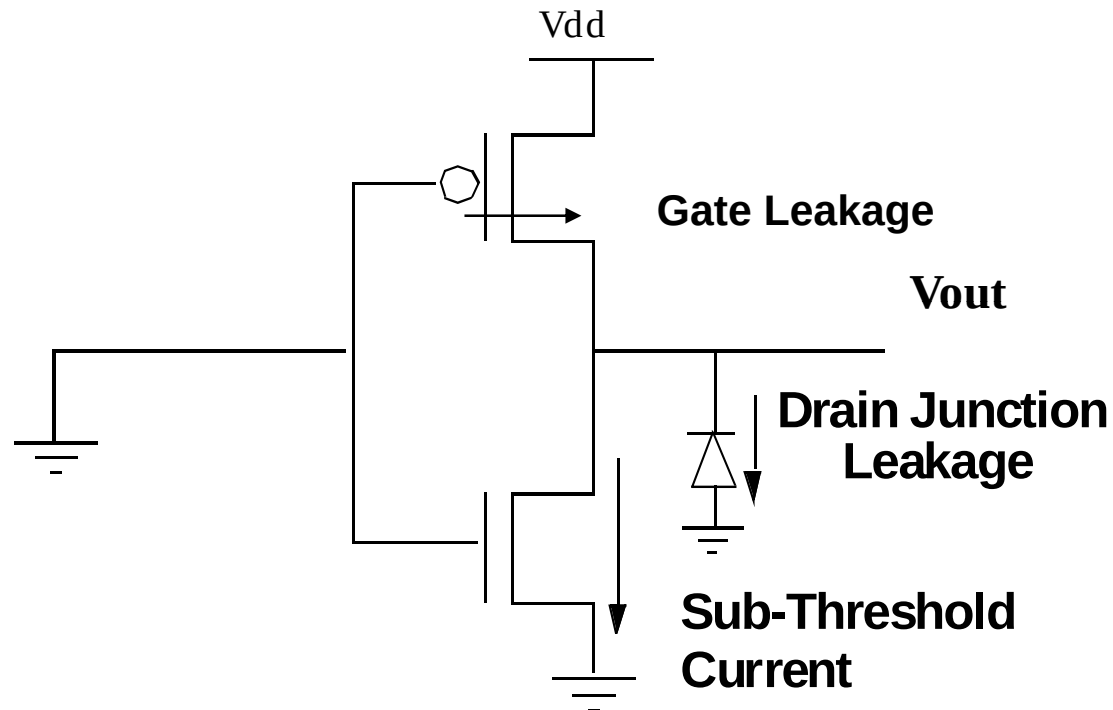
Modification for Circuits with Reduced Swing



$$E_{0 \rightarrow 1} = C_L \cdot V_{dd} \cdot (V_{dd} - V_t)$$

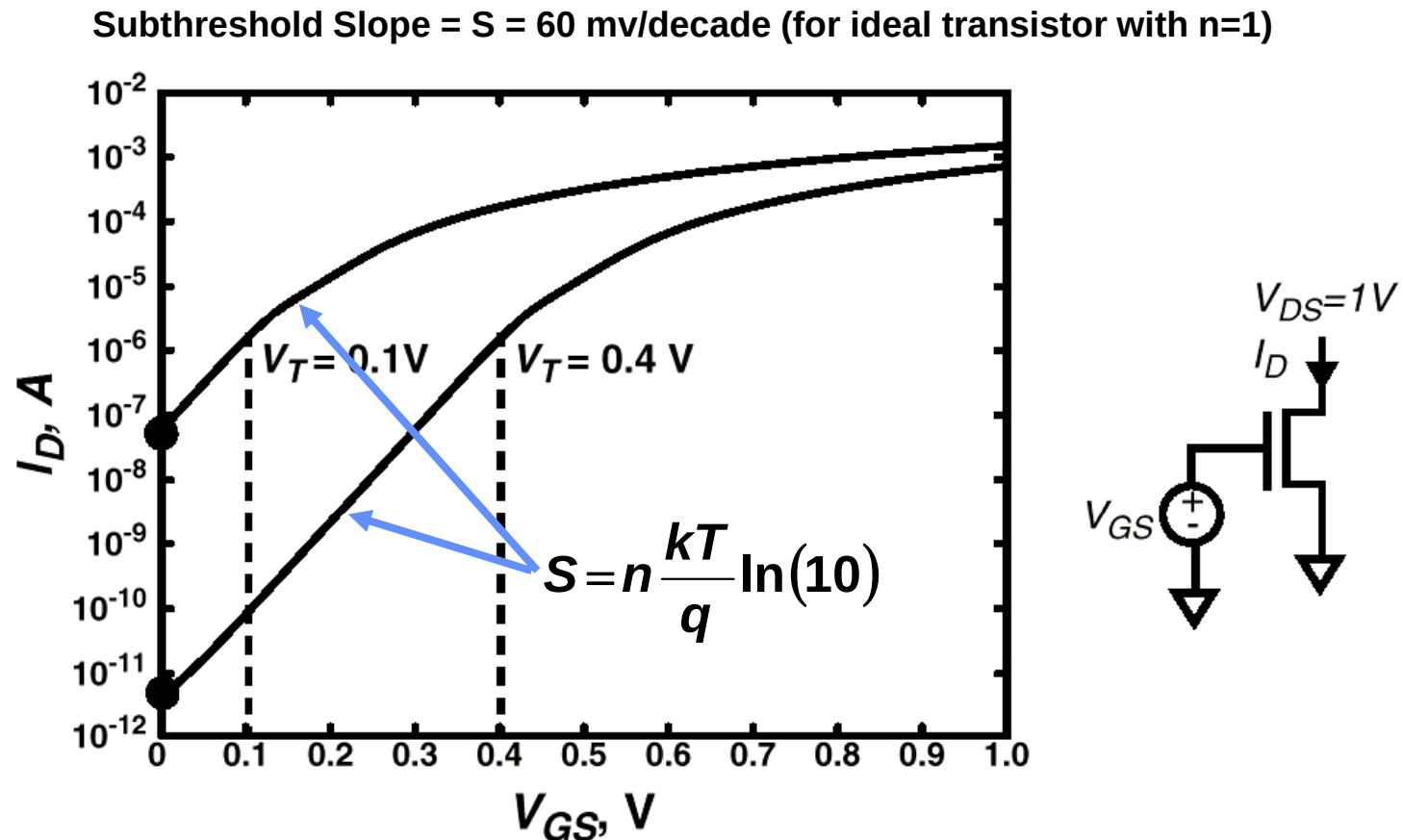
- Can exploit reduced swing to lower power (e.g., reduced bit-line swing in memory)

Primary Leakage Mechanisms



**Sub-threshold current one of most compelling issues
in low-power and energy-efficient circuit design!**

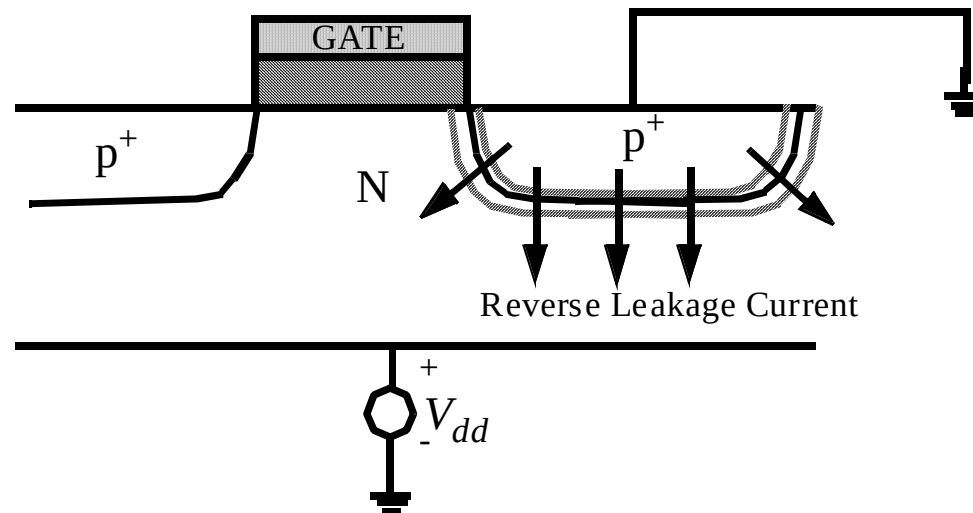
Subthreshold Leakage Component



- Leakage control is critical for low-voltage operation

Reverse-Biased Diode Leakage

Much smaller than
subthreshold
leakage....

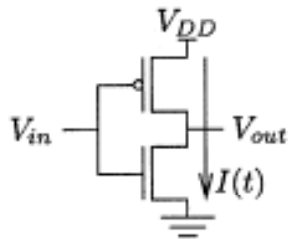


$$I_{DL} = J_S \times A$$

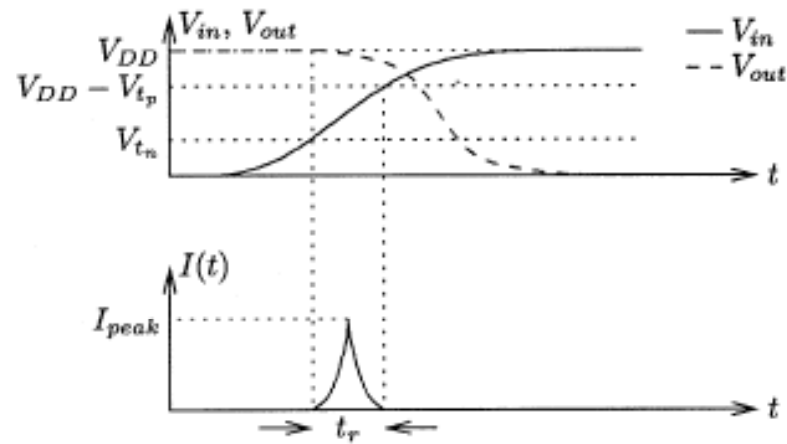
$J_S = 10\text{-}100 \text{ pA}/\mu\text{m}^2$ at 25 deg C for 0.25 μm CMOS

J_S doubles for every 9 deg C!

Short Circuit Currents



(a)
CMOS
inverter.



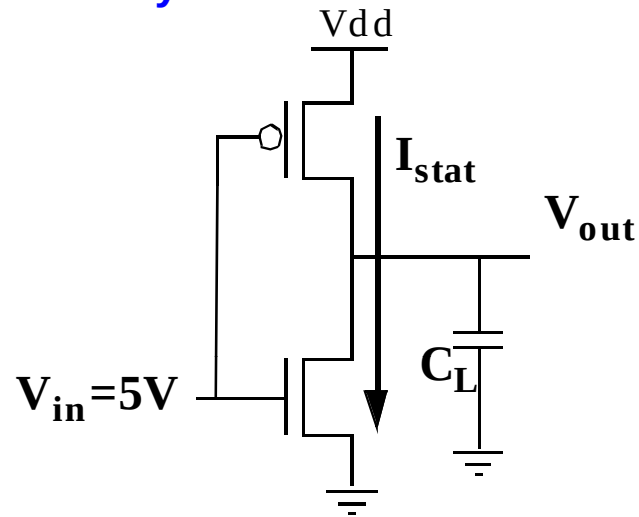
(b) Voltage and current waveforms.

K. Banerjee and A. Mehrotra, IEEE Transactions on
Electron Devices, Vol. 49, No. 11, 2002.

Fig. 5. Voltage and current waveforms of a CMOS inverter.

Static Power Consumption

In the absence of switching....steady-state operation



Sources:

Due to all previously mentioned leakage currents.....

$$P_{stat} = P_{(In=1)} \cdot V_{dd} \cdot I_{stat}$$

Wasted energy ...should be avoided in almost all cases...

Leakage Currents

□ Effect of leakage current

- “Wasted” power: power consumed even when circuit is inactive
- Leakage power raises temperature of chip
- Can cause functionality problem in some circuits: memory, dynamic logic, etc.

□ Reducing transistor leakage

- Long-channel devices
- Small drain voltage
- Large threshold voltage V_T

Leakage Power Reduction

□ Process scaling

- V_T reduces with each new process (historically)
- Leakage increases $\sim 10X$!

□ Leakage vs. performance tradeoff:

- For high-speed, need small V_T and L
- For low leakage, need high V_T and large L

□ One solution: dual- V_T process

- Low- V_T transistors: use in critical paths for high speed
- High- V_T transistors: use to reduce power

Principles for Power Reduction

☐ Prime choice: Reduce voltage!

- Recent years have seen an acceleration in supply voltage reduction
- Design at very low voltages still open question (0.6 ... 0.9 V by 2010!)

☐ Reduce switching activity

☐ Reduce physical capacitance

- Device Sizing

What is the Lowest Possible Power Supply?

V_{dd} must be greater than a few times kT/q

Why is that?

ECE 225

High-Speed Digital IC Design

Lecture 8 (Cont'd)

*Nanoscale Power and Thermal Management:
Electrothermal Couplings in Nanoscale CMOS
Self-Consistent Temperature Profile Estimation*

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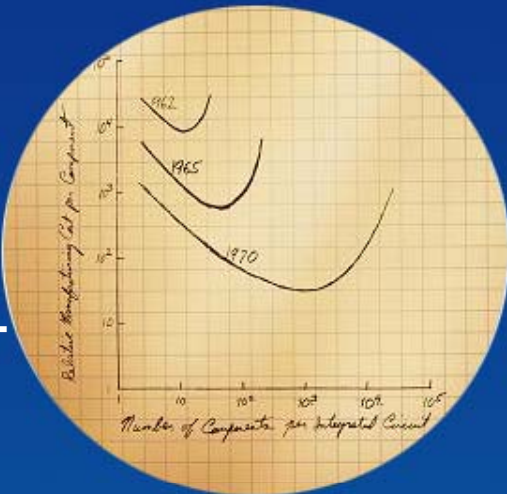


Outline

- ❖ Introduction
 - ❖ Technology Scaling Challenges
 - ❖ Power and Thermal Problems
 - ❖ Integrated Approach
- ❖ Integrated Power-Thermal Management
 - ❖ Electrothermal Couplings in Nanoscale CMOS
 - ❖ Design-Package Co-Optimization
 - ❖ Self-Consistent Temperature Profile Estimation

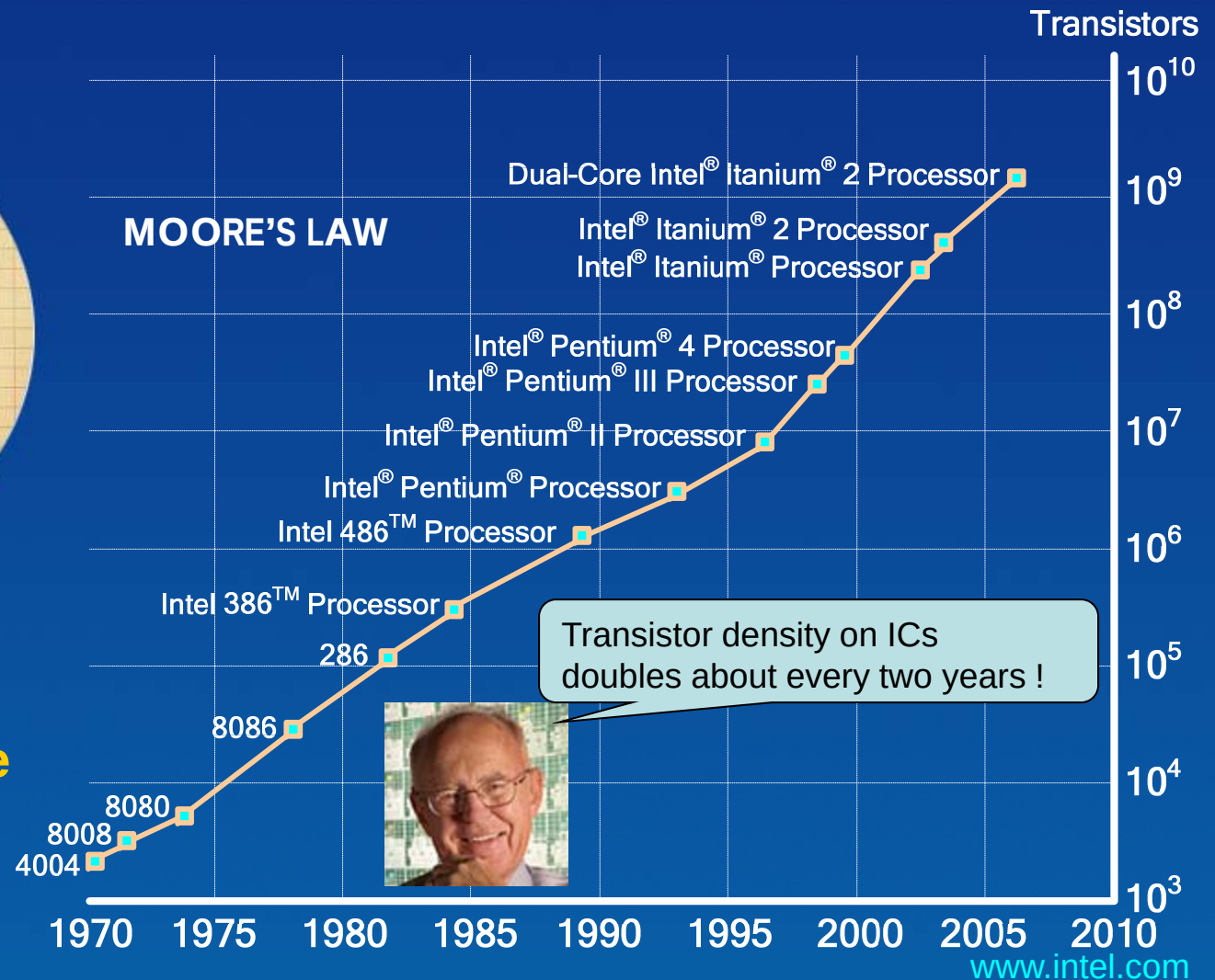
Technology Scaling — Moore's Law

Cost per Transistor



of Transistors

Better Performance
Lower Cost
More Functionality



In 1965, Gordon Moore sketched out his prediction of the pace of silicon technology. Decades later, Moore's Law remains true, driven largely by Intel's unparalleled silicon expertise.

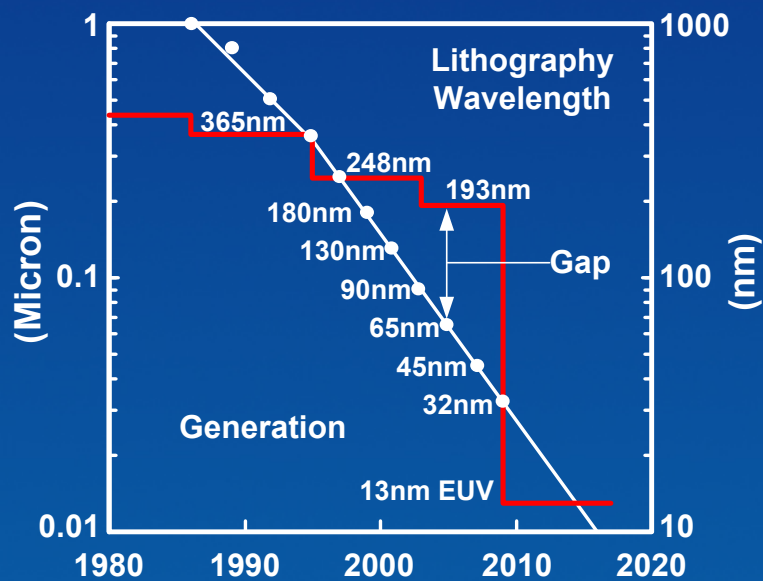


Technology Scaling Challenges — 1

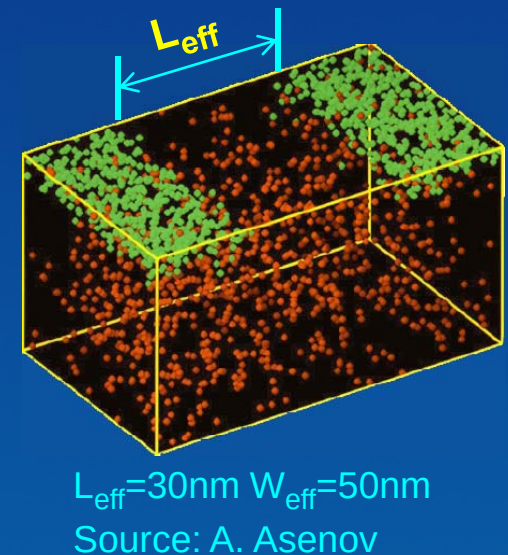
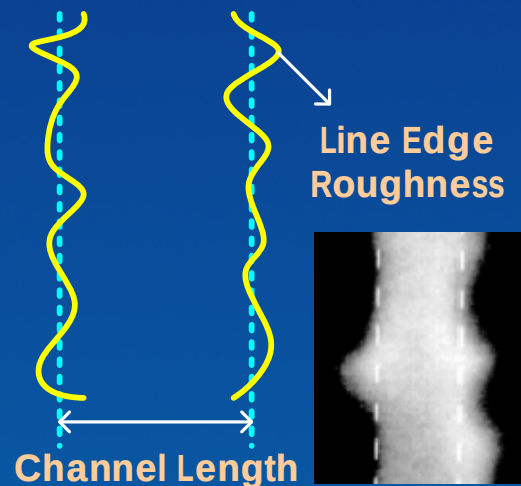
❖ Process-Induced Random Variations in Devices

❖ Critical Dimension Variation

❖ Random Dopant Fluctuation



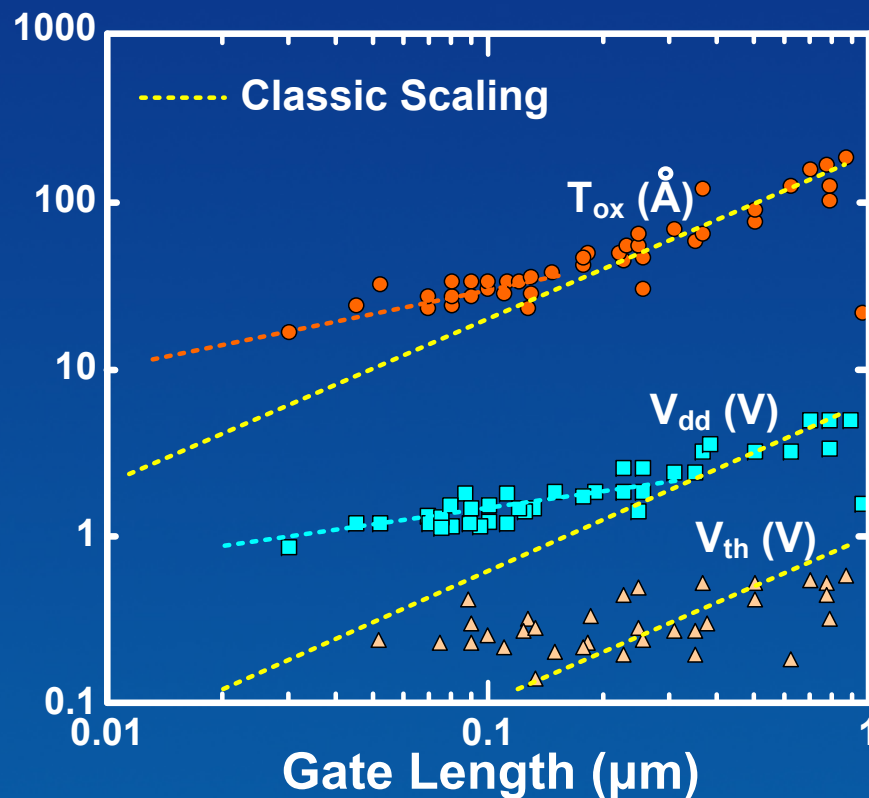
Source: Mark Bohr, Intel



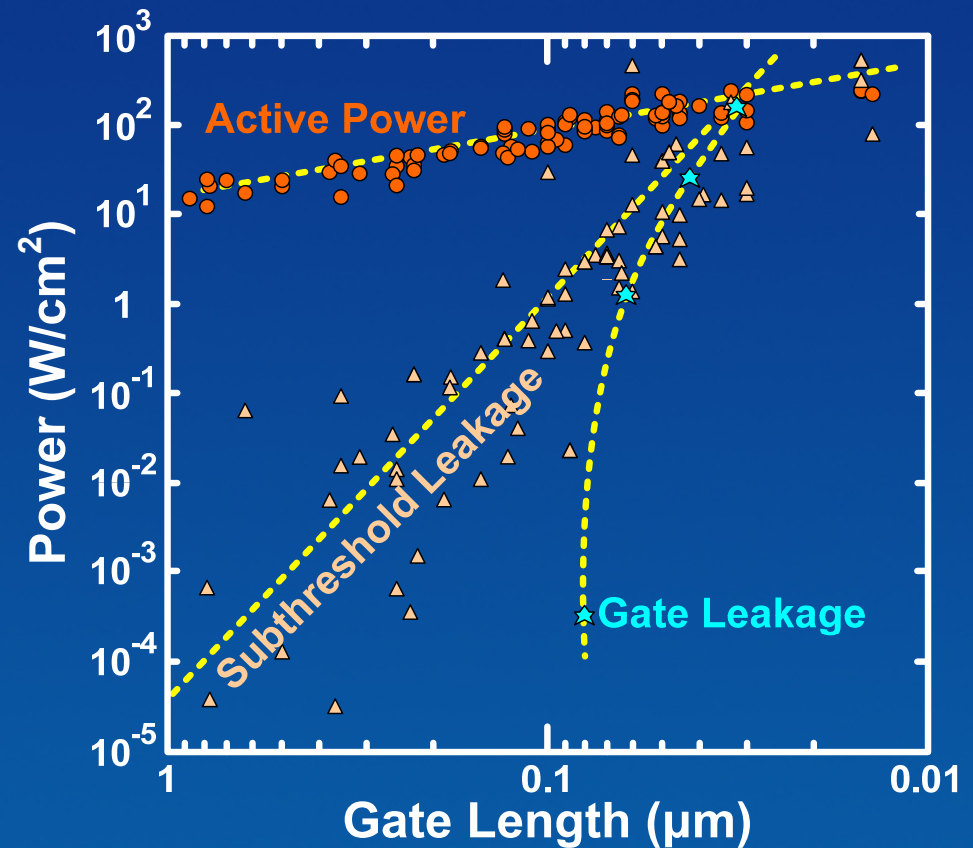
Random variations cause negative shift of threshold voltage, which increases leakage substantially.

Technology Scaling Challenges — 2

❖ Leakage



E.J. Nowak, 2002



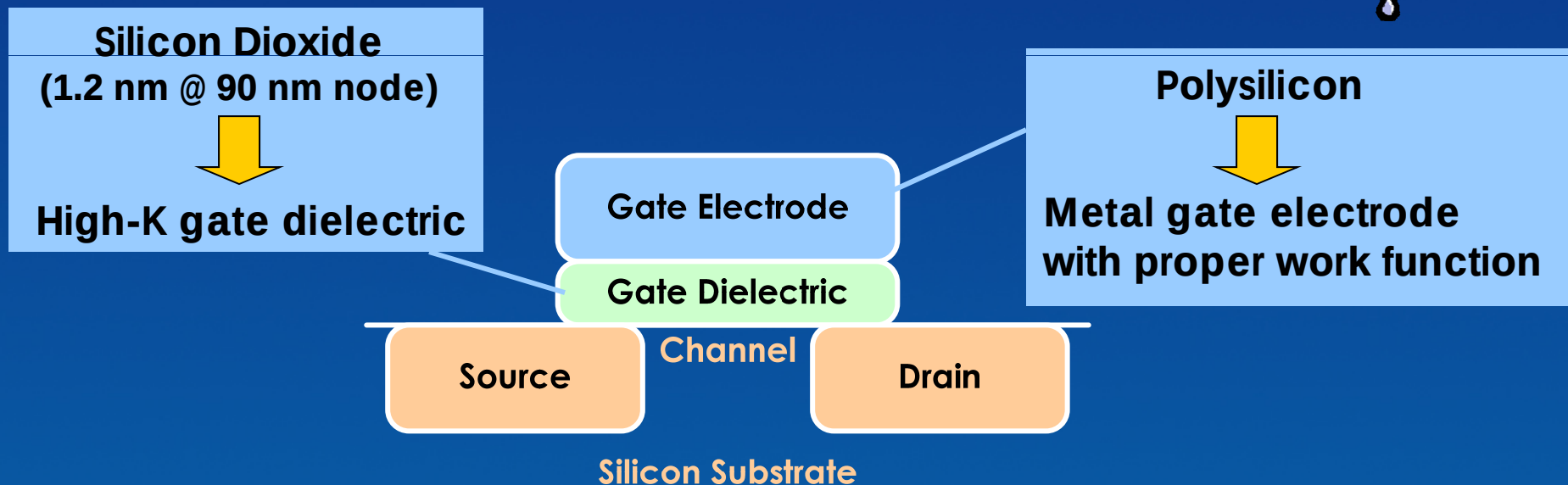
E.J. Nowak, 2002

Say goodbye to “happy scaling”

Technology Scaling Challenges — 3

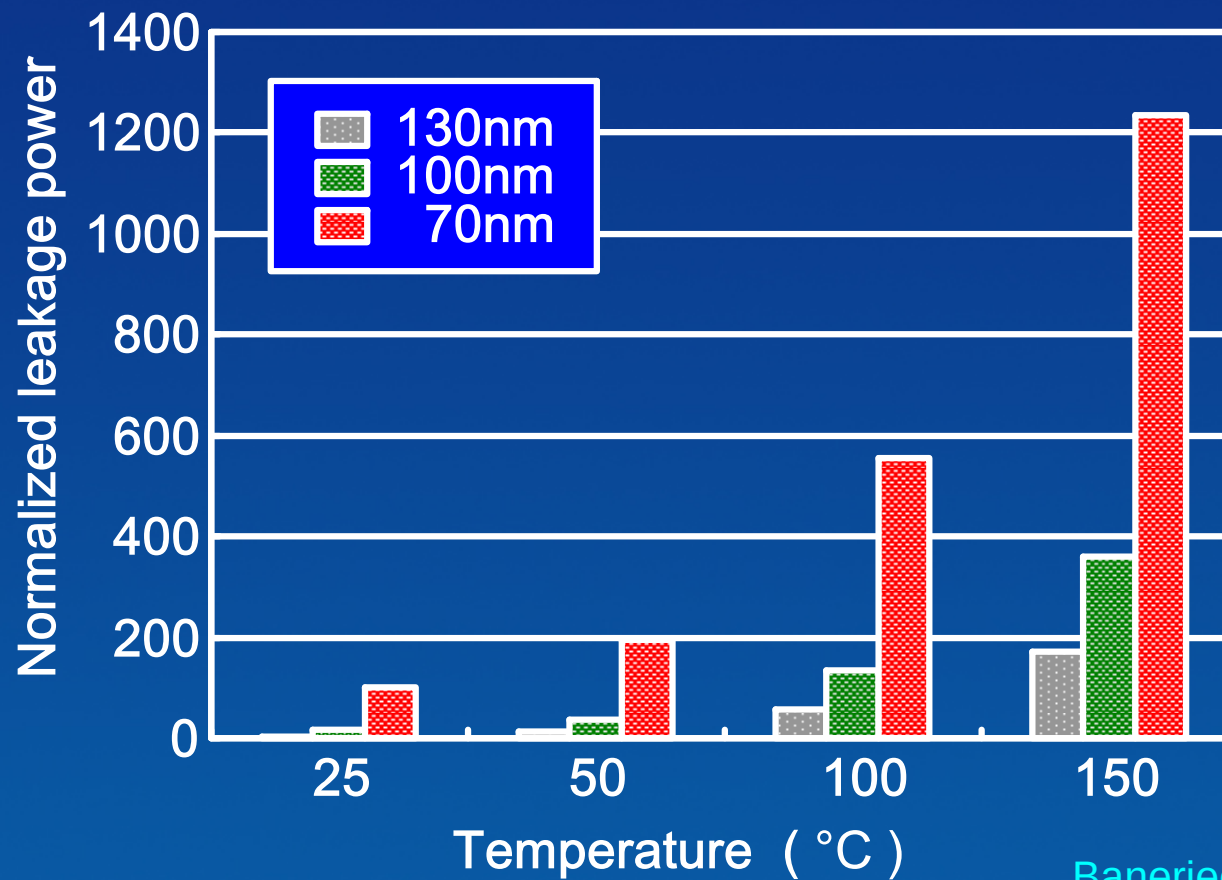
❖ Leakage:

❖ Gate Stack Processes and Materials (Reduce gate leakage)



1. Silicon Dioxide is too thin to be a good insulator.
2. Alternative gate electrode materials are needed.
(compatible with high-K gate dielectric)

Technology Scaling Challenges — 4

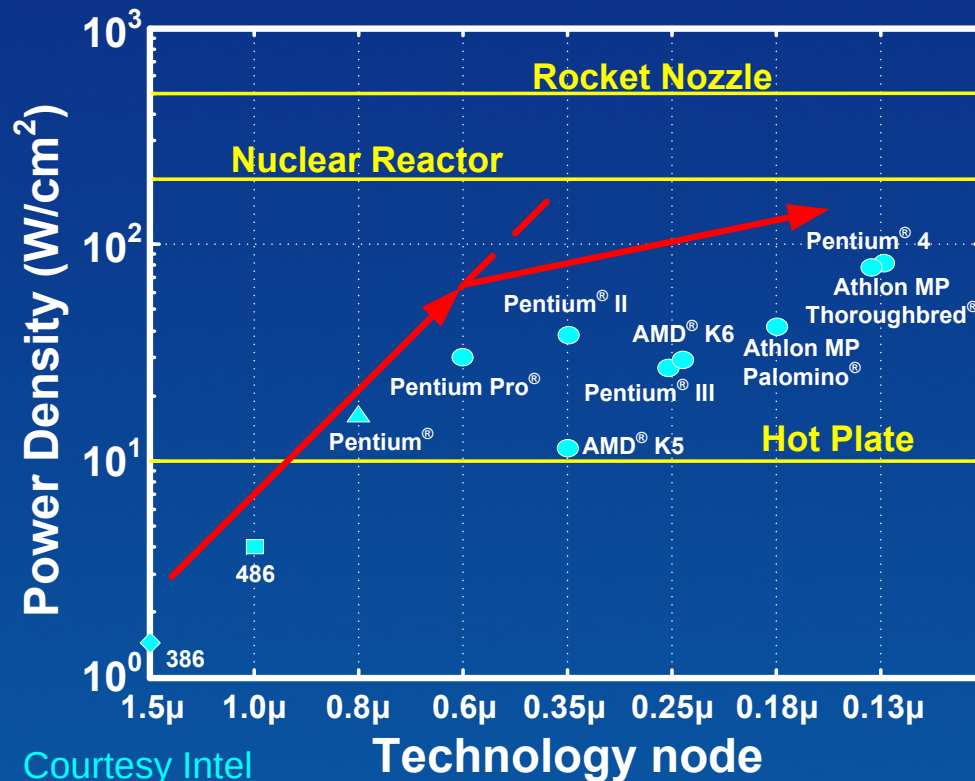


Banerjee et al. IEDM 2003

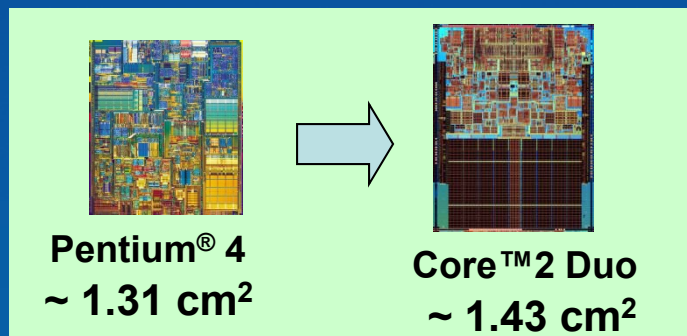
Subthreshold leakage increases with scaling and temperature.....



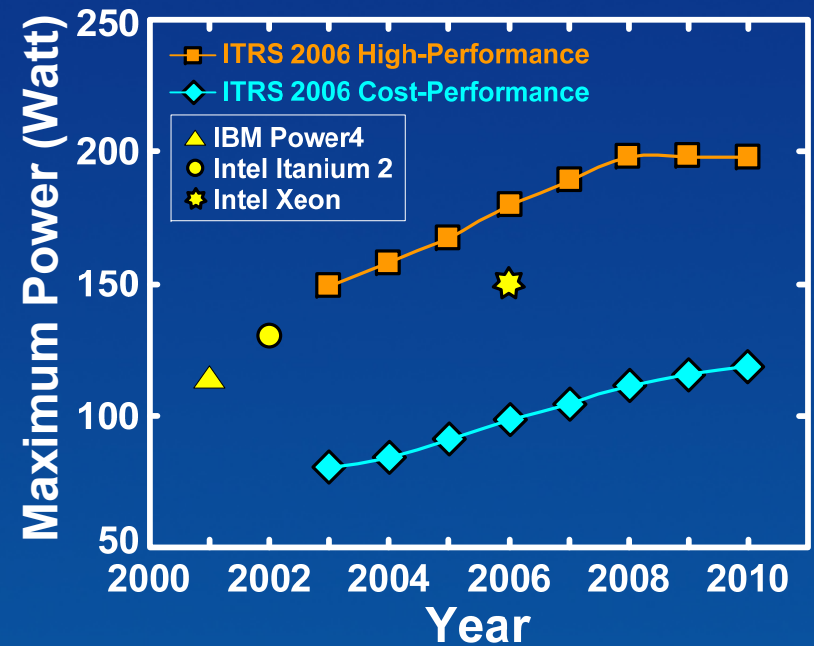
Increasing Power Demand.....



Courtesy Intel



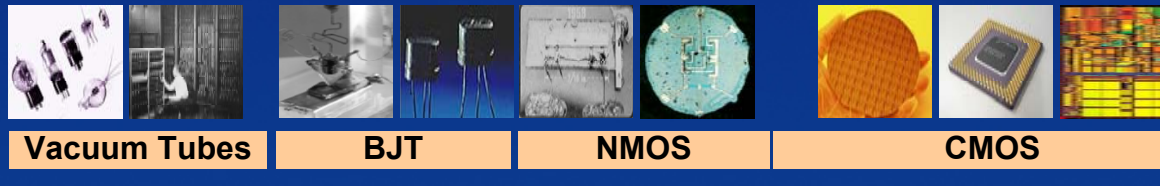
International Technology Roadmap for Semiconductors



- ❖ Higher performance
- ❖ More Functionalities
- ❖ Higher interconnect power
- ❖ Increasing leakage



Power has been a technology driver....



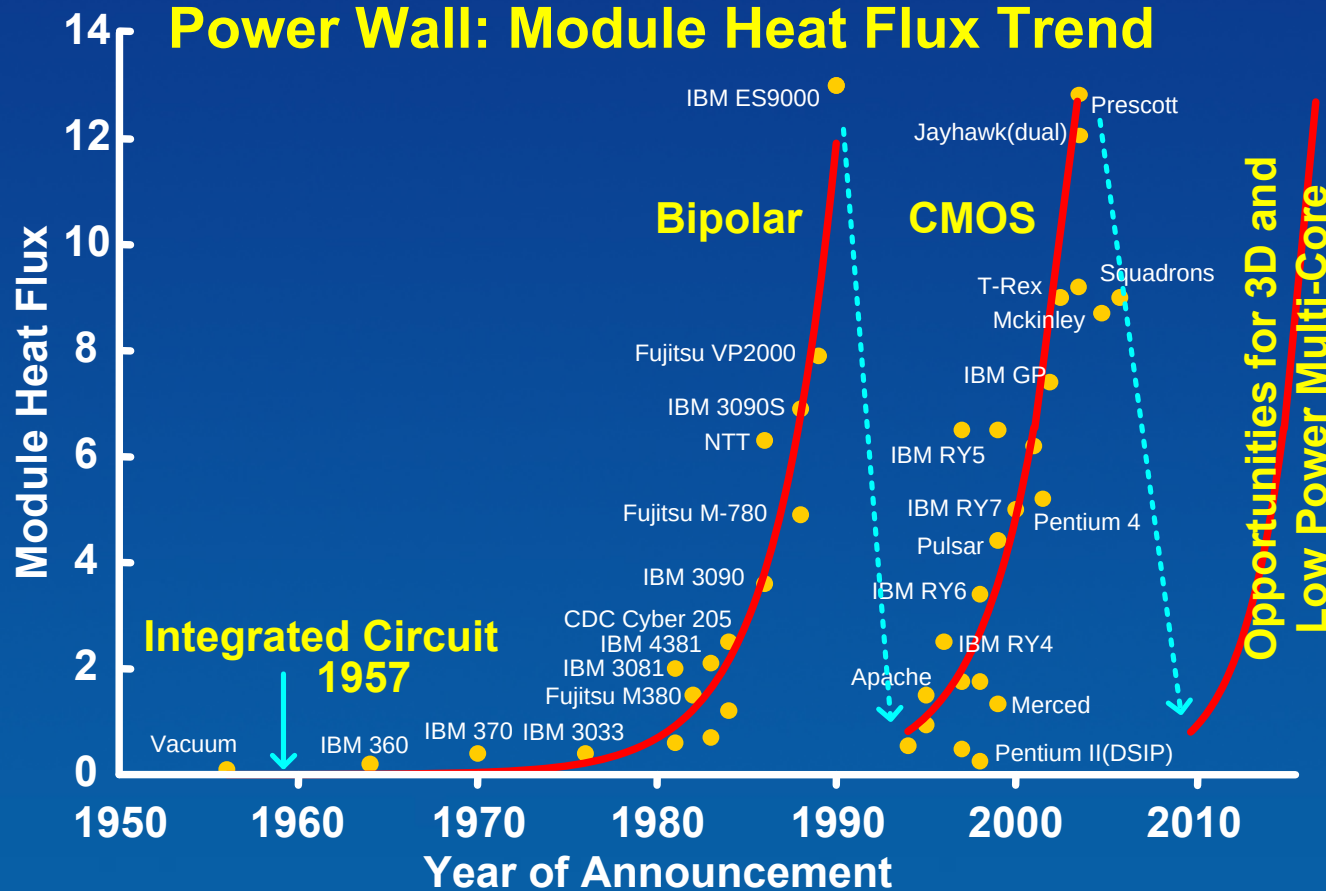
1906

1950

1960

1963

Power Wall: Module Heat Flux Trend



Power is the only limiter

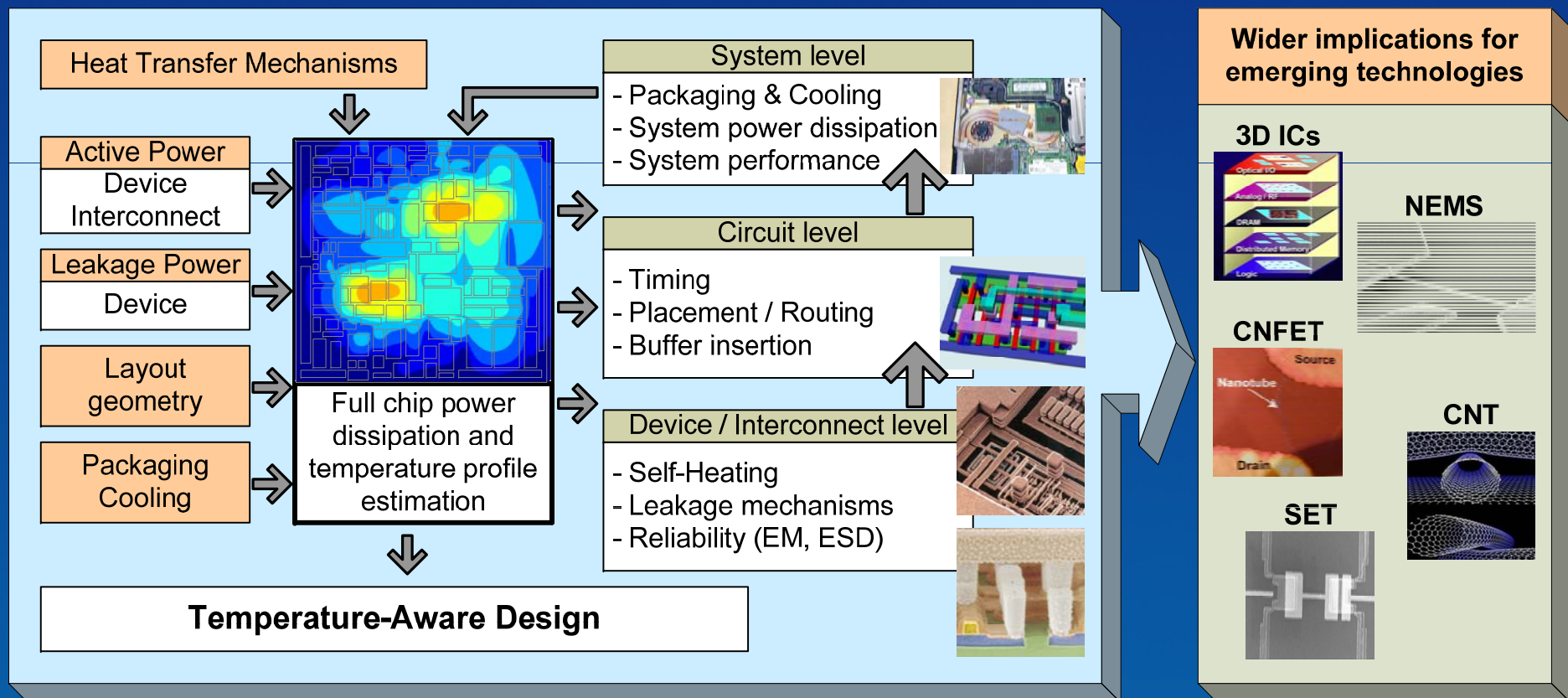


P. Gelsinger, Intel



Integrated Power & Thermal Management

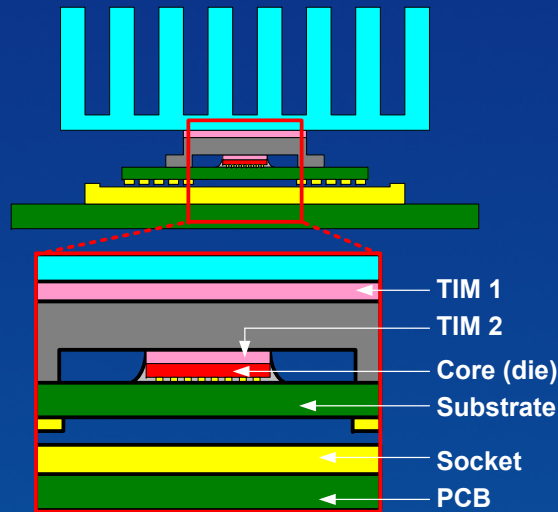
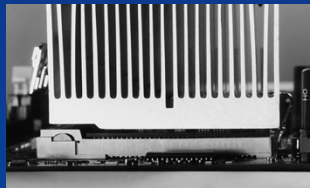
Temperature distribution plays a key role...



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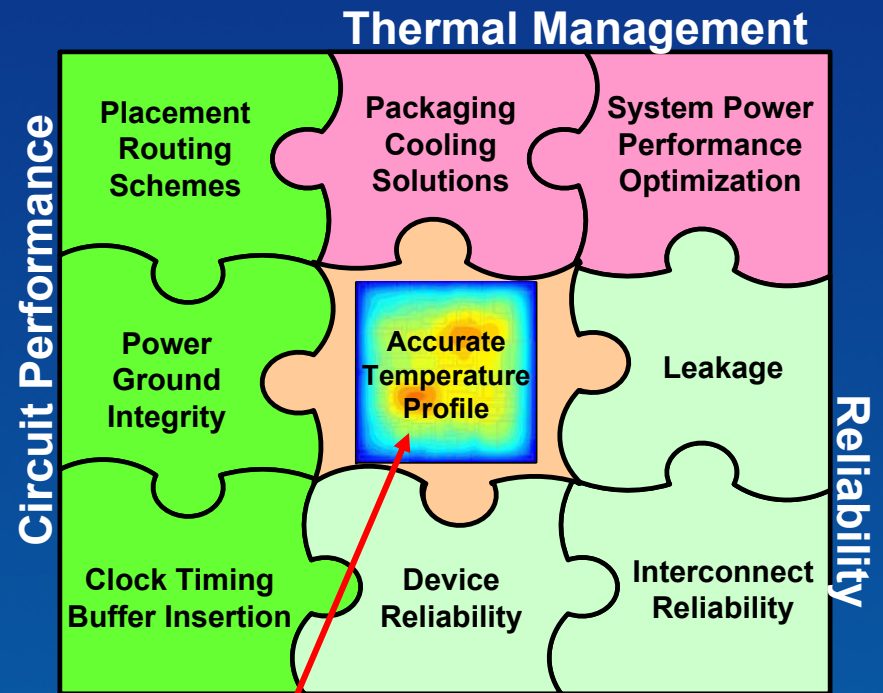
Design/Packaging Conflicts!



Design



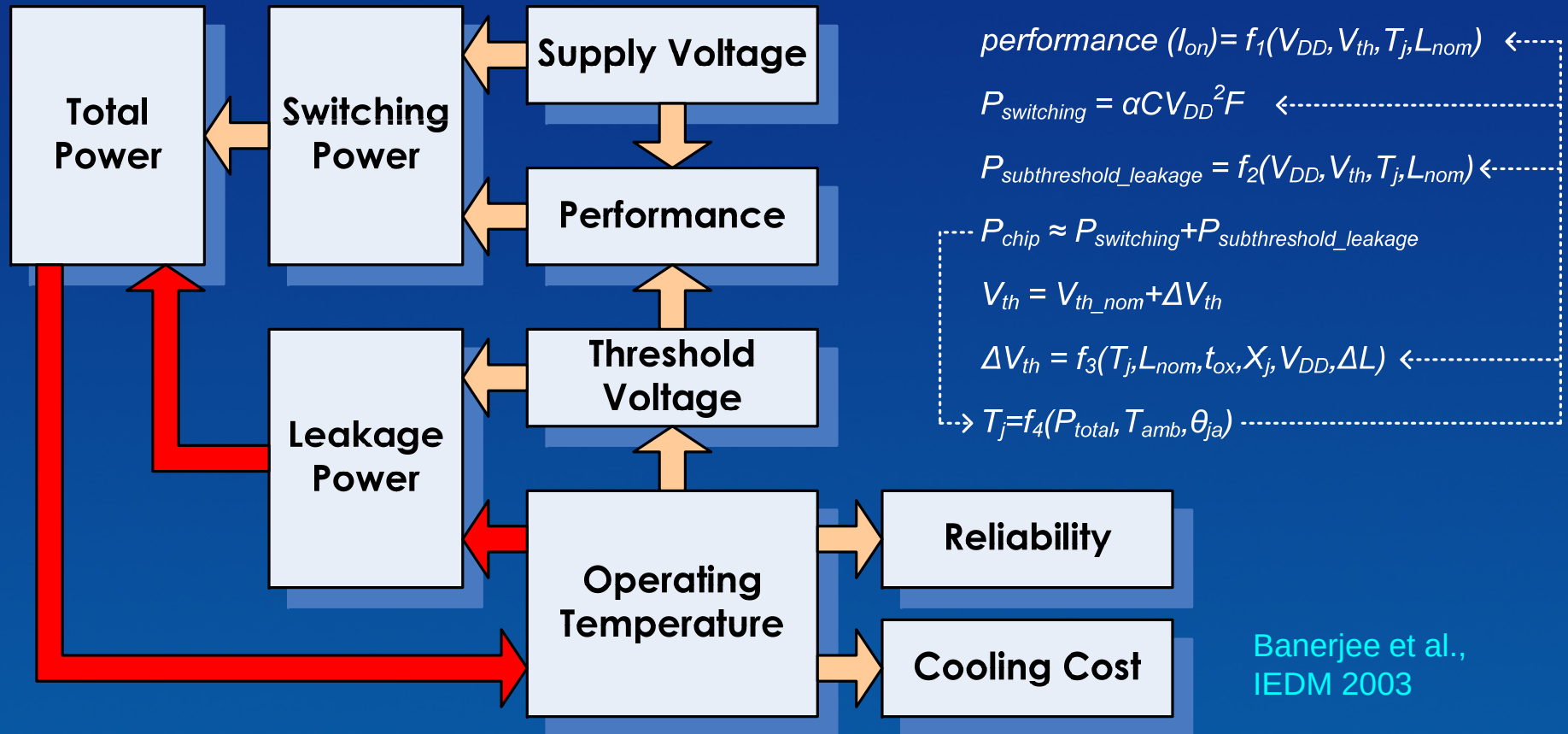
Packaging



Key piece of the design puzzle



Electrothermal (ET) Couplings

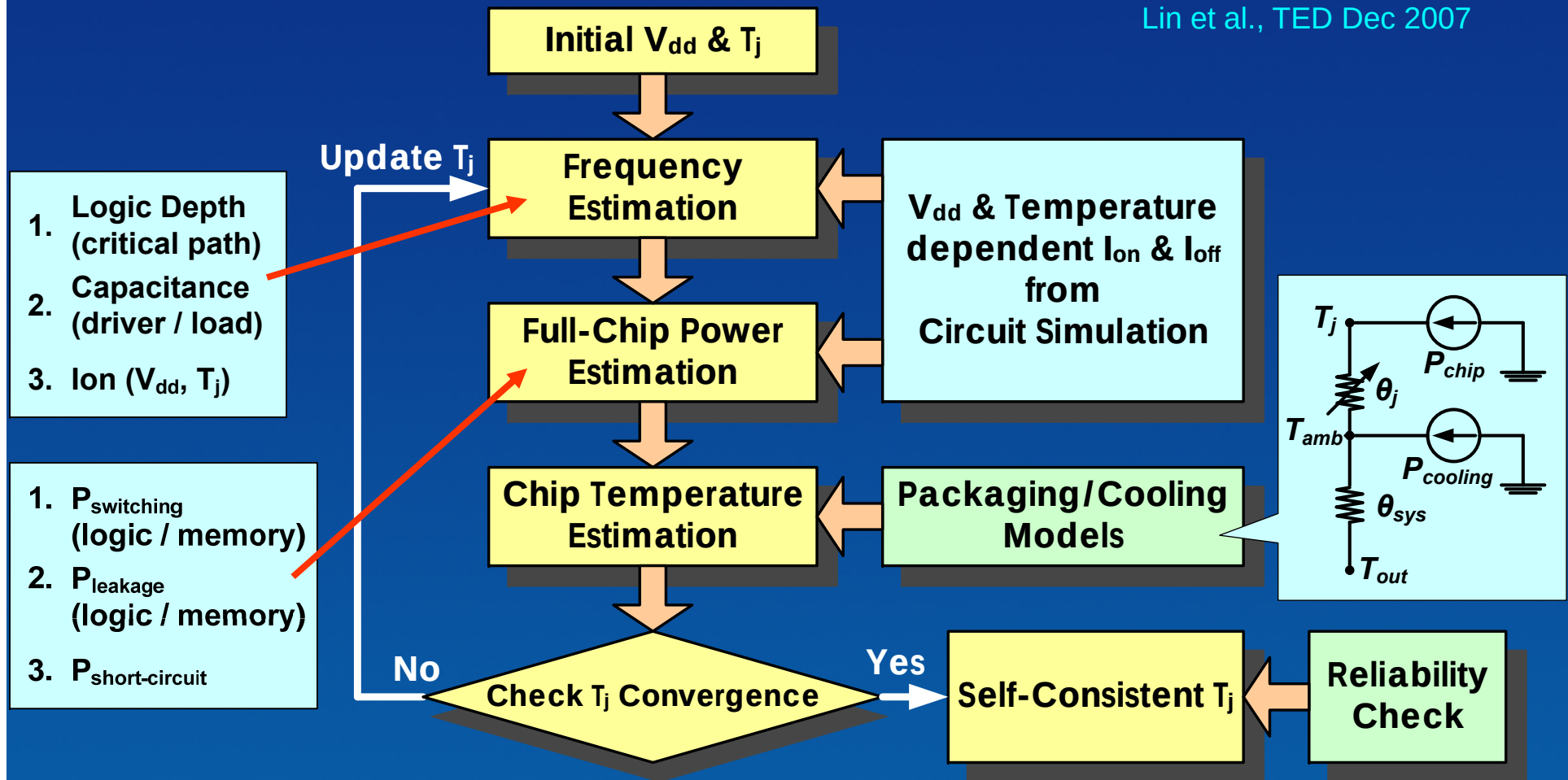


Banerjee et al.,
IEDM 2003

Positive feedback between temperature, leakage and total power leads to electrothermal couplings, which had been inconspicuous for earlier generation of ICs.

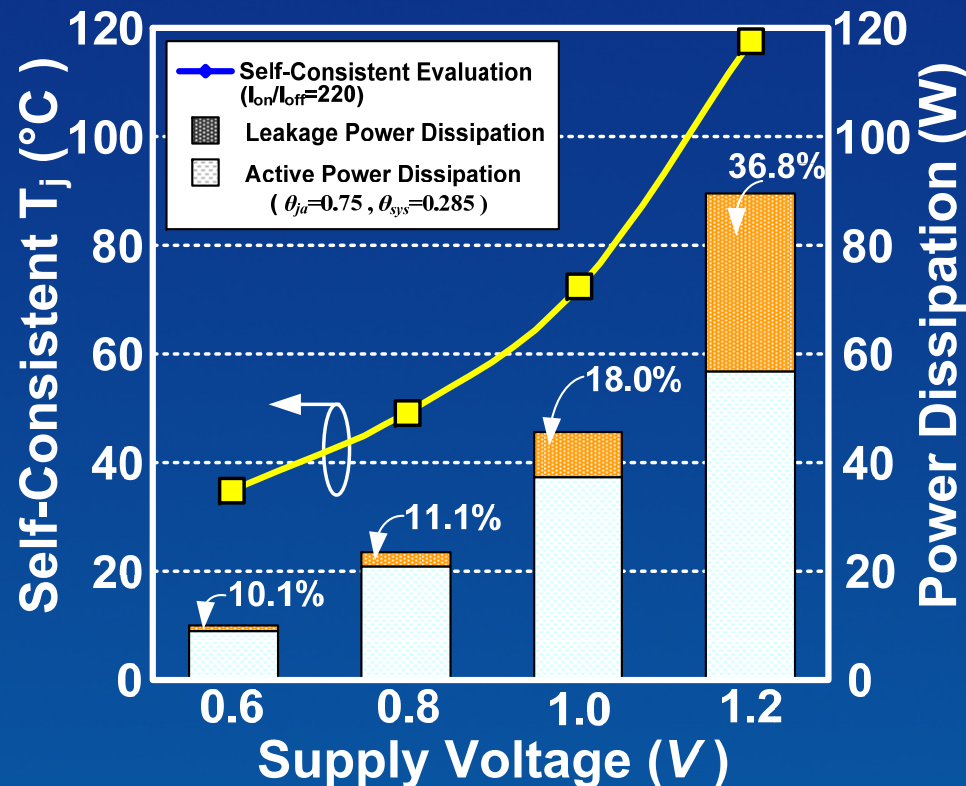
Self-Consistent Methodology

Lin et al., TED Dec 2007



Obtain a self-consistent average junction temperature

Self-Consistent Evaluation



1. Leakage power becomes a major contributor to total power when junction temperature is high.
2. For leakage dominant technologies, lowering supply voltage may even improve performance.