A Capacitorless DRAM Cell on SOI Substrate

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ABSTRACT

We propose a capacitorless DRAM (CDRAM) cell on SOI substrate with large READ current (>100μA/μm), small cell size, and simple fabrication process. PISCES simulations are used to analyze the memory cell operations. The CDRAM cell size is that of a transistor, which makes it very attractive for high density memory applications. Since the fabrication process of CDRAM is compatible with that of the general-purpose SOI CMOS and complementary BiCMOS process, CDRAM can also be used for integrated on-chip memory and is an interesting candidate as the technology driver of SOI VLSI.

INTRODUCTION

Dynamic random access memory (DRAM) is a major semiconductor product and has been the "technology driver" for the semiconductor industry. DRAM cell contains one transistor for controlling READ/WRITE operations and one capacitor for charge storage. The transistor uses the smallest feature size available thus drives the front-end technology such as lithography, transistor scaling and isolation. The technology developed for DRAM can later be used for fabricating other semiconductor products.

However the challenge of DRAM technology of 64 megabits and beyond has been more on how to build a capacitor in a small area with sufficient capacitance, usually 30fF to provide enough signal-to-noise ratio, rather than on transistor scaling. Novel high dielectric-constant material or novel capacitor structure become the main focuses for current DRAM technology[1]. Besides the fact that the fabrication process of 64 megabits DRAM and beyond is becoming more and more difficult, the development and manufacturing cost is increasing tremendously yet a significant portion of the technology developed for DRAM is not extendible to other products.

The concept of "gain cell" has been proposed to alleviate the dependence on large cell capacitance. Many gain cells proposed use an additional transistor (e.g., JFET[2] Complementary MOS[3], or BJT[4]) integrated with the one transistor/one capacitor DRAM cell unit to amplify the charge stored in a smaller-area capacitor whose capacitance is lowerbounded by soft-error consideration (~10fF). However these gain cells either take larger cell layout area or involve complicated fabrication process, both of which increase development and manufacturing costs. Another category of gain cells uses the concept of "dynamic threshold[5,6]." However these dynamic threshold cells proposed are more sensitive to the processing conditions and may be difficult to manufacture.

This paper describes a capacitorless DRAM (CDRAM) cell on SOI substrate. The memory operation of CDRAM is similar to the dynamic threshold cells therefore a distinct storage capacitor is not needed[5,6]. In CDRAM, the charge is stored in the SOI top Si/SiO_2 accumulation layer to modulate the threshold voltage of the bottom channel device. Device simulations show that the amount of charge read in the CDRAM cell can easily exceed the amount of charge read in ordinary DRAM cell (~100fC).

CDRAM CELL OPERATION

The device cross section of CDRAM cell is shown in Fig.1, in which CDRAM is based on a PMOSFET with an additional shallow n^+ region overlapping to the gate. CDRAM based on NMOSFET can be realized similarly. The device dimensions used in the simulations of the subsequent illustrations are listed in table I. Note that the feasibility to control one of the critical dimensions, the length of the sandwiched p region between the n type floating body and the shallow n^+ implant has been demonstrated in the base width control of SOI lateral BJT[7]. The general memory behavior of CDRAM can be understood with its equivalent circuit shown in Fig.2. A WRITE NMOSFET using the SOI front channel, a READ PMOSFET using the SOI back channel, and a "floating-gate-like" storage node using the front channel accumulation layer of the floating body are integrated within one transistor feature size. Since there are four signal lines associated with the CDRAM cell: the READ bit line (RBL), the WRITE bit line (WBL), the word line (WL) and the purge line (PL), there can be many ways to layout the memory array. In the following sections we will first describe the general memory operations, and then propose one possible memory array configuration that maximizes the memory density.

There are four operations of CDRAM: HOLD, READ, WRITE, and PURGE. The applied voltages used in the subsequent discussions are listed in table II.

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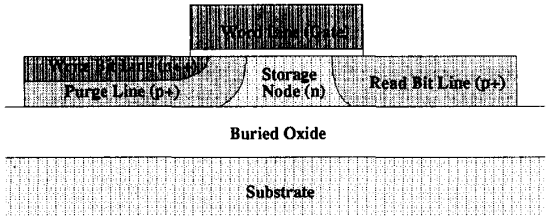

Fig.1 CDRAM cross section.

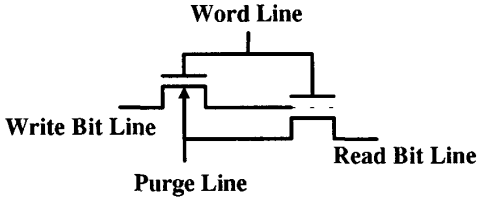

Fig.2 CDRAM circuit analogy.

Table I.
CDRAM device parameters used in simulation.

Gate Oxide Thickness	80 Å
Silicon Film Thickness	1600 Å
Buried Oxide Thickness	2000 Å
n^{++}/p Junction Depth	800 Å

Table II.
Voltages applied in simulation.

W/BL's / Function	WL	PL	RBL &WBL
HOLD	3	-1.5	0
READ "1"	0	-1.5	< 0
READ "0"			0
PURGE	-1.5	0	~ 0
WRITE "1"	3	0	0
WRITE "0"			0.6

A. HOLD

In the HOLD (stand-by) state, WL is biased at a high voltage (3V) and PL is biased at a negative voltage (-1.5V). In this condition, the n-type floating body is biased into accumulation. However the electrons from WBL to supply the accumulation layer is controlled by the p type silicon (PL) surrounding the floating body. Depending on whether the electrons supply is available, a deep potential well for state "0," or a shallow potential well for state "1" is formed as seen in Fig.3. Since electrons can diffuse in or out of the potential well and generation/recombination can occur, refreshing the cell is needed.

B. READ

In the READ operation the WL voltage is lowered. The electron potential energy of the floating body is raised by capacitance coupled from WL. At the same time, the hole barrier between RBL and PL is lowered. Note that the hole barrier is lower at the back channel due to weaker WL coupling (Fig.4). With WL voltage large enough, the hole barrier can be so low that a hole current will flow from RBL to PL via the SOI back channel as seen in Fig.5. It is clearly seen from Fig.3 that the CDRAM cell of state "1" can be turned on at a larger WL voltage than the one of state "0," because of electrons stored in the front accumulation layer. This layer has a function similar to that of the floating gate of an EPROM cell. When the READ voltage is properly chosen, the two states in Fig.3 can be distinguished as seen in Fig.6 and 7. Note that the READ signal is a DC-like current instead of a pulse charging signal in ordinary DRAM. Fig.6 and 7 show that the READ current difference between the "1" state and the "0" state can be larger than 100 μA/μm.

It should be noted that the electron barrier is also lower during READ, therefore electrons can get out of the floating body, which in turn reduces the PMOSFET READ current. The READ current thus decreases with the reading time (Fig.7). Note that the polarity between the biases of RBL and PL need to be considered. We have chosen to bias RBL at a higher voltage than PL. This is because if the opposite polarity is used, electrons will diffuse out of the floating body more easily to WBL through the narrow p^+ barrier and the READ current will decay more rapidly.

C. WRITE

Writing "1" into the CDRAM cell is done by first raising the WL voltage to form a potential well in the floating body. Then the p^+ electron barrier between the floating body and WBL is lowered using either PL. In other words, to turn on the WRITE NMOSFET. Electrons will continue to flow into the floating body to "fill" the potential well until the conduction bands of the floating body and WBL are aligned (Fig.8). After WRITE, the electron barrier is raised

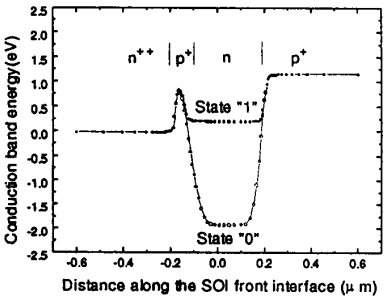

Fig.3 Front channel conduction band energy of the CDRAM cell for memory state "0" and state "1" at HOLD (stand-by).

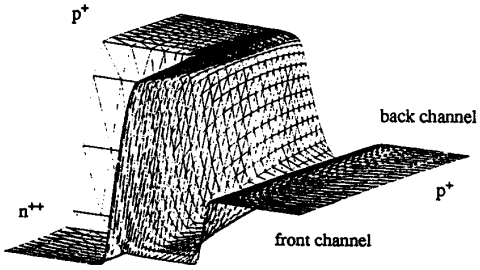

Fig.4 The quasi-3D plot of the valence band energy contour. Holes are likely to flow via the back channel from RBL to PL.

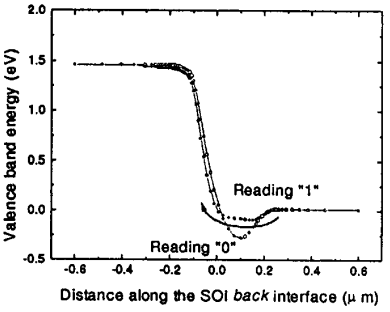

Fig.5 *Back* channel valence band energy of the CDRAM cell for memory state "0" or state "1" when it is read.

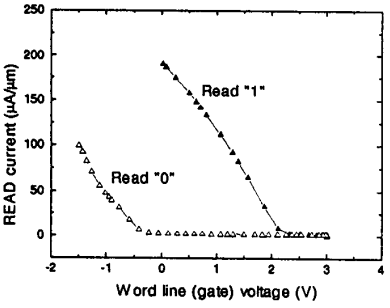

Fig.6 The memory window between state "1" and "0."

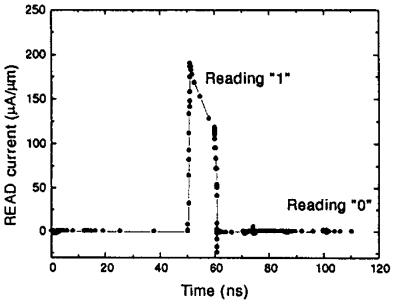

Fig.7 The transient simulation of the bit line current of a CDRAM cell for both reading "1" and reading "0."

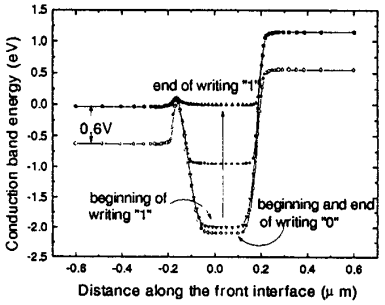

Fig.8 Front channel conduction band energy of the CDRAM cell for writing state "0" or writing state "1."

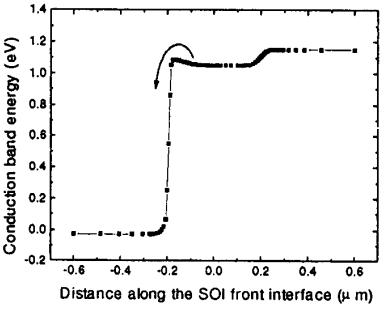

Fig.9 Front channel conduction band energy of the CDRAM cell during PURGE. Electrons are expelled out of the floating body.

again (PL being pulled to -1.5V) to keep the electrons in the floating body. Writing "0" into the CDRAM cell is done by the same procedure, except that WBL is now biased at 0.6V instead of 0V in the case of writing "1." With this additional barrier of 0.6eV, the WRITE NMOSFET will not be turned on, and electrons can not flow into the floating body (Fig.8). It is noted that the CDRAM cell can be written with "0" only from a previous "0" state. Thus a "PURGE" operation to reset every cell back to "0" is needed prior to every WRITE.

D. PURGE

The PURGE operation is to expel the electrons out of the floating body. It can be done by raising the floating body potential (by applying a negative voltage to WL) and reducing the electron barrier between the floating body and WBL by raising the PL potential (Fig.9). Once the cell is purged, it can be written with "0" or "1" using the WRITE scheme described above.

CDRAM ARRAY ARCHITECTURE

It was projected that the technology for 256 Mb DRAM will have a minimum feature size 0.25μm and a cell area $0.5\mu m^2$[1]. This is approximately the cell area with folded-bit line architecture which usually takes $8(F+a)^2$ per cell[8], where F is the minimum feature size and a is the alignment error. Folded-bit line architecture is used to suppress common mode noise during conventional DRAM sensing. However in gain cells such as CDRAM with large READ signal, folded-bit line architecture might not be necessary[2]. The insulating substrate can also help reduce the noise coupled through substrate. Moreover, single-ended sensing scheme is feasible for CDRAM. A $4(F+a)^2$ cell-size CDRAM array is proposed in Fig.10 with one-level metal and one-level polysilicon. A single bit line BL is used for both RBL and WBL to fit the CDRAM cell into one metal pitch per column. WL is formed by the gate. PL is formed by p+ diffusion. The cross section of the memory array along BL is shown in Fig.11. As can be seen the structure and process are rather simple compared with the that of the state-of-the-art DRAM technology. The operating voltages of the CDRAM array are identical to that in table II. The price paid for sharing BL between RBL and WBL is that the READ and WRITE operations can not be optimized separately, and the BL voltage swing is limited to about 0.6V to avoid disturbing the cells in unselected rows. It is also noted that two WLs are sharing one PL. Thus when WL1 in Fig.10 is selected for PURGE or WRITE with PL at 0V, WL2 should be biased at 1.5V to avoid disturbance of data.

CONCLUSION

CDRAM has a large READ current gain while its cell unit is comparable to the size of a single transistor. No extra storage capacitor is needed. Its structure and fabrication process are rather simple and planar as compared to that of the ordinary one transistor/one capacitor DRAM cell. The process is compatible with the general-purpose SOI CMOS process. This is particularly attractive for the role of being the technology driver. We have described the memory operations in detail and proposed a $4(F+a)^2$ cell-size CDRAM array. CDRAM is a promising candidate of gigabit-bit memory device.

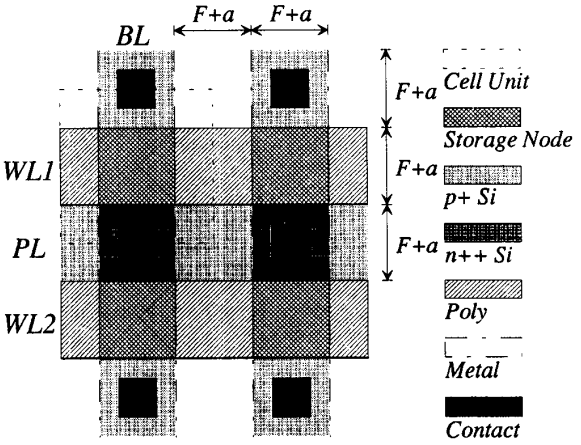

Fig.10 CDRAM array layout with $4(F+a)^2$ cell area.

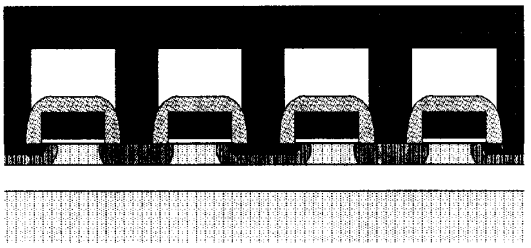

Fig.11 CDRAM array cross section along BL.

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