UNIVERSITY OF CALIFORNIA, SANTA BARBARA
Department of Electrical and Computer Engineering

Assignment #2

Due Date: Feb 28, 2011

Weekly Reading Assignment Reminder: Read the reference papers posted under each week.

1. Show that the minimum required V_{dd} for a digital CMOS logic circuit is given by a few times kT/q (= 26 mV). Hint: Consider an inverter circuit and remember that we must have gain>1. What will be the minimum V_{dd} for NMOS only designs? You must support your answers through detailed (theoretical) analysis.

2. The objective of this exercise is to develop a detailed understanding of the effect of supply voltage scaling on circuit performance, power dissipation, and robustness. Consider a minimum size CMOS inverter in a 45 nm technology node. The technology files can be found here: http://ptm.asu.edu Use the 45nm PTM HP model. You can use the "Latest Models" link to download the model, and change the device parameters in the model, or you can use the "Nano-CMOS" link on the PTM website to customize the model.
   i) Using SPICE simulations, plot the effect of V_{dd} scaling (while keeping V_{th} fixed) on the delay, power dissipation (various components), noise margins and the DC transfer curve of the CMOS inverter. Vary V_{dd} from the recommended value for the technology node to 26 mV. Summarize your observations.
   ii) Repeat (i) assuming V_{th} scaling at the same rate (as V_{dd}) and at half the rate (as V_{dd}). Provide a summary of the observations.
   iii) Repeat (i) and (ii) for a resistive-load inverter. Summarize your findings.
   iv) Repeat (i) and (ii) for a pseudo-NMOS inverter. Summarize your findings.
   v) Repeat (i) and (ii) for a pass-transistor based inverter. Summarize your findings.
   vi) Repeat (i) and (ii) for a dynamic inverter. Summarize your findings.
   vii) Repeat (i) and (ii) for a tri-state inverter. Summarize your findings.