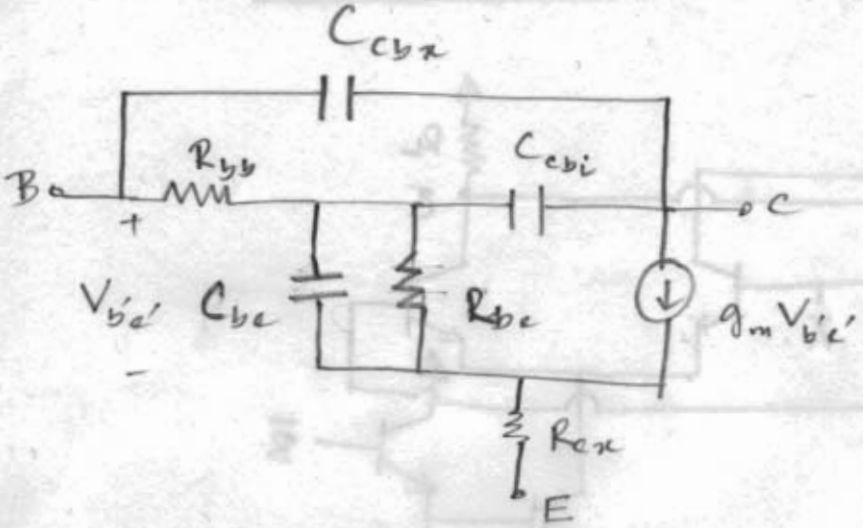
Homework 5 Solutions



This operates at a maximum of 12 $mA/\mu m^2$

Small signal parameters:

$C_{be} = C_{be,depl} + g_m \tau_f$

$C_{be,depl} = 32\,fF$

$\beta = 50$

$C_{cbi} = 2.2\,fF$, $C_{cbx} = 6\,fF$

$R_{bb} = 38\,\Omega$, $R_{ex} = 2.8\,\Omega$

for $A_E = 0.6\,\mu m \times 4.3\,\mu m$
$= 2.58\,\mu m^2$

1. The transistors carry a peak of 6 mA at $5\,mA/\mu m^2$

$\Rightarrow$ The transistors area can be scaled to $1.2\,\mu m^2$ emitter area. New small signal device parameters for this scaled down device are:

$$C'_{be,depl} = C_{be,depl} \times \frac{1.2}{2.58} = 14.88\,fF$$

$$C'_{cbi} = C_{cbi} \times \frac{1.2}{2.58} = 1.02\,fF$$

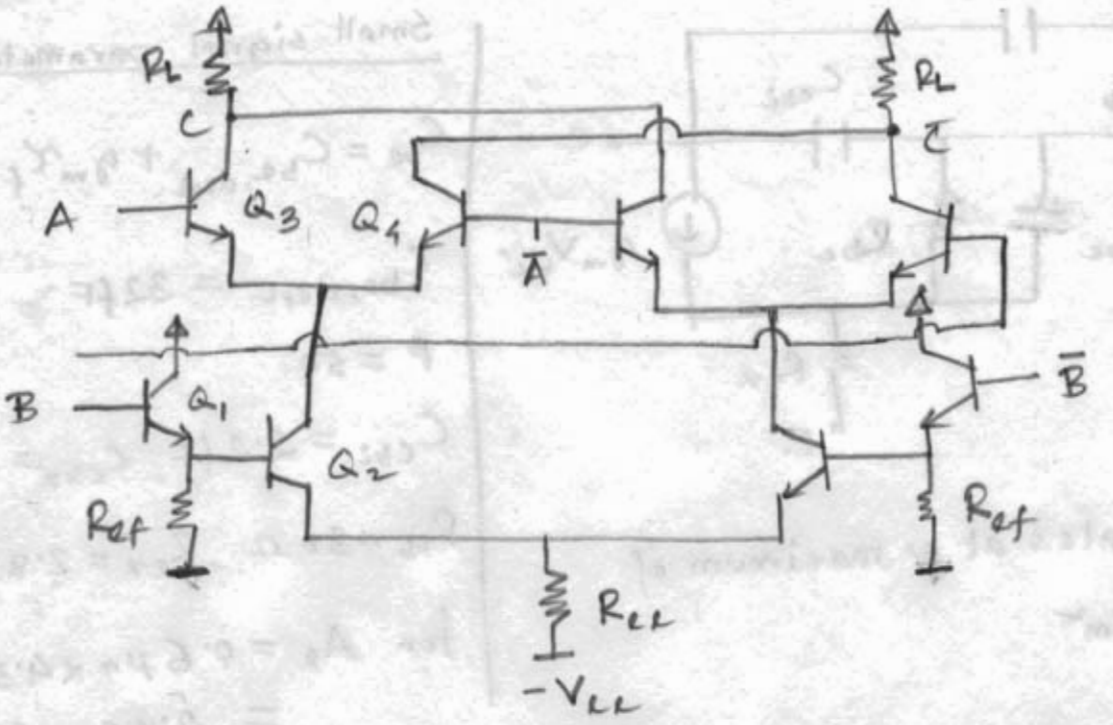
$$C'_{cbx} = C_{cbx} \times \frac{1.2}{2.58} = 2.79\,fF$$

$$R'_{bb} = R_{bb} \times \frac{1.2}{2.58} = 17.67\,\Omega$$

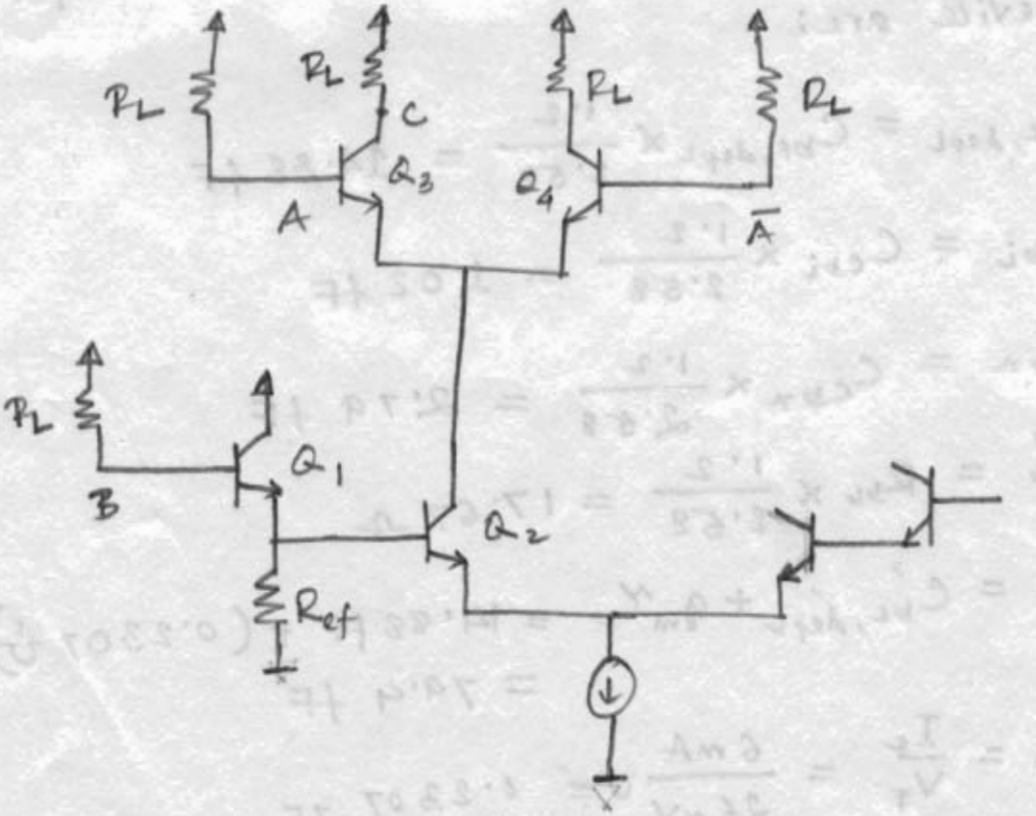
$$C'_{be} = C'_{be,depl} + g_m \tau_f = 14.88\,fF + (0.2307\,\mho)(0.28\,ps)$$
$$= 79.4\,fF$$

$$g_m = \frac{I_c}{V_T} = \frac{6\,mA}{26\,mV}\,\mho = 0.2307\,\mho$$

Circuit diagram for a CML XOR gate:



An equivalent half circuit for ease of analysis can be drawn as:



Since the transistors are being used for switching purposes, they are non-linear devices and we will have to use the large signal analysis where —

capacitance, $C = \frac{\Delta Q}{\Delta V}$

transconductance, $g_m = \frac{\Delta I}{\Delta V}$,

where ΔV = Logic swing

As a result,

$$g_{mL} = g_{m,\text{large signal}} = \frac{\Delta I}{\Delta V} = \frac{I_o}{I_o R_L} = \frac{1}{R_L} << \frac{q I_o}{kT}$$

$$C_{be,\text{diffusion}} = \frac{\Delta Q}{\Delta V} = \frac{I_o \tau_f}{\Delta V} = \frac{\tau_f}{R_L} << g_m \tau_f$$

$$A_{v,\text{large signal}} = \frac{\Delta V_{out}}{\Delta V_{in}} = -1$$

$$C_{cb,\text{large signal}} = \frac{\Delta Q}{\Delta V} = \frac{C_{cb} \cdot \Delta V}{\Delta V} = C_{cb}$$

Thus, the effective values of g_m and C_{be} have been reduced by roughly a factor of 10 for large signal analysis. $\left(\because \frac{\Delta V_{logic}}{\left(\frac{kT}{q}\right)} \approx 10:1 \right)$

Now, for gate propagation delay analysis, replace the switching transistors by their equivalent large signal models.

If the circuit has a transfer function:

$$\frac{V_{out}}{V_{in}} = \left[\frac{V_{out}}{V_{in}}\right]_{MB} \times \left[\frac{1 + b_1 s + b_2 s^2 + \cdots}{1 + a_1 s + a_2 s^2 + \cdots}\right]$$

Mean delay of transfer function $= (a_1 - b_1)$

Half the mean delay (Delay to 50% switching points)

$$T_{gate} = \frac{a_1 - b_1}{2}$$

where, a_1 is determined by MOTC

and $b_1 = \sum \frac{C_{be}}{g_m} - \sum \frac{C_{cb}}{g_{m,\,large\,signal}}$

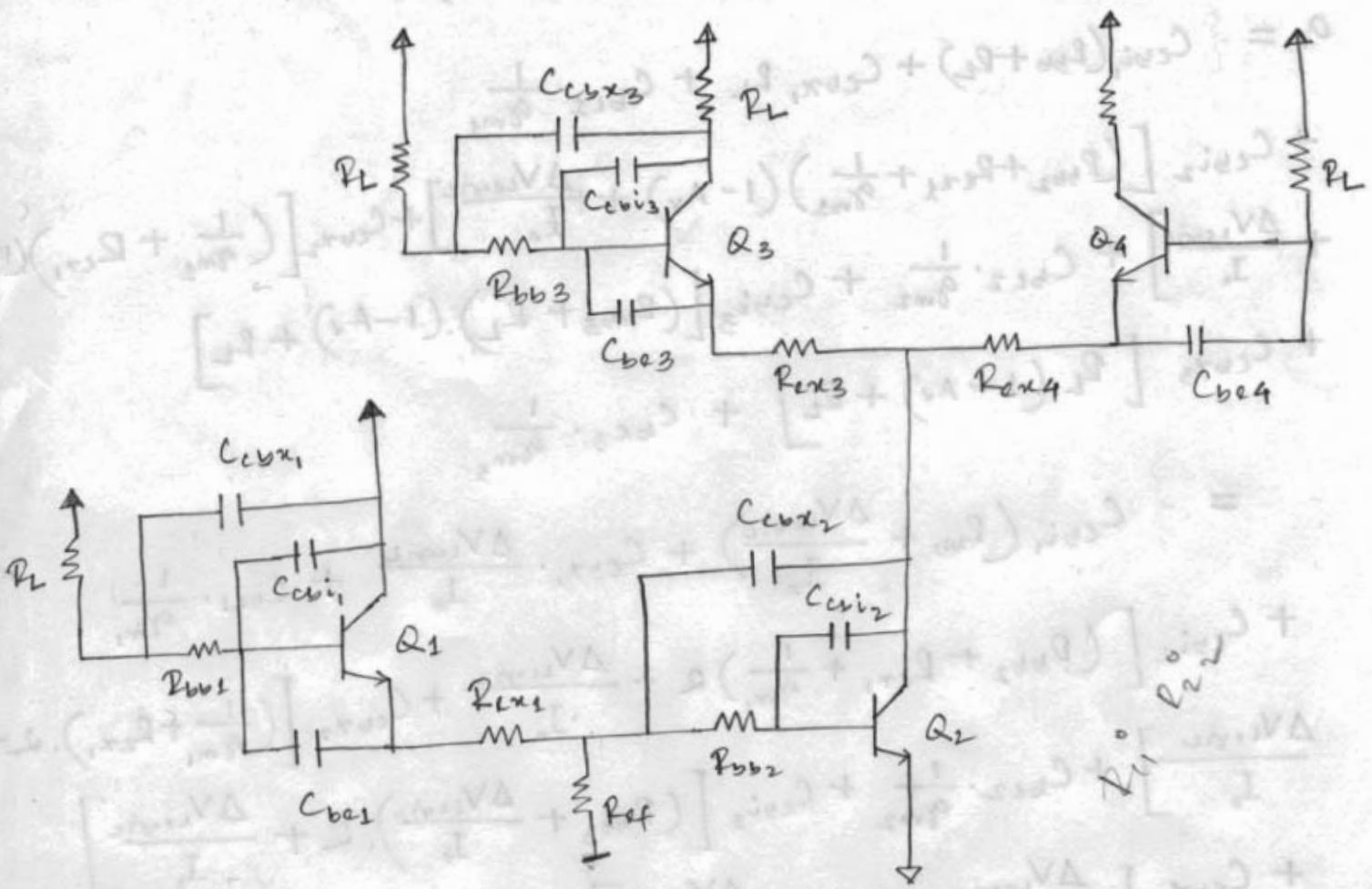
(Emitter followers) (common emitter stages)

Note: We use small signal value of g_m for emitter followers as they are not the switching elements.

Also, we neglect 2nd order effects a_2 in the circuit transfer function.

⇒ Emitter follower ringing is neglected.

Equivalent Half circuit with all the parasitic capacitances



Here, Q_1 is in emitter follower configuration

Q_2 is a common emitter

Q_3 is a common emitter

Assume that gain of $Q_2 \approx 1$

Logic voltage swing at collector of $Q_2 \approx \Delta V_{Logic}$

Applying MOTC in the half circuit,

$$a_1 = C_{cbi_1}(R_{bb}+R_L) + C_{cbx_1}R_L + C_{be1}\cdot\frac{1}{g_{m_1}}$$
$$+ C_{cbi_2}\left[\left(R_{bb_2}+R_{ex_1}+\frac{1}{g_{m_1}}\right)(1-A_v)+\frac{\Delta V_{Logic}}{I_o}\right] + C_{cbx_2}\left[\left(\frac{1}{g_{m_1}}+R_{ex_1}\right)(1-A_v)\right.$$
$$\left.+\frac{\Delta V_{Logic}}{I_o}\right] + C_{be2}\cdot\frac{1}{g_{m2}} + C_{cbi_3}\left[(R_{bb_3}+R_L)(1-A_v)+R_L\right]$$
$$+ C_{cbx_3}\left[R_L(1-A_v)+R_L\right] + C_{be_3}\cdot\frac{1}{g_{m_3}}$$

$$= C_{cbi_1}\left(R_{bb}+\frac{\Delta V_{Logic}}{I_o}\right) + C_{cbx_1}\cdot\frac{\Delta V_{Logic}}{I_o} + C_{be1}\cdot\frac{1}{g_{m_1}}$$
$$+ C_{cbi_2}\left[\left(R_{bb_2}+R_{ex_1}+\frac{1}{g_{m_1}}\right)2+\frac{\Delta V_{Logic}}{I_o}\right] + C_{cbx_2}\left[\left(\frac{1}{g_{m_1}}+R_{ex_1}\right).2+\right.$$
$$\left.\frac{\Delta V_{Logic}}{I_o}\right] + C_{be2}\cdot\frac{1}{g_{m2}} + C_{cbi_3}\left[\left(R_{bb_3}+\frac{\Delta V_{Logic}}{I_o}\right).2+\frac{\Delta V_{Logic}}{I_o}\right]$$
$$+ C_{cbx_3}\left[\frac{\Delta V_{Logic}}{I_o}.2+\frac{\Delta V_{Logic}}{I_o}\right] + C_{be_3}\cdot\frac{1}{g_{m3}} \qquad \text{——— (I)}$$

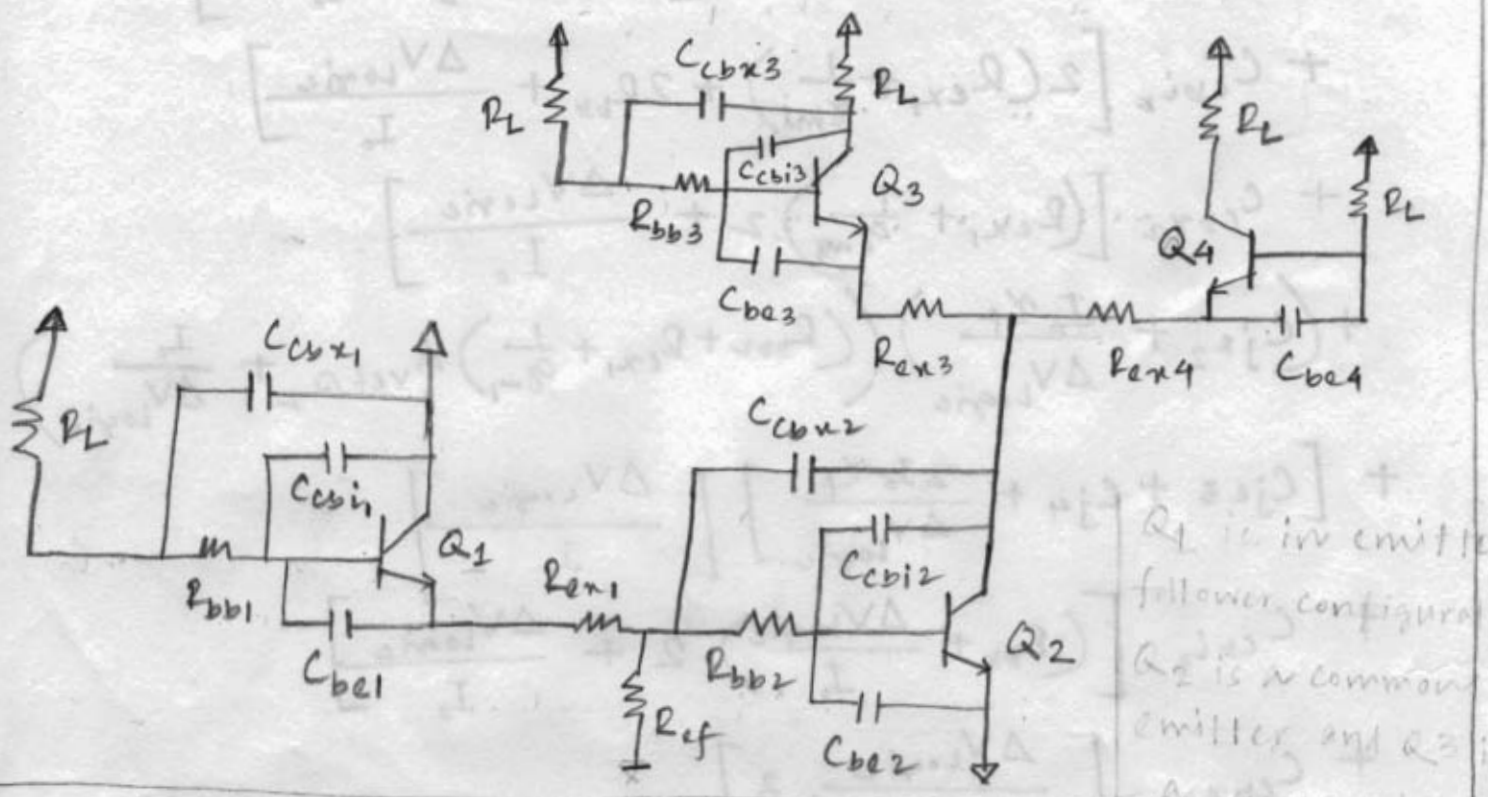
Now, $b_1 = \sum \frac{C_{be}}{g_m} - \sum \frac{C_{cb}}{g_{m,\,large\ signal}}$

(Emitter follower) (Common emitter)

$$= C_{be_1}\cdot\frac{1}{g_{m_1}} - \left(C_{cbi_2}+C_{cbx_2}\right)\cdot\frac{1}{g_{m_2}} - \left(C_{cbi_3}+C_{cbx_3}\right)\cdot\frac{1}{g_{m_3}}$$

——— (II)

Equivalent Half circuit with all the parasitic capacitances:



Now, if T_{gate} = propagation delay, and

$2T_{gate} = a_1 - b_1$

$$\Rightarrow 2\times T_{gate} = \left\{C_{cbi_1}\left(R_{bb}+\frac{\Delta V_{logic}}{I_o}\right) + C_{cbx_1}\left(\frac{\Delta V_{logic}}{I_o}\right) + C_{be1}\cdot\frac{1}{g_{m_1}}\right.$$

$$+ C_{cbi_2}\left[\left(R_{bb_2}+R_{ex_1}+\frac{1}{g_{m_1}}\right).2+\frac{\Delta V_{logic}}{I_o}\right] + C_{cbx_2}\left[\left(\frac{1}{g_{m_1}}+R_{ex_1}\right).2+\frac{\Delta V_{logic}}{I_o}\right]$$

$$+ C_{be_2}\cdot\frac{1}{g_{m_2}} + C_{cbi_3}\left[\left(R_{bb3}+\frac{\Delta V_{logic}}{I_o}\right).2+\frac{\Delta V_{logic}}{I_o}\right] + C_{cbx_3}\left[\frac{\Delta V_{logic}}{I_o}.2+\right.$$

$$\left.\left.\frac{\Delta V_{logic}}{I_o}\right] + C_{be_3}\cdot\frac{1}{g_{m_3}}\right\} - C_{be_1}\cdot\frac{1}{g_{m_1}} + \left(C_{cbi_2}+C_{cbx_2}\right)\frac{1}{g_{m_2}}$$

$$+ \left(C_{cbi_3}+C_{cbx_2}\right)\frac{1}{g_{m_3}}$$

Thus,

$$2T_{gate} = C_{cbi_1}\left[R_{bb} + \frac{\Delta V_{logic}}{I_o}\right] + C_{cbx_1}\left[\frac{\Delta V_{logic}}{I_o}\right]$$

$$+ C_{cbi_2}\left[2\left(R_{ex_1} + \frac{1}{g_{m1}}\right) + 2R_{bb} + \frac{\Delta V_{logic}}{I_o}\right]$$

$$+ C_{cbx_2}\left[\left(R_{ex_1} + \frac{1}{g_{m_1}}\right)2 + \frac{\Delta V_{logic}}{I_o}\right]$$

$$+\left(C_{je_2} + \frac{I_o \tau_f}{\Delta V_{logic}}\right)\left(\left(R_{bb2} + R_{ex_1} + \frac{1}{g_{m_1}}\right) A_{vef} Q_2 + \frac{I_o}{\Delta V_{logic}}\right)$$

$$+ \left[C_{je3} + C_{j4} + \frac{2I_o\tau_f}{\Delta V_{logic}}\right]\left[\frac{\Delta V_{logic}}{I_o}\right]$$

$$+ C_{cbi_3}\left[\left(R_{bb} + \frac{\Delta V_{logic}}{I_o}\right).2 + \frac{\Delta V_{logic}}{I_o}\right]$$

$$+ C_{cbx_3}\left[\frac{\Delta V_{logic}}{I_o}.3\right]$$

$$+ \left(C_{cbi_2} + C_{cbx_2}\right)\left(\frac{I_o}{\Delta V_{logic}}\right) + \left(C_{cbi_3} + C_{cbx_3}\right)\left(\frac{I_o}{\Delta V_{logic}}\right)$$

where —

$C_{cbi} = 1{\cdot}02$ fF

$C_{cbx} = 2{\cdot}79$ fF

$R_{bb} = 17{\cdot}67\ \Omega$

$R_{ex} = 2{\cdot}8\ \Omega$

$g_{m1} = 0{\cdot}2307\ \mho$

$\tau_f = 0{\cdot}28$ psec

$C_{je} = 14{\cdot}88$ fF

$I_o = 6$ mA

$\Delta V_{logic} = I_o R_L$

$= 6\text{ mA} \times 50\ \Omega$

$= \underline{\underline{0{\cdot}3\text{ V}}}$

Thus,

$$2T_{gate} = 1.02\,fF\left[17.67 + \frac{0.3V}{6\,mA}\right] + 2.79\,fF\left[\frac{0.3V}{6\,mA}\right]$$

$$+ 1.02\,fF\left[2(2.8+4.33)+2\times17.67+50\right]$$

$$+ 2.79\,fF\left[2(2.8+4.33)+50\right]$$

$$+ \left(14.88\,fF + \frac{0.28\,psec}{50\,\Omega}\right)\left[(17.67+2.8+4.33)\,0.3 + 0.02\right]$$

$$+ \left[2\times14.88\,fF + \frac{2\times0.28\,psec}{50}\right]\left[50\right]$$

$$+ 1.02\,fF\left[(17.67+50)\,2 + 50\right]$$

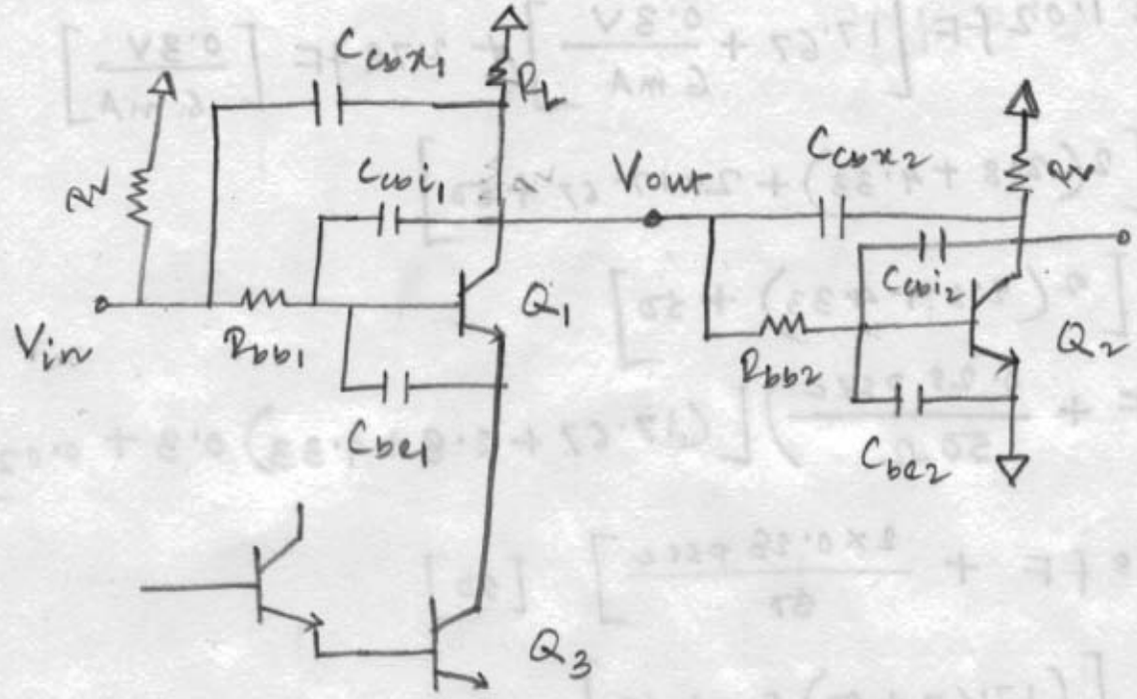
$$+ 2.79\,fF \times 150 + \frac{3.81\,fF}{50} + \frac{3.81\,fF}{50}$$

$$= 69.02\,f_s + 139.5\,f_s + 101.592\,f_s$$
$$+ 179.28\,f_s + 152.7\,f_s + 2048\,f_s$$
$$+ 189\,f_s + 418.5\,f_s + 0.0762\,f_s$$

$$= 3297.16\,f_{sec}$$

$$\Rightarrow T_{gate} = 1648\ f_{sec} = \underline{\underline{1.64\ psec}}$$

A level propagation delay when the signal is propagated between successive stages on A level inputs alone :



$$a_1 = C_{be1}(R_{bb}+R_L) + C_{cbi}\left((R_L+R_{bb})(1-A_v) + R_L\right)$$
$$+ C_{cbx}\left[R_L(1-A_v) + R_L\right]$$
$$= \left(C_{je} + \frac{I_o \tau_f}{\Delta V_{logic}}\right)\left(R_{bb} + \frac{\Delta V_{logic}}{I_o}\right) + C_{cbi}\left(\left(R_{bb} + \frac{\Delta V_{logic}}{I_o}\right).2 + \frac{\Delta V_{logic}}{I_o}\right) + C_{cbx}\left[\frac{\Delta V_{logic}}{I_o}.2 + \frac{\Delta V_{logic}}{I_o}\right]$$

$$b_1 = -\left(C_{cbx} + C_{cbi}\right)\frac{\Delta V_{logic}}{I_o}$$

$$2T_{gate} = a_1 - b_1 = \left(C_{je} + \frac{I_o \tau_f}{\Delta V_{logic}}\right)\left(R_{bb} + \frac{\Delta V_{logic}}{I_o}\right)$$
$$+ C_{cbi}\left[\left(R_{bb} + \frac{\Delta V_{logic}}{I_o}\right).2 + 2.\frac{\Delta V_{logic}}{I_o}\right]$$
$$+ C_{cbx}\left[4.\left(\frac{\Delta V_{logic}}{I_o}\right)\right]$$

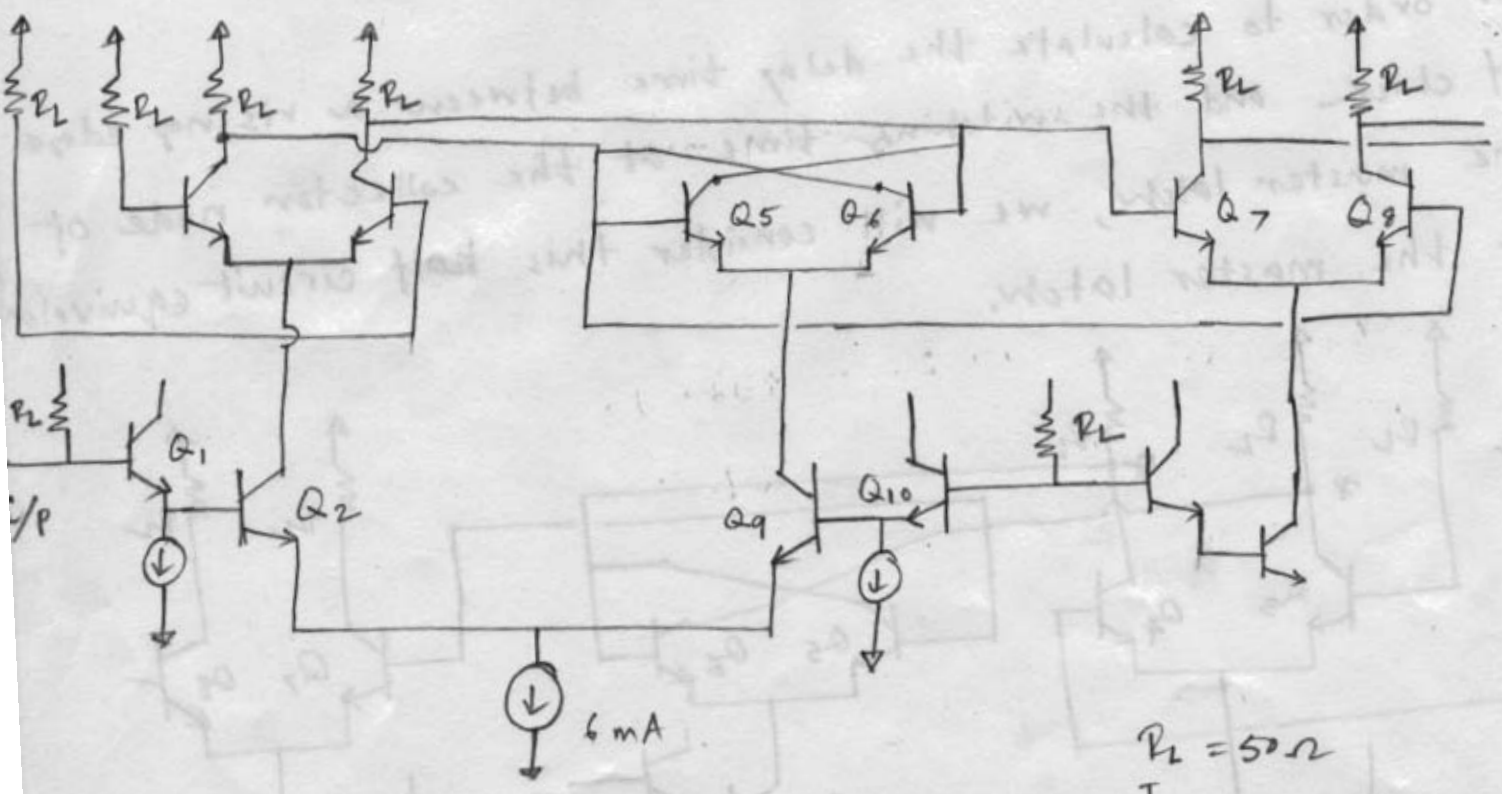
$$\Rightarrow 2T_{gate} = \left(14.88\ fF + \frac{0.28\ psec}{50}\right)(17.67 + 50)$$

$$+ \ 1.02\ fF\,(2 \times 17.67 + 4 \times 50) + 2.79\,(4 \times 50)$$

$$\Rightarrow 2T_{gate} = 2183\ fs$$

$$\therefore T_{gate} = 1.091\ psec$$

2. Schematic for a master-slave latch:



$R_L = 50\,\Omega$

$I_{Bias} = 6\ mA$

The scaling for transistors in order to operate at $5mA/\mu m^2$ when turned on proceeds as in the previous solution.

Transistor emitter area, $A_E = \frac{6mA}{5mA/\mu m^2} = 1.2\ \mu m^2$

Small signal parameters for the scaled down model

$$C'_{be,depl} = C_{be,depl} \times \frac{1.2}{2.58} = 14.88\ fF$$

$$C'_{cbi} = C_{cbi} \times \frac{1.2}{2.58} = 1.02\ fF$$

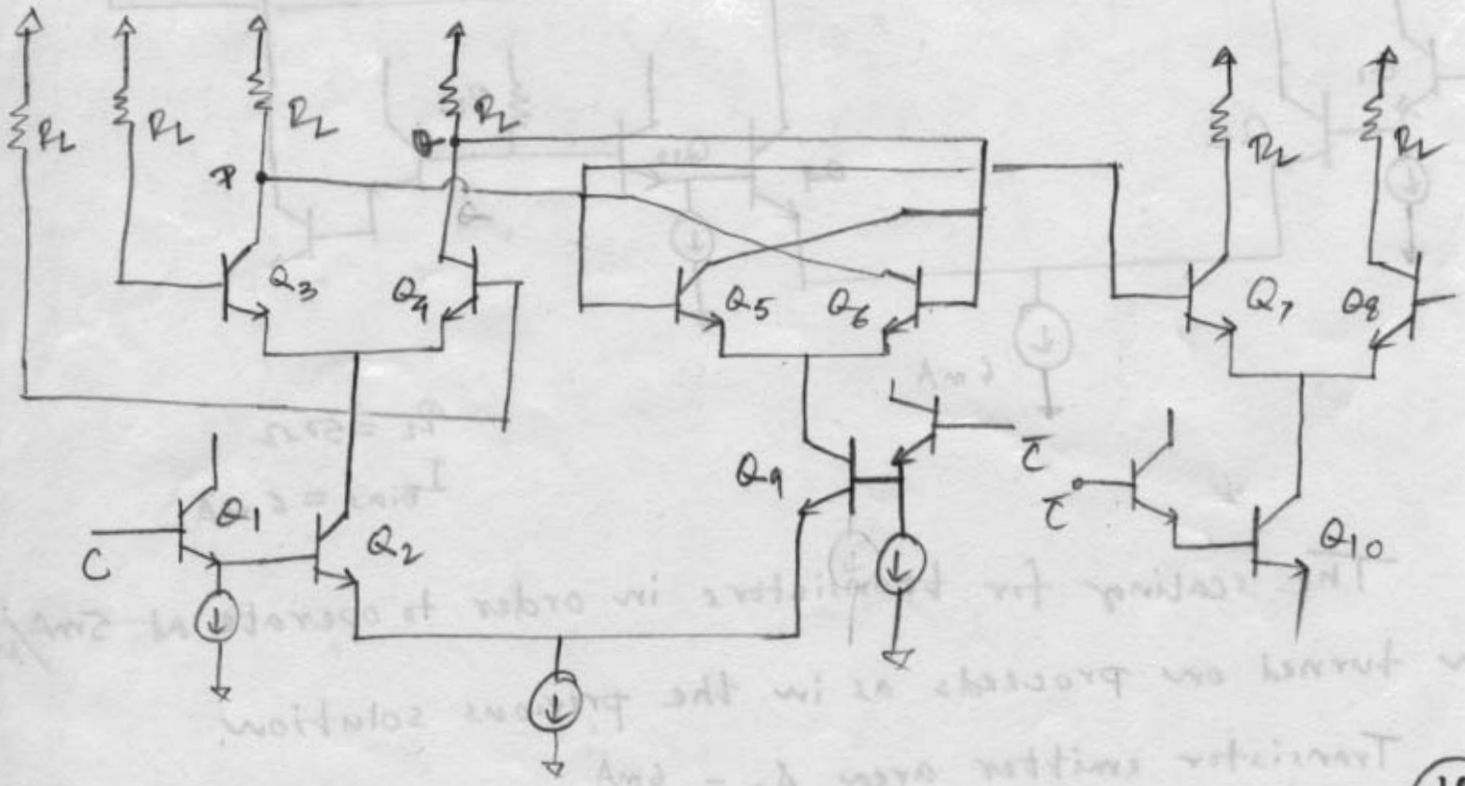
$$C'_{cbx} = C_{cbx} \times \frac{1.2}{2.58} = 2.79\ fF$$

$$R_{bb'} = R_{bb} \times \frac{1.2}{2.58} = 17.67\ \Omega$$

$$g_m = \frac{I_c}{V_T} = 0.2307\ \mho$$

$$\tau_f = 0.28\ psec$$

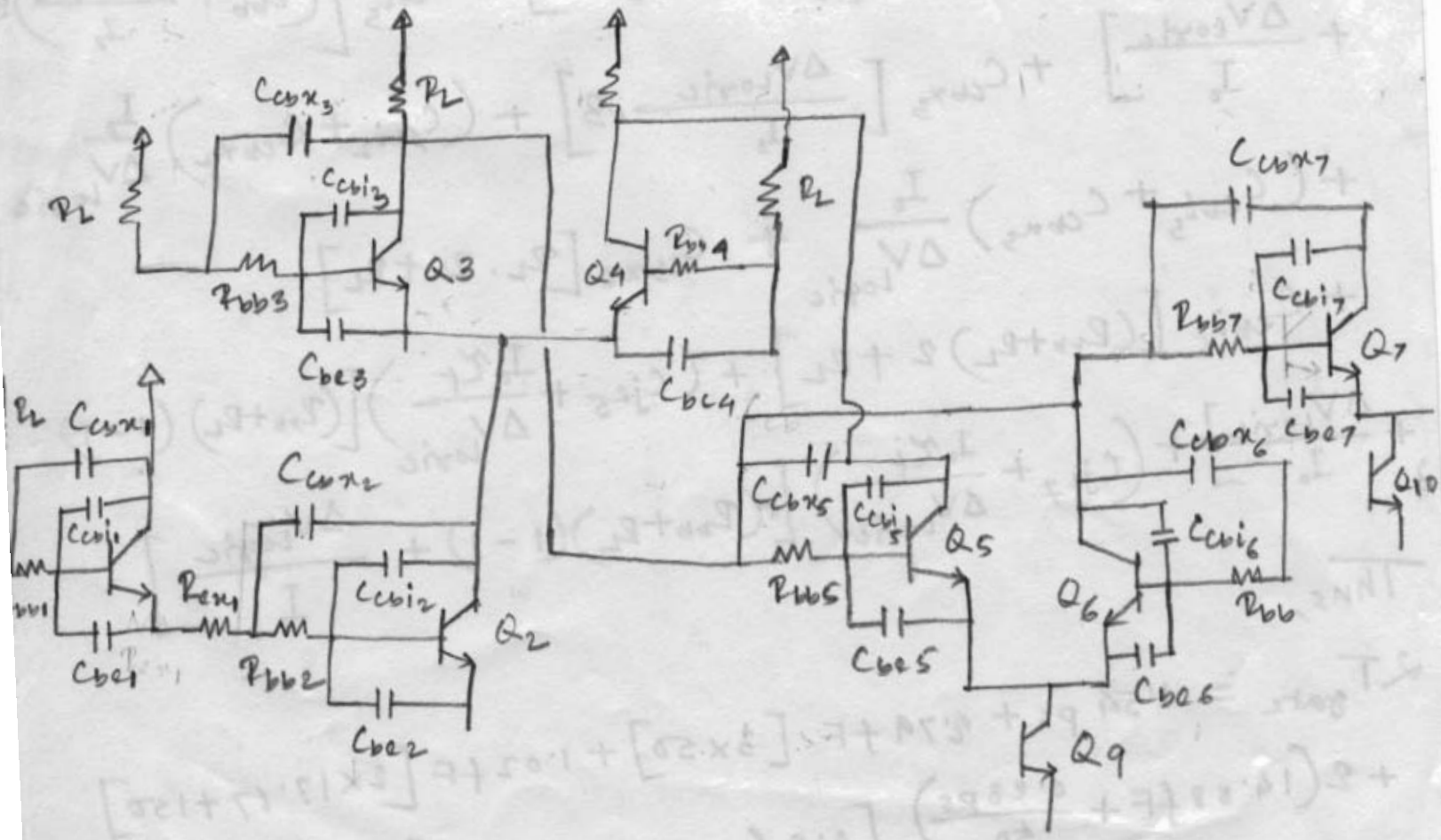
In order to calculate the delay time between a rising edge of clock and the switching time at the collector node of the master latch, we will consider this half circuit equivalent for the master latch.



We need to measure the delay between switching at points C and P.

The delay calculations for switching of transistors $Q_1 - Q_4$ will be similar to previous solution, however, there will be an additional delay at the node P due to the time required for charging capacitances C_{beQ5}, C_{cbQ6} and C_{beQ7}. A similar argument holds good for node Q as well.

Equivalent half circuit with all the parasitic capacitance:



Assume logic swings at collectors of Q9 and Q10 to be ΔV_{logic}

If T_{gate} = Delay time

$$2T_{gate} = C_{cbi_1}\left(R_{bb} + \frac{\Delta V_{Logic}}{I_o}\right) + C_{cbx_1}\left(\frac{\Delta V_{Logic}}{I_o}\right)$$

$$+ C_{cbi_2}\left[2\left(R_{ex_1} + \frac{1}{g_{m_1}} + R_{bb}\right) + \frac{\Delta V_{Logic}}{I_o}\right]$$

$$+ C_{cbx_2}\left[2\left(R_{ex_1} + \frac{1}{g_{m_1}}\right) + \frac{\Delta V_{Logic}}{I_o}\right]$$

$$+ \left(C_{je_2} + \frac{I_o \tau_f}{\Delta V_{logic}}\right)\left[\left(R_{bb_2} + R_{ex_1} + \frac{1}{g_{m_1}}\right) A_{of\,Q2} + \frac{I_o}{\Delta V_{Logic}}\right]$$

$$+ \left[C_{je_3} + C_{j4} + \frac{2 I_o \tau_f}{\Delta V_{Logic}}\right]\left[\frac{\Delta V_{Logic}}{I_o}\right] + C_{cbi_3}\left[\left(R_{bb} + \frac{\Delta V_{Logic}}{I_o}\right)2 + \frac{\Delta V_{Logic}}{I_o}\right]$$

$$+ C_{cbx_3}\left[\frac{\Delta V_{Logic}}{I_o} \cdot 3\right] + \left(C_{cbi_2} + C_{cbx_2}\right)\frac{I_o}{\Delta V_{logic}}$$

$$+ \left(C_{cbi_3} + C_{cbx_3}\right)\frac{I_o}{\Delta V_{logic}} + C_{cbx_6}\left[R_L \cdot 2 + R_L\right]$$

$$+ C_{cbi_6}\left[(R_{bb} + R_L)2 + R_L\right] + \left(C_{je_5} + \frac{I_o \tau_f}{\Delta V_{logic}}\right)\left[(R_{bb} + R_L)(1-1) + \frac{\Delta V_{Logic}}{I_o}\right]$$

$$+ \left(C_{je_7} + \frac{I_o \tau_f}{\Delta V_{Logic}}\right)\left[(R_{bb} + R_L)(1-1) + \frac{\Delta V_{Logic}}{I_o}\right]$$

Thus,

$$2T_{gate} = 1.54\,ps + 2.79\,fF\,[3 \times 50] + 1.02\,fF\,[2 \times 17.67 + 150]$$

$$+ 2\left(14.88\,fF + \frac{0.28\,ps}{50}\right)[0.3(17.67 + 50) + 50]$$

$= 3.297\,ps + 418.5\,fs + 189.04\,fs + 2048.52\,fs$

$= 5952.54\,fs$

$\therefore T_{gate} = 2976.27\,fsec = 2.97\,psec$

Maximum clock frequency $= \frac{1}{2T_{gate}} = \underline{\underline{167.9\ GHz}}$