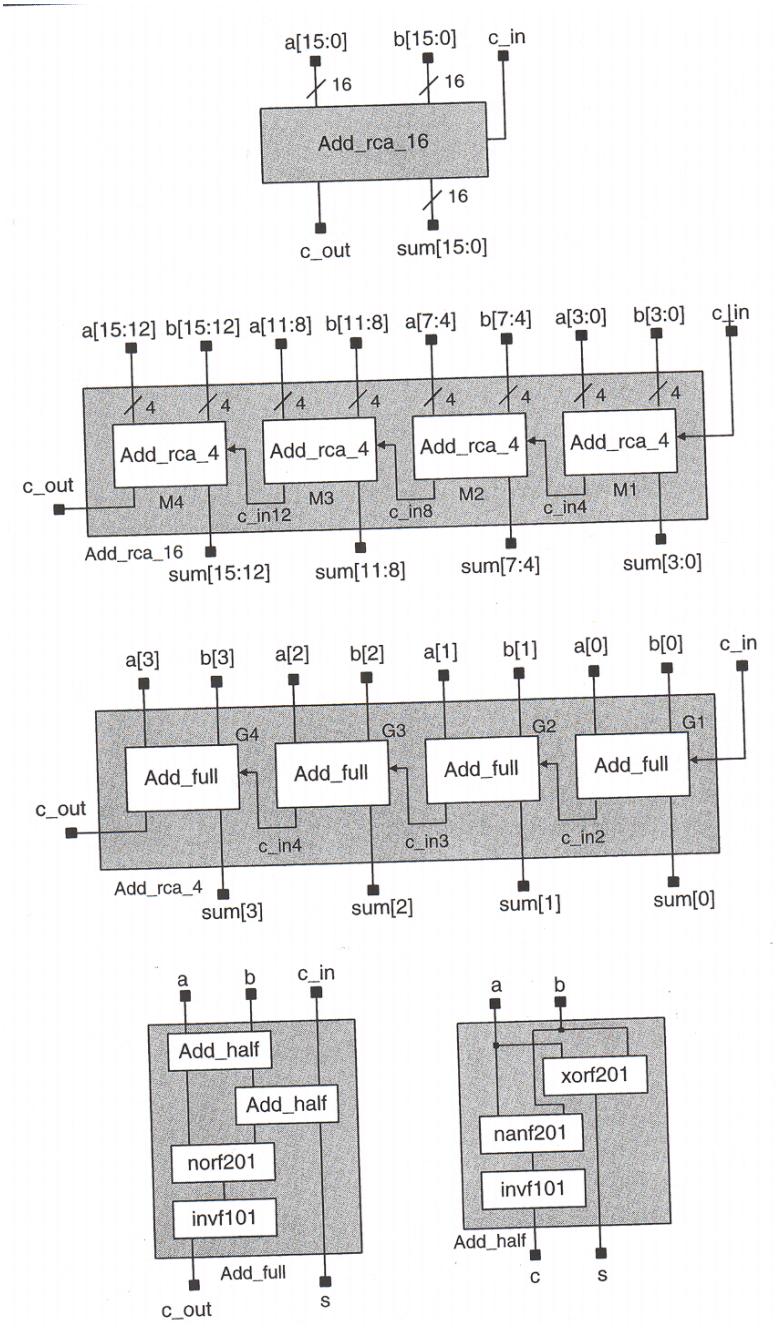
VERILOG HOMEWORK ASSIGNMENT

1. The hierarchical decomposition of a 16-bit ripple-carry adder is presented in the figure below. This example will illustrate the relationship between module declarations and instantiations. The top-level module contains four instantiations of four-bit slice adders, which themselves contain instantiations of full adders, each of which contains half adders and glue logic; the half adders are defined in terms of modules declared in a cell library.



Construct the 16 bit full adder in verilog using module instantiations of the lower level blocks. As an example, add_half looks like this:

```
module Add_half(s, c, a, b);
     output          s, c;
     input           a, b;
     wire            c_bar;

     xorf201   G1(s, a, b);
     nanf201   G2(c_bar, a, b);
     invf101   G3(c, c_bar);
endmodule
```

(Hint: You will need to create modules for add_full, add_rca_4, and add_rca_16) The library models for the nand, nor, inverter, and xor gate are instantiated with the arguements (output, inputa, inputb, inputc..).

2. Design a two-bit comparator that has 2 two-bit inputs, and three 1-bit outputs. The outputs are A_lt_B, A_gt_B, and A_eq_B. A_lt_B is asserted if {A1,A0} is less than {B1,B0}. A_gt_B is asserted if {A1,A0} is greater than {B1,B0}. A_eq_B is asserted if {A1,A0} equals {B1,B0}.

   Create Boolean equations for each. Design the comparator in verilog using a structural description, and again using a behavioral description.

3. Design a 4-1 Multiplexer in Verilog. There are four inputs, and a two-bit select inputs to specify which input should be sent to the output.

4.

Example 7.58 Mealy machine. The state transition graph in Figure 7.57 depicts the behavior of a finite state machine controller for a moving vehicle. The machine is modeled with four states; transitions between states depend on the state and control inputs (brake and accelerator). The brake overrides the accelerator in the event that both are asserted. Parameters define the bit patterns of the states andmake the description more readable. The (Mealy) output, dyn_ind, indicates the acceleration.

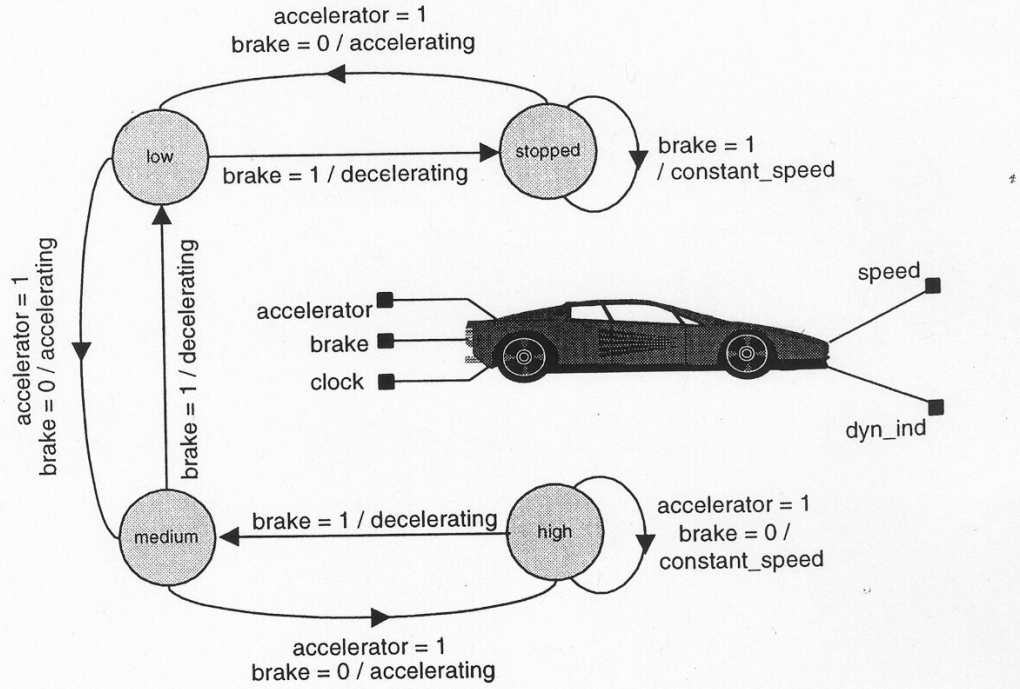


Figure 7.57 State transition graph for a speed-controlled moving vehicle.