Experiment #2

1.1 Abstract

This experiment will focus on sequential logic design. The goal is to construct an up/down counter circuit which will count from 0 – 5 repeatedly, or count 5 – 0 repeatedly depending on the logical value assigned by a push button switch. This design will require the use of logic minimization techniques learned in lecture. Similar to the first experiment, a BCD driver and a seven-segment display will be used.

1.2 Introduction

This experiment essentially consists of three parts. The first part of the lab consists of wiring a toggle push-button switch with an LED. The LED will be used to determine which way the count goes. You may design the LED on to signify an up count, or down count.

The second part will be the design portion of the lab. It is important to formulate logic equations from the problem description, as learned from lecture. These logic equations can be created from truth tables, and reduced using methods learned from lecture such as K-Maps.

The third and final part of the lab is to wire the outputs of the counter to a seven-segment display using the same BCD driver used in the first experiment.

In order to see the count, set the input signal frequency to 1Hz just as in lab #1. Remember the offset should be 1.25V and the amplitude 2.5V for the square wave.

1.3 Hardware

1.3.1 D flip-flops

D flip-flops are devices that hold a state that is dependent on the input value at a clock edge. For this experiment we will be using positive edge D flip-flops. The data sheet for this component should be reviewed to ensure proper timing and functionality.

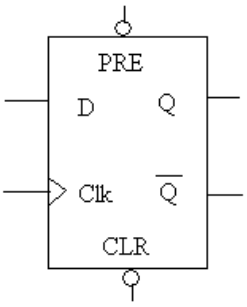


Figure 1: D Flip-Flop Schematic Symbol

The bubbles shown in figure 1 mean these inputs are active low. The PRE input with a bubble means there is an active low preset, meaning, a low input here will force the output high regardless of the clock. Similarly CLR with a bubble, is an active low clear. Whenever CLR is low, the output is forced low regardless of clock. There are two outputs of a D flip-flop. Either can be used to simplify the design if possible. The output Q will be set to the value of D at the positive edge of the clock. The inverse output Q' will become the inverted value of D at the positive edge of the clock.

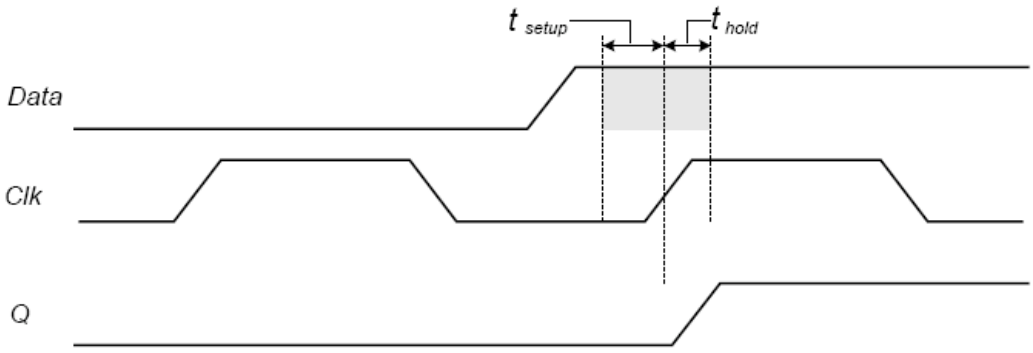


Figure 2: Setup/Hold Time of a Flip-Flop

Setup Time

Setup time is a time necessary for data to be stable at the input of the flip-flop prior to the positive edge of the clock. If D is not stable during this time the flip-flop may store an incorrect value.

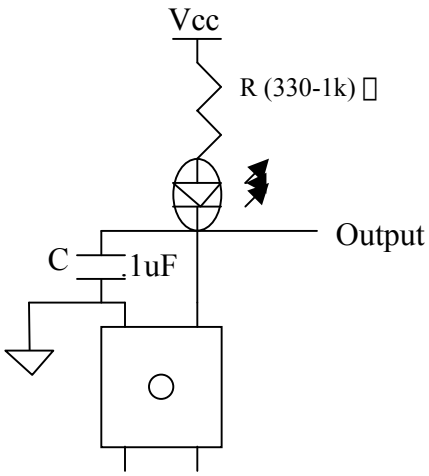
Hold Time

Hold time, similar to setup time is a time necessary for the data to remain valid at the input after the positive clock edge. If the data is not held at the state seen at the clock edge for the proper amount of time, the value stored in the flip-flop may be invalid.

The setup and hold times can also be helpful in determining the maximum frequency of a design. The maximum frequency can be determined by the longest delay between sequential elements. This is not a requirement for this project.

1.3.2 Push Button Switch

The push button switch should be wired as shown in the figure below. Push button switches typically have a lot of “bounce” in the output signal when the button is pressed. Severe bounce in a signal can lead to improper or damaging logical values to be propagated into the circuit. The addition of a capacitor will clean up the signal to make an appropriate logic high or logic low level.



1.4 Truth Table

When you have a sequential design, a truth table can be constructed similar to combinational designs, but will include the current and next state of all sequential elements. For this design your truth table will look like the one below.

Current State			Next State (A=0)			Next State (A=1)		
B	C	D	B^+	C^+	D^+	B^+	C^+	D^+
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

You will need to fill in the next state values. The next state variables need to be mapped to logical equations and minimized.

1.5 Flowchart for Design

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