D Xilinx Software & Tools

D.1 Introduction

This appendix introduces you to the different programs you will use with the FPGA. It does not cover programming etc. but focuses on how to use the different tools. At the end of the manual, you will find a copy of the XSA50 board manual — it contains

D.2 Project Navigator

D.2.1 Introduction

The following sections describe how to perform the most important tasks in Xilinx Project Navigator. After logging on to your computer, there should be an icon named *"Project Navigator"*. Double click to start the software. Alternatively there should be an entry in the *"Start Menu"*.

D.2.2 Creating a new project

This sections walks you through the steps necessary to create a new project.

1. File → New Project
2. In the dialog window, enter project name and location (somewhere on your network drive, i.e. `Z:\`. The type of the top-level module should be HDL.
3. On the next dialog page, choose your target device. The device family is **Spartan2** and the device is a **xc2s50**. Select the package option **tq144** and the speed grade **-6**. Make sure that the generated simulation language is set to **Verilog**.
4. Click through the remaining dialog pages to create your project.

D.2.3 Processes for Current Source

A window in the left lower corner is titled *"Processes for Current Source"*. It contains all the tasks that you can perform on your design. The tasks are structured in a tree hierarchy, the top-level components are:

1. **Design Entry Utilities**: Allows you to create schematic symbols for your design and to start the ModelSim simulator.
2. **User Constraints**: Edit implementation constraints, FPGA pin assignments etc.
3. **Synthesize - XST**: Compile and synthesize your design.
4. **Implement Design**: Implement your design, i.e. determine the allocation of FPGA resources to your design.

5. **Generate Programming File** Create the bit stream to download your design onto the FPGA.

You can expand the items in the hierarchy and see their lower level components. Double-clicking on an entry starts the corresponding task. You can also right-click to get a context-menu with the available options.

D.2.4 Pin Assignments

To do the pin assignment and select what pins your input/output signals should be routed to, select *User Constraints* → *Assign Package Pins*. A new program, Xilinx PACE, will open up.

In the window *Design Browser*, select the option *I/O pins*. The window "Design Object List" then displays a list of all your I/O pins. You can make your pin assignments by entering the desired pin in the *LOC* field. **Note that pins are specified using a P followed by the pin number!** E.g. to specify pin 3, you have to type `P3`; for pin 78 type `P78`.

When you are done, save your changes and exit Xilinx PACE. To generate a programming file to download to the FPGA, run the *Generate Programming File* option in Project Navigator.

D.3 XSTools

The XSTools contain various programs to operate your FPGA board:

- **GXSTEST**: FPGA board test. The *board type* is **XSA50**, and it should be connected to *port* **LPT1**. Note that you might have to take the board out of the breadboard so that it tests correctly.
- **GXSSETCLK**: modify the frequency of the internal clock generator.
- **GXSLOAD**: program FPGA with the bit stream that implements your design
- **GXSPORT**: write values to the parallel port. Helpful for debugging when you map your FPGA board inputs to the pins connected to the parallel port data lines (see appendix **??**).

For further documentation, refer to the XSA50 board user manual attached at the end of this manual.