University of California, Santa Barbara

Department of Electrical and Computer Engineering

Homework #6

(Due by 5:00PM on 03/10/03)

Note: Place your homework in the homework-box for ECE 152A located on the fifth floor of Eng. I

1. Using the Fig. 1, trace the signals through the master-slave J-K flip-flop when the following input sequence is applied. Draw the timing diagram. **(10 points)**

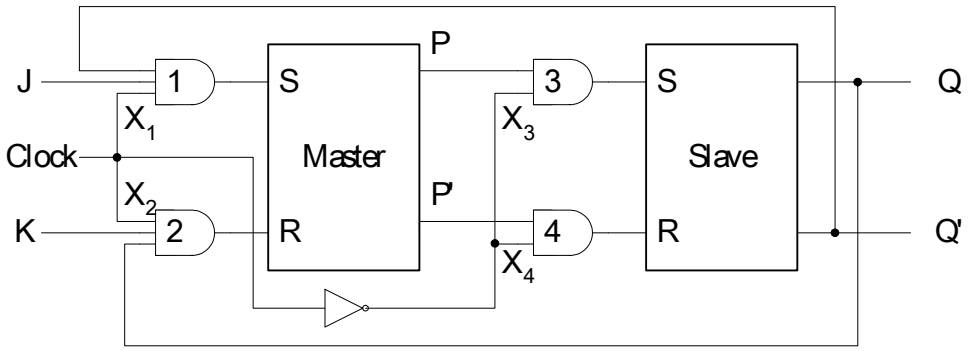

Fig. 1

   (a) Starting with J = K = P = Q = 0. JK change to 10, clock pulse, JK change to 01, clock pulse, JK change to 11, clock pulse.
   (b) Starting with J= K = clock = P = Q = 0. Input sequence: J = 1, K = 1, clock = 1, J = 0, K = 0, clock = 0, K = 1, clock = 1, clock = 0.

2. Draw the logic diagram for the following requests. **(20 points)**
   (a) Convert a clocked T flip-flop to a clocked J-K flip-flop by adding external gates.
   (b) Convert a clocked D flip-flop to a clocked T flip-flop by adding external gates.

3. Design a 3-bit counter which counts in the sequence: **(20 points)**
   001, 100, 101, 111, 110, 010, 011, 001, ……
   (a) Use clocked D flip-flops
   (b) Use clocked T flip-flops
   (c) What will happen if the counter of (a) is started in state 000?

4. If the cyclic shift register of Fig. 3 is changed so that D is connected to the K input of flip-flop A and D' is connected to J, determine the sequence of register states.

(20 points)

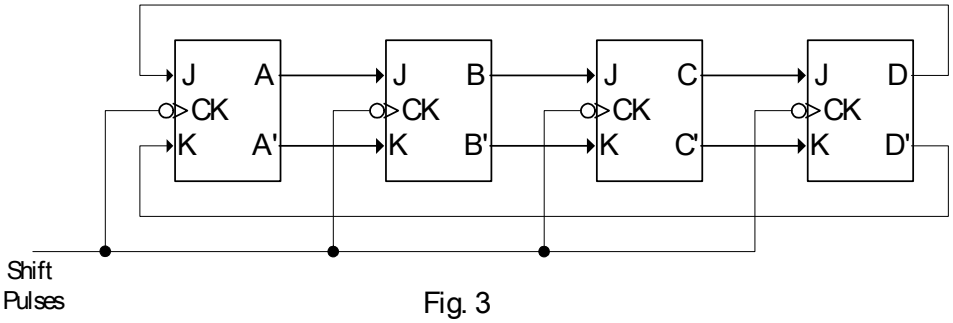

Fig. 3

(a) Draw a complete state graph showing all states.
(b) Derive a complete state table showing all states.
(c) What is the sequence of states starting with ABCD = 0000?

5. A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations: **(30 points)**

$$D_A = \overline{X}Y + XA, \qquad D_B = \overline{X}B + XA, \qquad Z = B$$

(a) Draw the logic diagram of the circuit.
(b) Derive he state table.
(c) Derive the state diagram (Use the Mealy machine).