Start Project Navigator

1. Start new Project Navigator from "*Start Menu*."

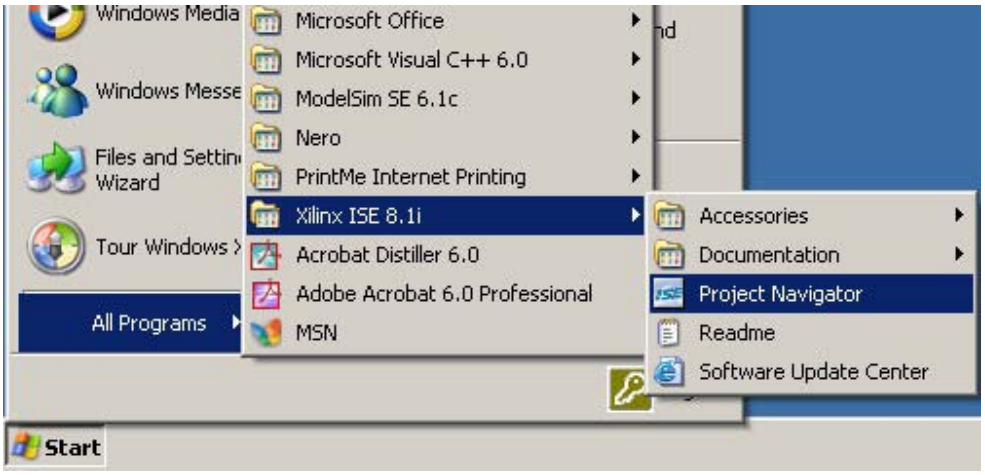

Fig (1)

Create New Project

1. File ->New Project

2. In the dialog page, enter project named and location (somewhere on your network drive, i.e. Z:\. The type of the top-level module should be **HDL**.

3. Select the project options as shown in Fig (2).

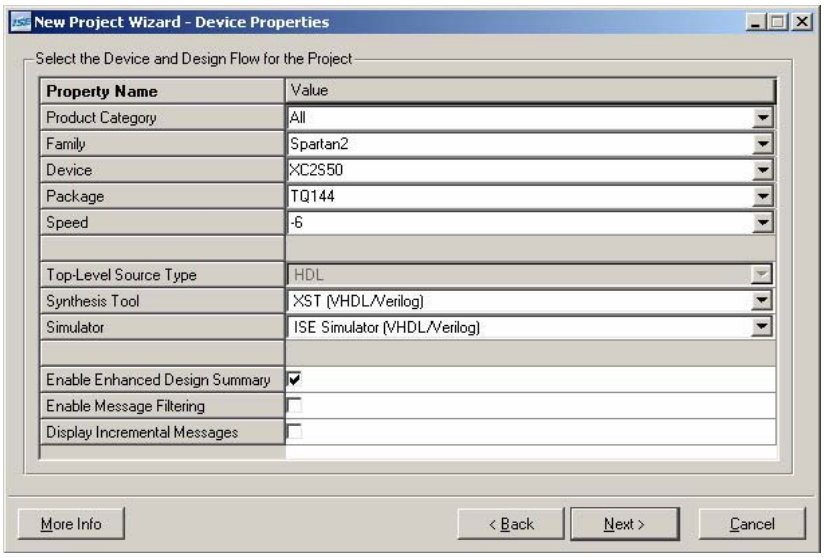

Fig (2)

Depending on which lab you are doing, you will either Create a New Schematic (Labs 1,3) OR Create a New Verilog Module (Labs 2,4,5)

Create New Schematic - (Labs 1 and 3)

1. Create New Source->Schematic.

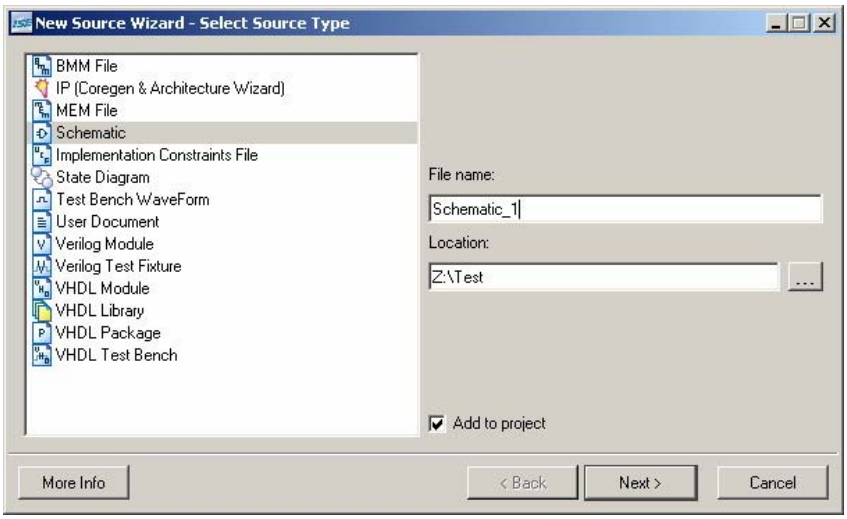

Fig (3)

2. Select the symbols for your schematic from the panel on the left.

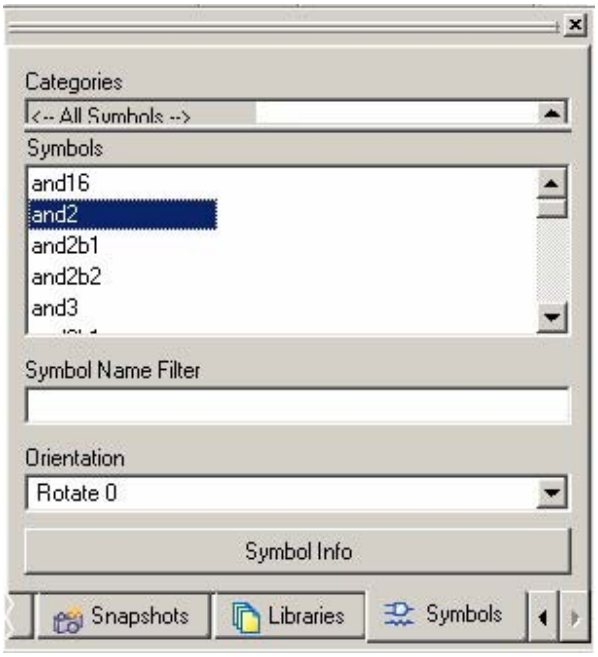

Fig (4)

3. Add -> I/O Maker to add the input/output pins of your schematic.

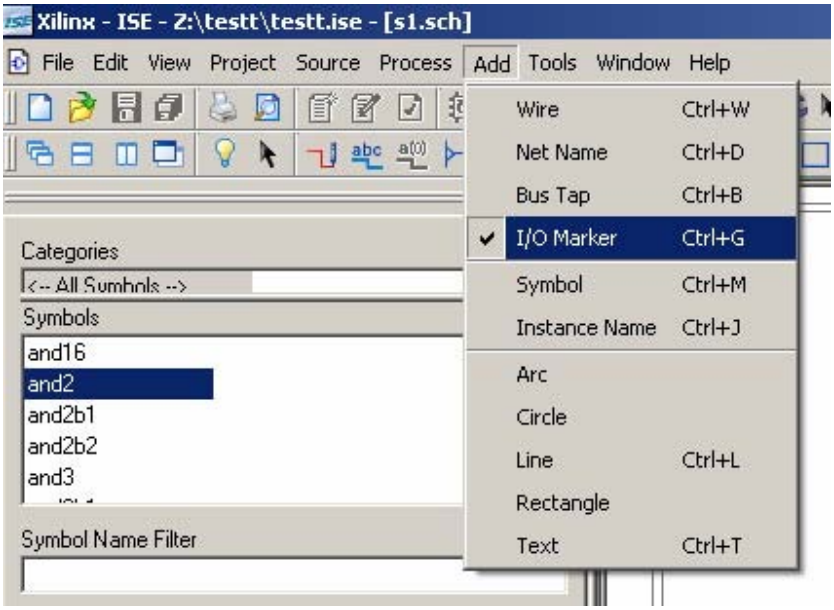

Fig (5)

4. Double clicking on the I/O label can edit the property of each I/O pin.

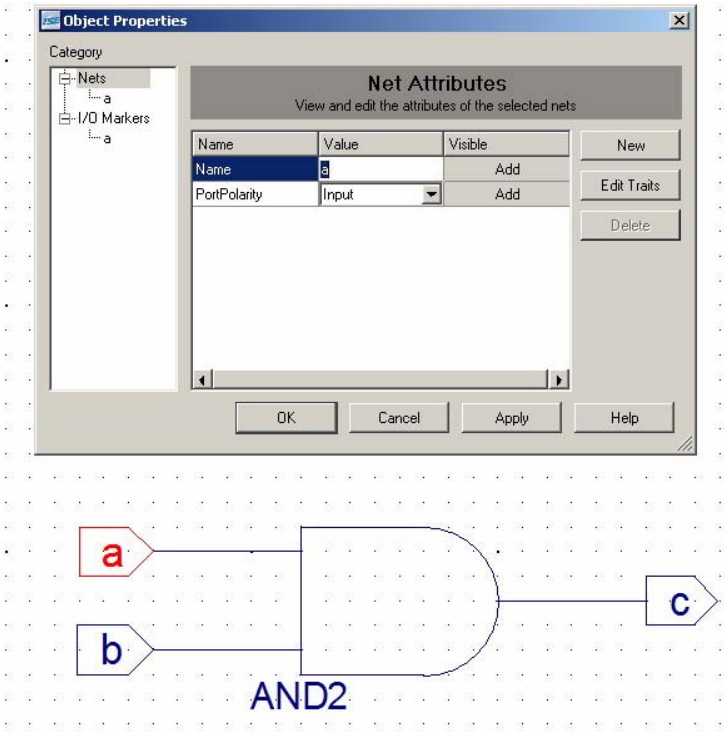

Fig (6)

Create New Verilog Module - (Labs 2, 4, 5)

1. Create New Source->Verilog Module.

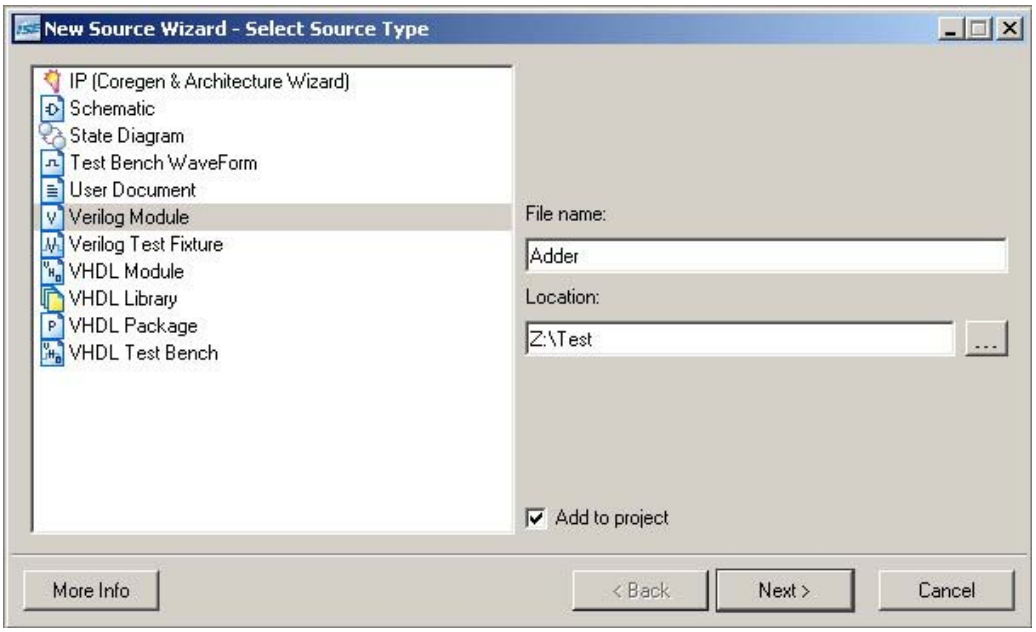

Fig (7)

2. Set Module I/O port.

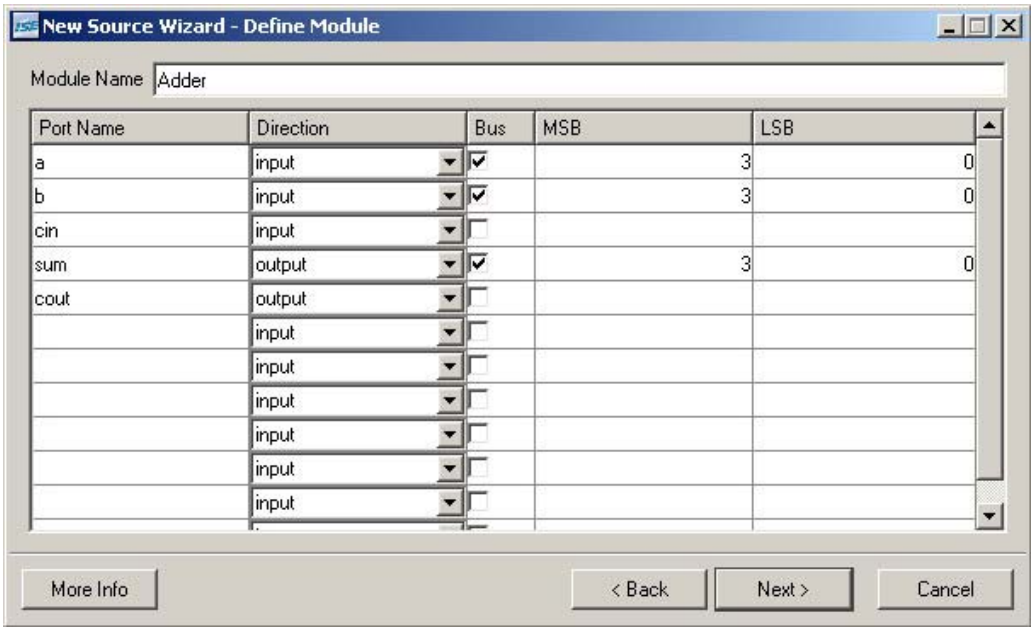

Fig (8)

In order to simulate either your schematic or verilog module you must create a test bench

Create Test Bench Waveform

1. Create New Source->Test Bench Waveform.

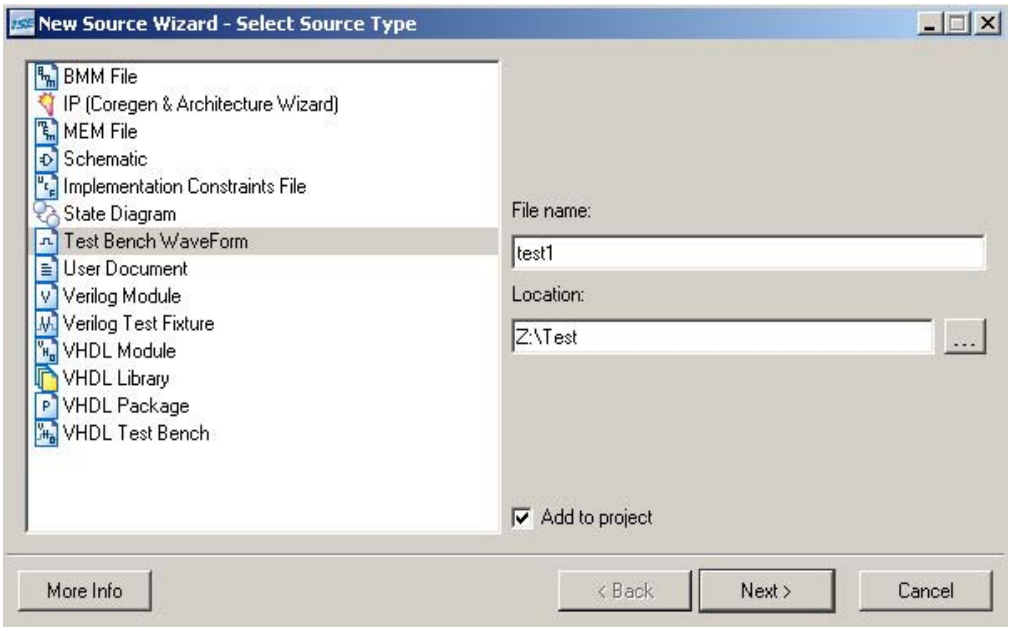

Fig (9)

2. Select a source you want to associate with the test bench.

3. Enter the input test pattern by clicking on the waveform. Double-clicking on the waveform will bring up the Pattern Wizard which is useful for long input patterns.

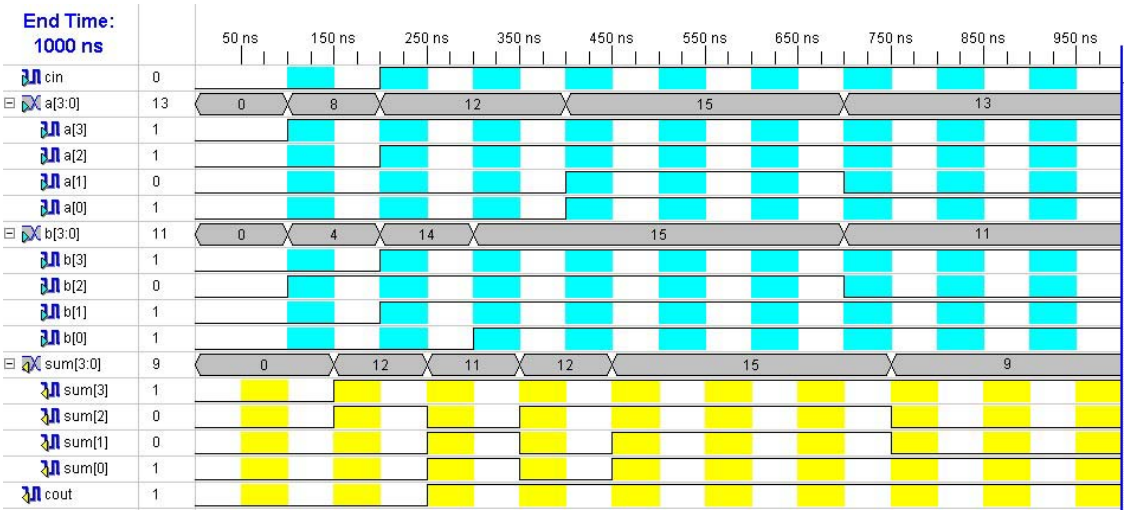

Fig (10)

Run Simulation

1. Change the mode to "*Behavioral Simulation*."

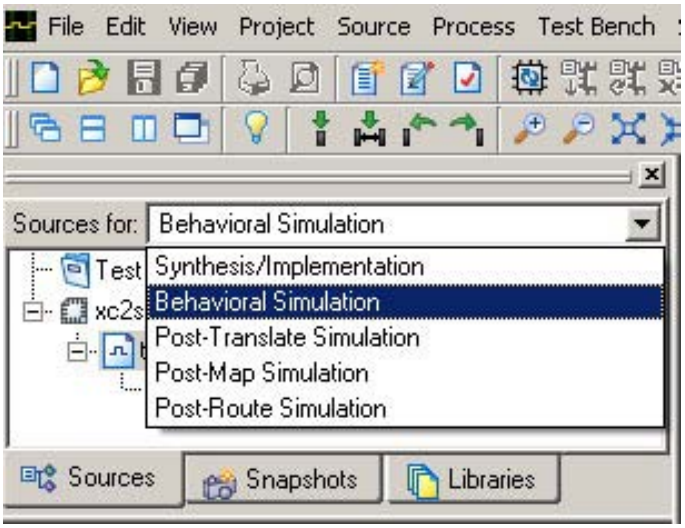

Fig (11)

2. Ensure that your test bench is selected, then double click on "Generate Expected Simulation Results" to run the simulation, shown as Fig (12)

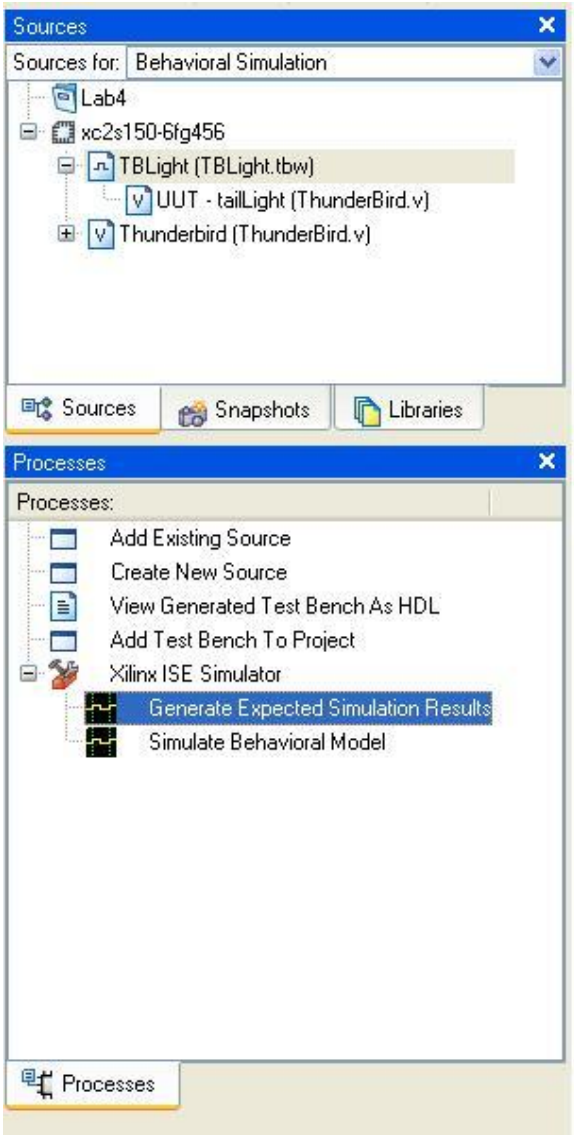

Fig (12)