UCSB/ECE Digilab FPGA

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DigiLab-FPGA Board Software

User Interface to the DigiLab-FPGA Board

FPGAtool

Version 1.02/GL

Section

1

Download & Installation

http://vader.ece.ucsb.edu/digilab-fpga

Where to get the software

The FPGAtool Windows application can be obtained by downloading it from the main DigiLab-FPGA board website: http://vader.ece.ucsb.edu/digilab-fpga . The latest version is available for downloading from the home page as well as on the Downloads page. Simply access the appropriate link and save the FPGAtool.exe program on your computer.

The FPGAtool.exe program is a Windows-XP application that provides access to the DIgilab-FPGA board via a USB connection.

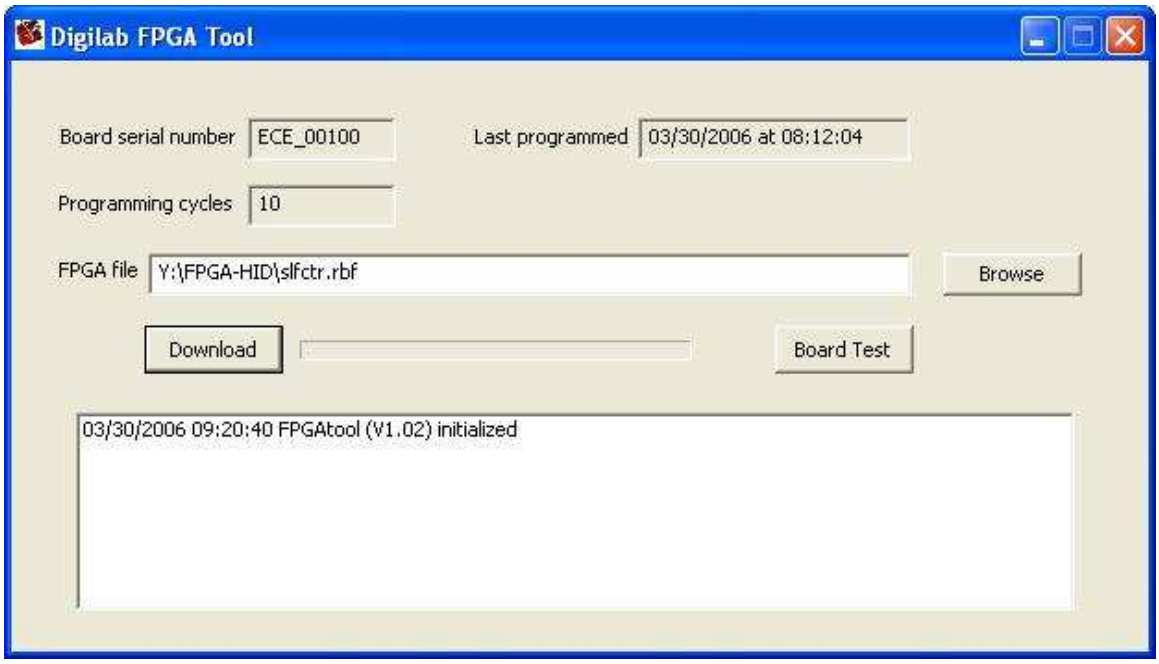
How to Install

No special installation procedure is required for FPGAtool. The program is a single graphical user interface that is packaged as a regular Windows ".exe" file. You can save it anywhere that you find convenient. When stored on the desktop, FPGAtool will show up with its toolbox icon.

FPGAtool does not require any special Windows drivers or non-standard software. It uses the Windows human-interface device (HID) model to connect to the hardware via USB. HID devices have restrictions on the amount of data sent back and forth in each report and on the frequency with which data can be exchanged. What we "pay" in exchange for using the Windows HID driver is that it takes a little longer for us to download FPGA configuration information from the computer to the FPGA board.

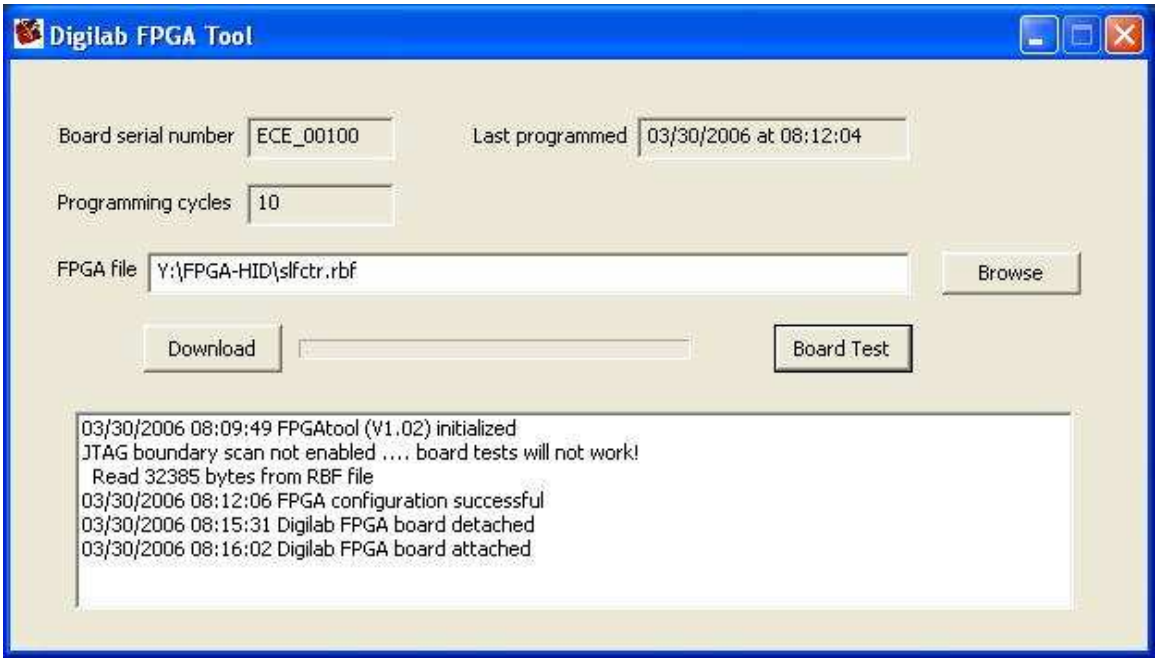
Running FPGAtool

The FPGAtool application is launched just like most other Windows applications. Simply select its icon and open (normally this action is configured as simply a double-click). When opened, the program should start running and the main user dialog should appear.



The main user dialog is a window with several fields showing information about the Digilab-FPGA board that is plugged into one of the computer's USB ports. The image above resulted from launching the FPGAtool program after a Digilab-FPGA board had previously been connected and powered-up. The board serial number (shown above as ECE_00100) and information about the contents of its on-board flash memory appear in the fields.

It is also possible to launch the FPGAtool program without any Digilab-FPGA board attached. When this happens, the information fields in the main dialog will say "<unknown>" to indicate that the program is unable to locate any FPGA boards. When a board is subsequently plugged in and powered up, the dialog should be updated to show the information about the attached board. Below is an screen shot showing the result after initial startup with a board connected, then a user disconnect (USB unplugged), and finally a re-connect. Note that the large edit window at the bottom of the dialog contains a log of all events since the program was launched.



In the case shown above, FPGAtool was launched with an FPGA board that had not been previously programmed with an RBF file. Thus, when it was initialized the error "JTAG boundary scan not enabled" was reported. Subsequently, the user downloaded an RBF file (more about that soon) and the log reflects the successful FPGA configuration. After that, the user unplugged the USB cable and FPGAtool logged the detach event. Thirty seconds later, when the board was re-attached, FPGAtool entered another event in the log.

Pressing the reset button on the FPGA board is equivalent to detaching and then reattaching the USB cable. The reset button also causes the FPGA to get reinitialized.

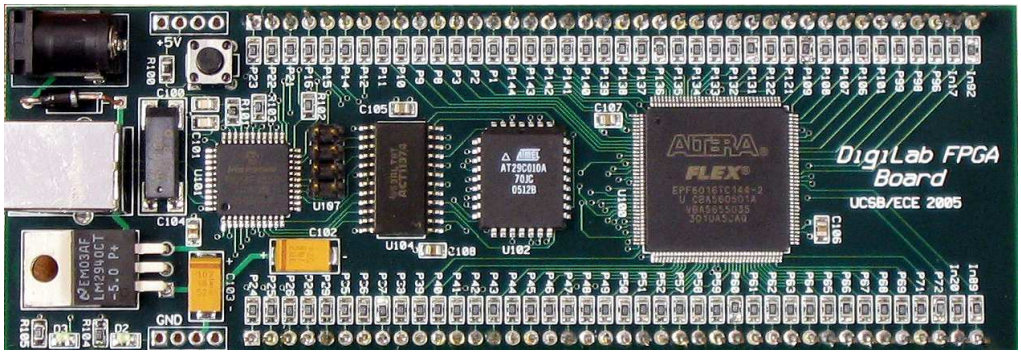
Section

2

Project Hookup and Checkout

Choosing Pins of the FPGA Board

The primary purpose of the DigiLab-FPGA board is to support the prototyping of digital systems projects and experiments. As such, it is important to learn how to properly attach signals to the board. Below is a photo of the FPGA board. Note the rows of pin headers along the top and bottom edges.



In all there are 80 user-accessible signal pins in these headers. The headers are each labeled with the attached FPGA pin number so that when a pin is chosen, matching allocation of that pin can be made in the Quartus-II project (documentation of Quartus-II is available on the DigiLab-FPGA website as well as within the Help system of Quartus-II itself). A map of available FPGA pins is given on the DigiLab-FPGA website, under Documentation → FPGA Board Pinout. Note that the first batch of boards (ECE_100 through ECE_199) have ten pins that are designated as “high-drive” pins. These pins are the leftmost ten pins in the top header strip, beginning near the reset bottom (P23-P9). You should use these for outputs with higher fanout loads or to drive LEDs, etc. Later versions of the DigiLab-FPGA board will have all pins setup for :high-drive”.

All pins designated “**P<number>**” are general-purpose pins. As such, they can be provisioned for use as inputs, outputs, or bidirectional pins. There are four special input-only pins. These are located on the extreme right end of the pin headers and they are labeled “**In<number>**”, specifically **In17**, **In20**, **In89**, and **In92**. These special pins can only be used for inputs to the FPGA. They are intended to carry signals that need to be distributed to many parts of the FPGA, e.g. clocks, or resets, or other global signals. These pins are especially provisioned within the FPGA for low-skew, broadcast–style signals.

Making Attachments to the FPGA Board

The DigiLab-FPGA board is intended to be inserted into a laboratory prototyping board. Note that a considerable amount of force may be required to do the insertion. Please be careful when doing this; even though the boards have been made thicker than normal, it is possible to break the printed circuit boards if too much downward force is applied. It is critical to check the alignment of all of the board pins before attempting to force them down into the prototyping board holes. Once inserted, it is a good idea to leave the DigiLab-FPGA boards installed in their prototyping boards. Removing them and reinstalling them is asking for trouble.

With the boards installed in a prototyping board, the power connections can be made. Note that there are four power pins (+5V DC) and four ground pins provided on the bottom side of the DIgiLab-FPGA board. These pins are located on the left end of the header strips with the +5V pins on the top edge and the GND pins along the bottom edge. Locate these pins on your board. Always hook the FPGA board's GND signals to the ground leads of your other components.

The FPGA board's voltage regulator provides +5V DC at up to 1 amp. If your project needs 1 amp or less you should use the FPGA board's +5V output to power your circuits. This setup should result in the best possible signal integrity. Note that your board's regulator may become quite hot when it is delivering current near its full 1A capacity. Be careful not to burn yourself. If your external circuits use more than 1 amp you should not use the DigiLab-FPGA board's +5V DC output. In such a case you can get +5V from one of the power supplies in the laboratory. **Do not attempt to connect the FPGA board's +5V DC output in parallel with another external lab power supply**. If you need more than the 1A that is provided then the power connections to the FPGA board should be to the GND terminal only, with no connections made to the +5V DC. We do not want to create a situation where two power supplies "fight" with each other. Of course, the FPGA board must always get its power from an external 9V module through the black barrel connector in the extreme upper left corner of the board. These power modules are installed at each station in the Digital Systems Lab.

Using JTAG for Wiring Checkout

The Flex6000 FPGA contained on the DigiLab-FPGA board implements JTAG boundary scan (subsequently called "JTAG") This capability allows us to read the state of the pins of the FPGA and report them to the user. It is also possible to temporarily cause the FPGA to drive any of its pins to a user-chosen value. These capabilities are useful in checking out the connections between the board and other lab components.

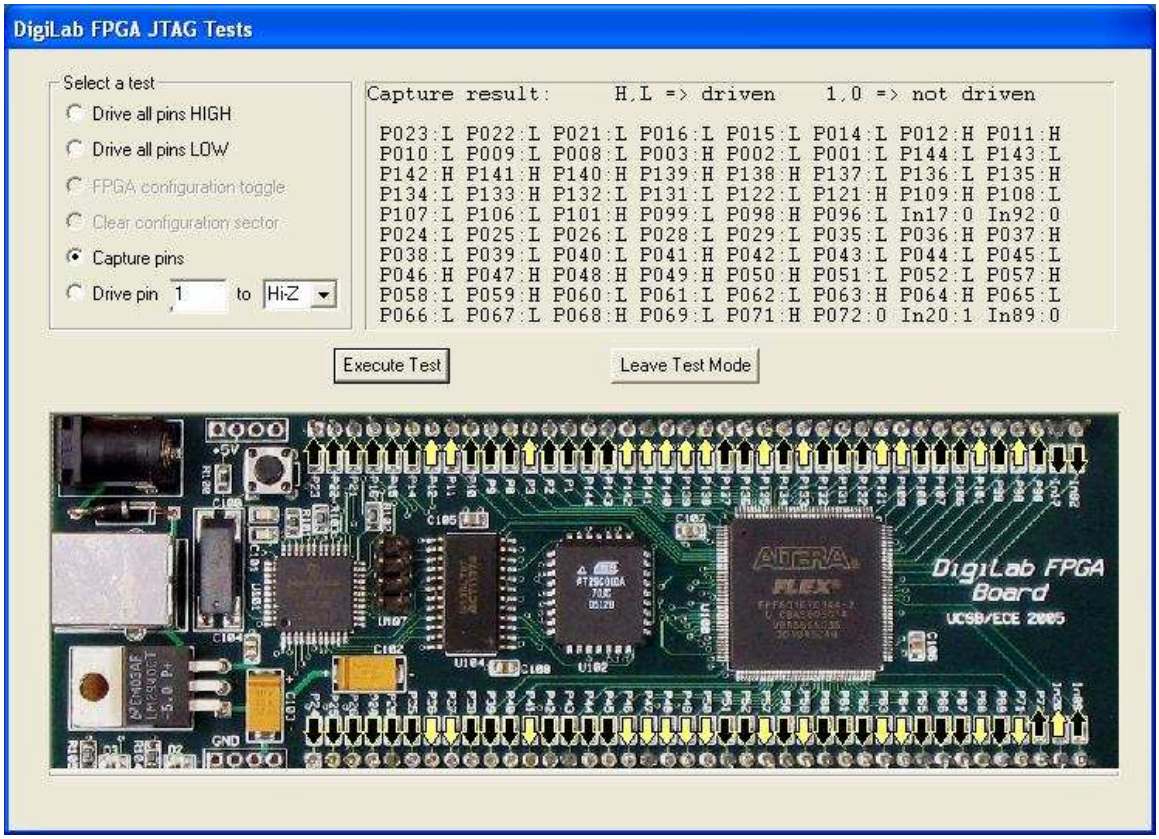
In order to use the JTAG capabilities of the FPGA board, the FPGA's configuration file must specifically enable JTAG/BSC mode. The website discusses the Quartus-II settings required in order to accomplish this. It is good idea always to enable the JTAG/BSC feature. It doesn't cost anything in performance or pin utilization. The pins used for JTAG are not made available to users (in this design) for non-JTAG purposes. If JTAG is not enabled in the configuration file stored on-board then the JTAG features cannot be used.

To enter the JTAG dialog, click on FPGAtool's "Board Test" button. The JTAG dialog shown below should appear.

Note that the JTAG dialog contains a board image (with small colored arrows overlaying each user pin), a message area containing the message "<no tests performed yet>", and a set of buttons within a box labeled "Select a test". Once JTAG transactions occur the colored arrows will indicate the state of each FPGA pin. The direction of each arrowhead indicates whether the corresponding FPGA pin is acting as an input or an output. The color of each will indicate whether the pin is currently high (light yellow) or low (black).

The initial display (shown above) has the arrows pointing from the outside in (i.e. toward the FPGA). This direction indicates input. The arrow color (light yellow) indicates logic-1. Though this initial screen does not represent the true state of the FPGA, the meaning of such a display would be that, when captured, all of the FPGA pins were acting as inputs and they were captured with high logic levels.

Once the user requests a "Capture pins" test, the screen would be updated to reflect the real data, as shown below.



In the image shown above, the user has selected “Capture pins” and then clicked “Execute Test”. Once the JTAG boundary scan capture occurred, the resulting FPGA pin states were displayed in the message window using “H” or “L” for output pins and “1” or “0” for input pins. Additionally, the arrow heads have been colored and oriented so as to indicate the same information.

You can also select single pins on the board image. When you click near a pin header or its corresponding arrow, the system will do another capture and update the screen. The message window will display the state of the single pin under the mouse.

In addition to pin capture, JTAG can support temporary changes to pin state. This is done by selecting one of the tests “**Drive all pins HIGH**”, “**Drive all pins LOW**”, or “**Drive pin <X> to “<value>**”. These tests are self explanatory. “**Drive all pins HIGH**” makes all of the FPGA’s pins act as output pins, driving logic-1’s. Of course, the input-only pins 17, 20, 89, and 92 cannot participate in this test as they are permanently configured as inputs. The “**Drive all pins LOW**” test makes all of the FPGA pins act as outputs, driving a low logic level.

For the “**Drive pin <X> to “<value>**” test, the FPGAtool first uses JTAG capture mode to capture the state of the FPGA. Then, it changes the single selected pin so that it will have the prescribed value and sends it back to the FPGA. Note that though the single selected pin will indeed get the value you have specified, the rest of the FPGA will freeze with the most recently captured pin states. This is not, in general, the same as simply changing the one pin to have the behavior specified. JTAG cannot do that. Instead it must use EXTEST (external test) mode to cause preloaded values to override the real FPGA pin values. The preloaded values were those captured immediately before changing the specified pin.

Section

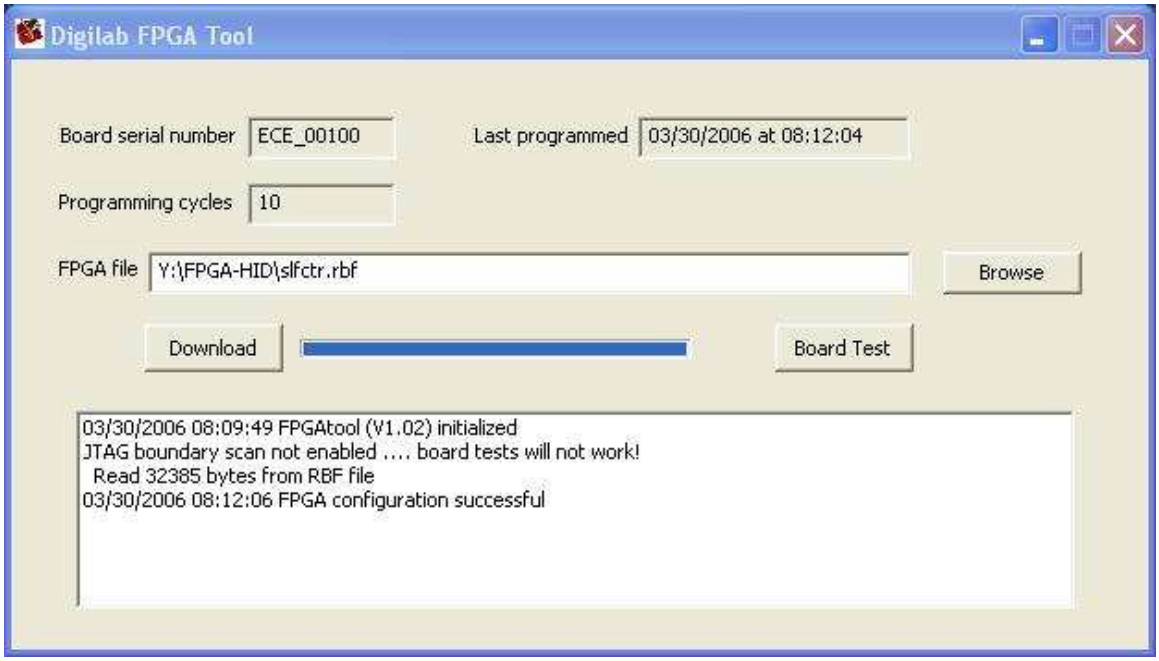
3

Configuration of the FPGA

Downloading the RBF file to the FPGA Board

The Digilab-FPGA board contains a flash memory to hold the user's FPGA configuration file. Flash memories are non-volatile. Once programmed, they are capable of storing data for at least 20 years. The path to the flash memory involves USB and FPGAtool. Once the user has plugged the DigiLab-FPGA board in as a USB device and fired up FPGAtool, the main dialog screen should appear (refer to the screen shot on page 2).

There are two buttons on this screen that pertain to the FPGA configuration file. The first is "Browse". When clicked, the Browse button brings up a standard Windows file browser window which allows you to navigate the file systems of the local computer. The file browser should be configured to help locate files with the "**.RBF**" extension. These files are Altera Flex6000 FPGA configuration files in raw binary format (hence R-B-F). Refer to the DigiLab-FPGA website for directions for using Quartus-II to synthesize your design and produce an RBF file. This section describes how to download that RBF file into the on-board flash memory and configure the FPGA.



Actually, downloading is very easy to do. Once you have clicked "Browse" and located your RBF file, hit the file browser's "Open" button to indicate your file selection. That should leave the file browser window and take you back to the main FPGAtool dialog window. Next, you hit the "Download" button and watch the progress of the downloading

via the blue progress bar next to the Download button. As the download proceeds, the LED in the extreme lower left corner of the Digilab-FPGA board should blink. When it stops blinking --- if all has gone well --- the progress bar should be fully extended and a message in the message window should indicate a successful FPGA configuration. If anything goes wrong, the on-board LED should remain on. The screenshot above shows the dialog window after a successful download operation.

The statistics fields that are displayed on FPGAtool's main dialog window help to keep track of the RBF file that has been most recently downloaded. The board also keeps track of the number of downloads. Flash memories have a finite lifetime on the order of 20,000 write cycles. The purpose of keeping track of the number of flash downloads is to see how close each board is getting to its service lifetime.

Resetting the FPGA Board

There is a reset button located near the upper left corner of the Digilab-FPGA board. This button can be pressed at any time. While pressed, the on-board microcontroller is held in reset. Since the on-board microcontroller is in charge of everything that happens on the DigiLab-FPGA board, resetting it makes the board completely start fresh, just as if the power had been disconnected and then reconnected.

When the microcontroller comes out of reset, it tries to establish a USB connection with the host computer. If FPGAtool is running, you should see a **detach** message in the log, followed by an **attach** message. Every time FPGAtool attaches to its FPGA board, it reads the statistics from the flash memory and displays them in their fields on the main dialog window. Independent of whether FPGAtool is running or not, the microcontroller comes out of reset and attempts to configure the FPGA using the latest RBF file that has been stored in its flash memory. If for any reason it is unsuccessful in performing this configuration, the LED in the lower left corner of the FPGA board (labeled D3) will come on. You should think of this LED as an error LED. Whenever it is illuminated and stays statically illuminated, it means that something incorrect has happened. It is <u>not</u> an error for this LED to blink during downloading. We do that so that you can see progress during downloading as well as know that the LED is capable of turning on. The only time that LED D3 signifies an error condition is when it is statically on. The second LED (D2) is a power-ON indicator. D2 should be on at all times that the DigilabFPGA board is attached to its power cube.

Most of the time you will be operating the FPGA board with FPGAtool attached. When this is so, any errors that occur should be reported in FPGAtool's message window or via various JTAG-related failure messages for cases where errors happen while in the "Board Test" mode. If FPGAtool isn't running, however, you must pay attention to the error LED. As long as it remains off, everything is fine. When it comes on and stays on it means some sort of error condition has occurred.

Generally, an error condition should cause you to try resetting the board by pushing the reset button. You really cannot hurt anything by resetting the board … and it gets everything off to a clean start. Of course, you must think carefully about what this "clean start" is going to mean as far as your attached experiment is concerned! Remember that the FPGA is going to get reconfigured. During that reconfiguration, its pins will be tri-stated. The signals seen by attached logic may be unpredictable.

If an error persists after a couple of resets, you should probably connect your board to the computer via USB and run FPGAtool to see what additional information can be learned

about the problem. Ultimately you may need to make changes in your FPGA design and reload the RBF file into the flash. In the rarest cases you may have to take your board back to the ECE shop to have its firmware reloaded. Hopefully this is never necessary but, if all other attempts fail, that's the next step to be tried. It is not possible to reload the microcontroller firmware in the Digital Systems Lab since a special test fixture is required. If your board is "dead" you will have to take it to the ECE Shop for diagnosis and possibly for firmware reloading. The shop has a test fixture that facilitates these activities.