2025-2026 UCSB Senior Capstone Project

Radar Receiver ASIC: Designing an ASIC for Radar Signal Processing

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Introduction: Scientists and engineers at HRL Laboratories, LLC (previously known as Hughes Research Laboratories, established in 1948) have been on the leading edge of technology, conducting pioneering research, providing real-world technology solutions, and advancing the state of the art. Our research collaborations with our LLC Member companies (General Motors and Boeing), government, commercial and academic institutions are realizing groundbreaking advances in ultra-high-performance circuitry, robust computing and communications, automated data extraction, and innovative architected materials. Our technologies operate in space, on aircraft, in automobiles, and in a variety of consumer products.

Background: Radar systems can be found within aviation, marine navigation, automotive safety and more. They're used to detect, locate, and track objects by receiving radio waves and analyzing the reflections through signal processing. A standard radar system signal processing flow starts from the antenna receiver, converts the signals with an ADC, then goes through windowing, an FFT, and detection algorithms to produce a detection. The signal processing chain can be computationally expensive, especially on large data collections, which is a critical bottleneck on systems in motion like aircraft or automobiles. Current FPGA-based signal processing chains could be sped up with the design of an ASIC targeting specific radar computation. This could include detection algorithms, matrix computations, or accelerated FFT processing. In addition to designing the ASIC, effort is needed to integrate the ASIC with an FPGA-based signal processing chain to generate real detections.

Project Description: The scope for this project focuses on the tape-out and testing of an ASIC designed as part of the chain for processing radar data including simulating the ASIC behavior on an FPGA to prove its functionality. The ASIC will be integrated with an FPGA to create a full, functioning radar data processing chain. HRL will work collaboratively with the interested project group to define the ASIC design that is most appropriate in scope for a Capstone development effort. HRL and interested students will develop:

- Project scope for an ASIC tape-out
- Key metrics and requirements for development efforts
- HRL mentorship and collaboration structure

If some part of this overall problem fits a team's interests and skillsets, please brainstorm a few potential focus areas to work with HRL to curate a project in this area. A well-defined project in this area should seek to:

- Capture system design challenges from ASIC design for a single radar data processing focus area. For this effort these include but are not limited to:
    - Matrix operations such as inversion
    - Detection algorithms
    - FFT
    - Windowing
- Have a project scope that addresses a key technical challenge and is easy to build upon in future works
- Have a demonstratable output product or simulation of output product

Reference:

- https://ieeexplore.ieee.org/document/7015344
- https://www.tsmc.com/english/dedicatedFoundry/technology/logic/l_65nm