ECE 225
High Speed Integrated Circuit Design
Lecture 1

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Course Description….

- Advanced digital VLSI design: CMOS scaling, nanoscale issues including variability, thermal management, interconnects, reliability
- Non-clocked, clocked and self-timed logic gates clocked storage elements
- High-speed components, PLLs and DLLs
- Clock and power distribution
- Memory systems
- Signaling and I/O design
- Low-power design

Textbook and References

- Textbook
  - Digital Integrated Circuits: A Design Perspective (Second Edition)
    - Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic
    - Prentice Hall Publishing Company, ISBN 0-13-090996-3
- Reference Materials and Recommended Reading
  - To be posted on the class web site:

    http://www.ece.ucsb.edu/courses/ECE225/225-W06Banerjee/default.html

Prerequisites

- Semiconductor Physics
- Device Physics
- Basic Circuit Analysis (both analytical and simulation based)
- Other
  - Logic design
    - Combinational and clocked logic, Gates, latches, flip-flops, etc.
  - Fundamentals of electromagnetic theory (physics)
    - Resistance, capacitance, inductance, power/energy

Preparation for the course

- Computing environment and tools
  - Setup computer account, and the compute environment
  - Familiarize with the schematic and layout editors
  - Familiarize with the circuit simulator
- Theory
  - Review device physics
  - Review logic design, computer architecture, and electromagnetics
- Projects
  - You should start formalizing your project ASAP
  - **Must work on your own**

Understanding the MOSFET

- *Band Diagrams*
- *I-V curves*
- *Static/dynamic behavior*
- *Parameters (process, temperature, voltage) that impact device behavior*
- *Impact on circuit parameters (delay, power, NM)*

Implementation & Sizing of Complex Gates

- *Described as: Function, K-map, Truth Table, or propositions*
- *Sizing of gates to get equivalent inverter size (based on worst case delay) ---with and without considering internal capacitances*

Circuit Level Implementation Choices for Complex gates

- *Implement a function F with*
  - *Static CMOS*
  - *Pass Transistors*
  - *Pseudo-NMOS*
  - *Dynamic Logic (including Domino)*
- *Pros and Cons of each of the methods (in terms of delay, power, area, noise margins etc.)*

Elmore Delay

Know how to apply Elmore delay to find the delay between any two points in a:

- *Given RC tree*
- *Given topology of gates (find their equivalent RC…)*

Optimization of a Design

- *Optimizing a design in terms of delay and power dissipation*
- *Choosing optimal number and sizes to minimize the delay for*
  - *Inverter chain*
  - *Gates (Logical Effort)*
- *Trade-off between delay and power dissipation*

Sequential Circuits

- *Design of foreground memory elements*
  - *Latches*
  - *Filp Flops*
- *Timing parameters (understand in terms of circuit design and topology)*
  - *setup time*
  - *hold time*
  - *clock skew*

Semiconductor Memories

- *Basic Types*
- *SRAM (circuit level implementation…., read and write operations, sizing issues)*
- *DRAM (circuit level implementation, read and write operations, processing issues)*

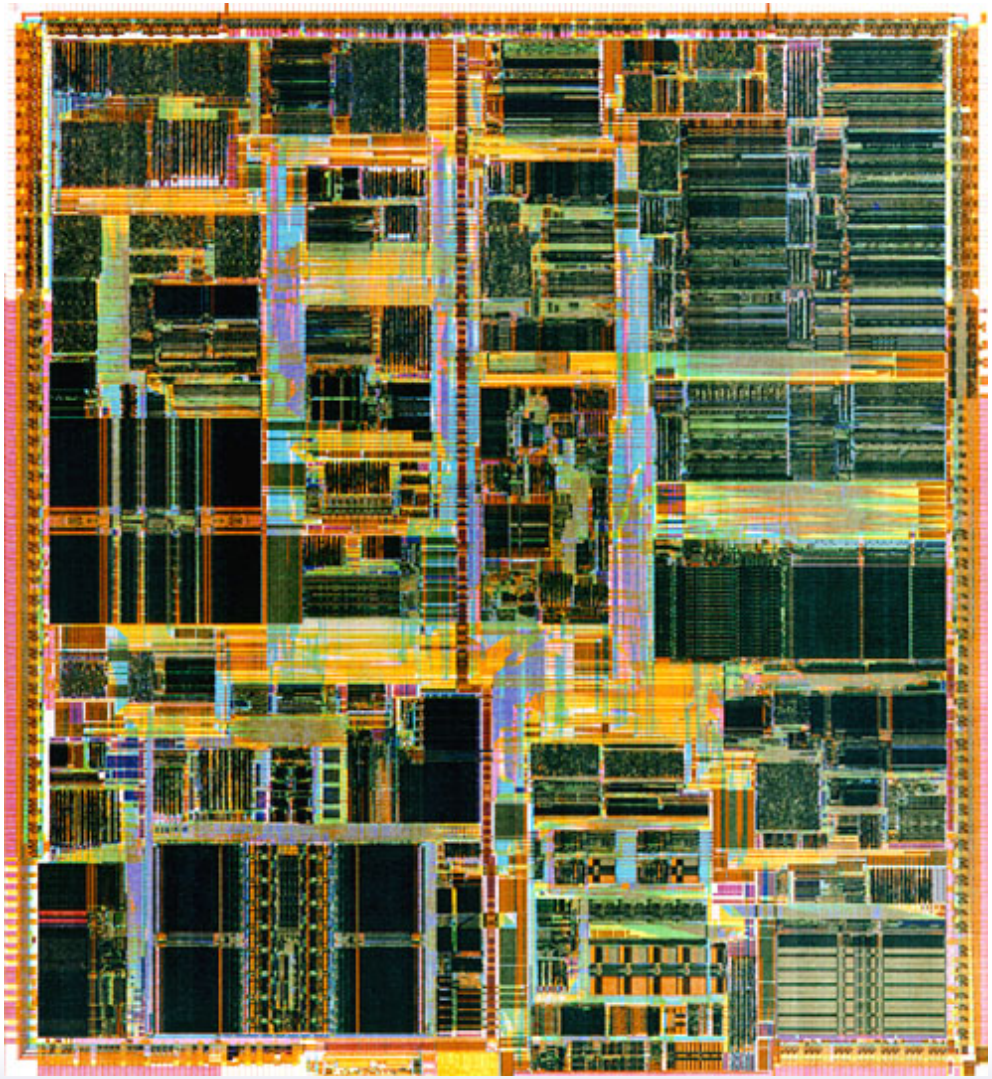
Introduction

- Why is designing digital ICs different today than it was before?
- Will it change in future?

Integrated Circuit History

- Invention of BJT (1948)
- First silicon transistor (1954)
- MOS transistor (1960)
- MOS integrated circuit (1962)
- DRAM cell (1968)
- Intel formed (1968), AMD formed (1969)
- Microprocessor invented (1971)
- 32-bit microprocessors (1980)

Intel Pentium (IV) microprocessor

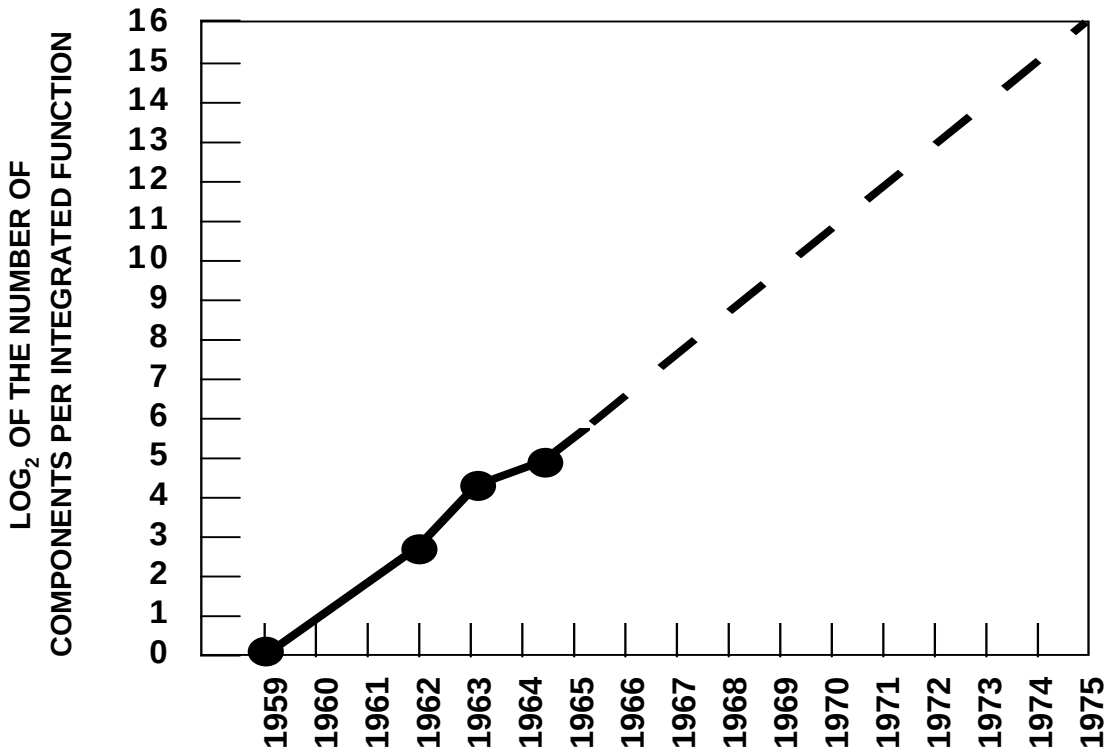


2003:
CMOS based
> 50 million transistors
> 3GHz operation

Moore's Law

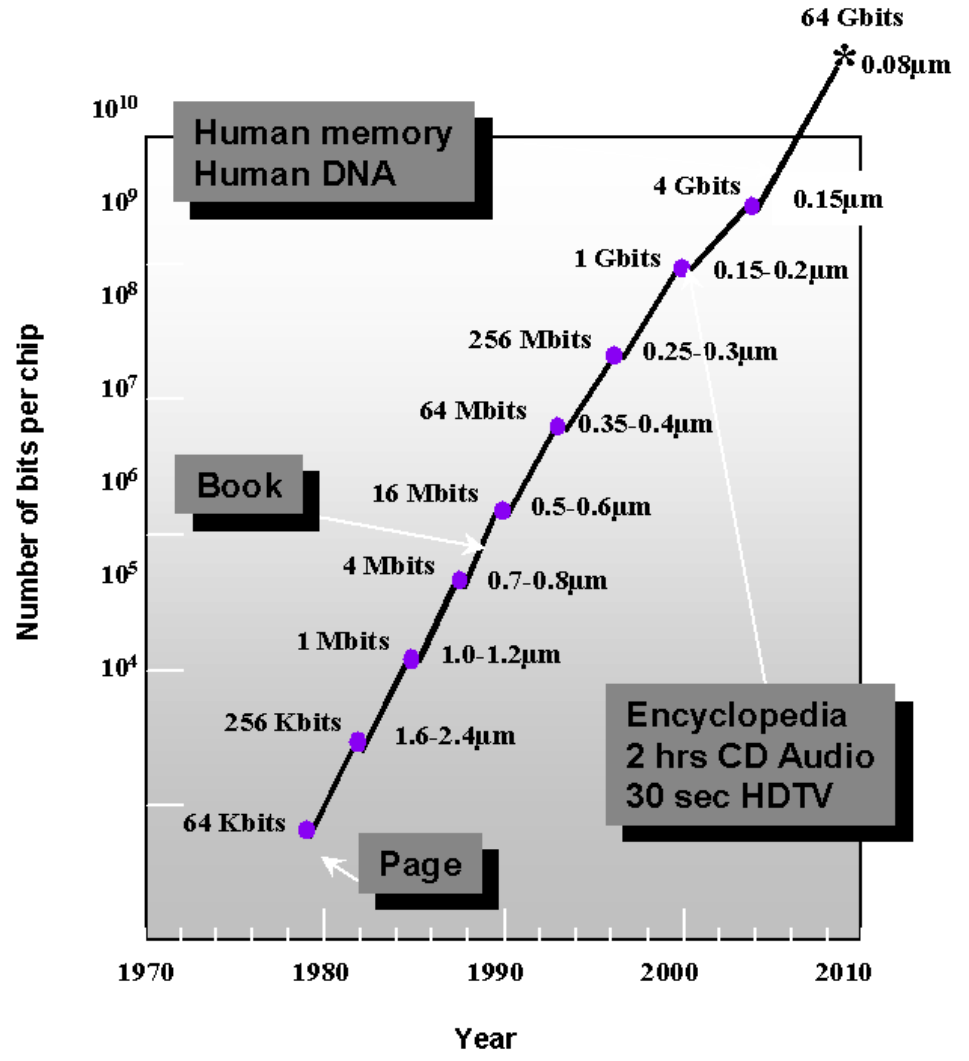
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

Moore's Law



Electronics, April 19, 1965.

Evolution in Complexity

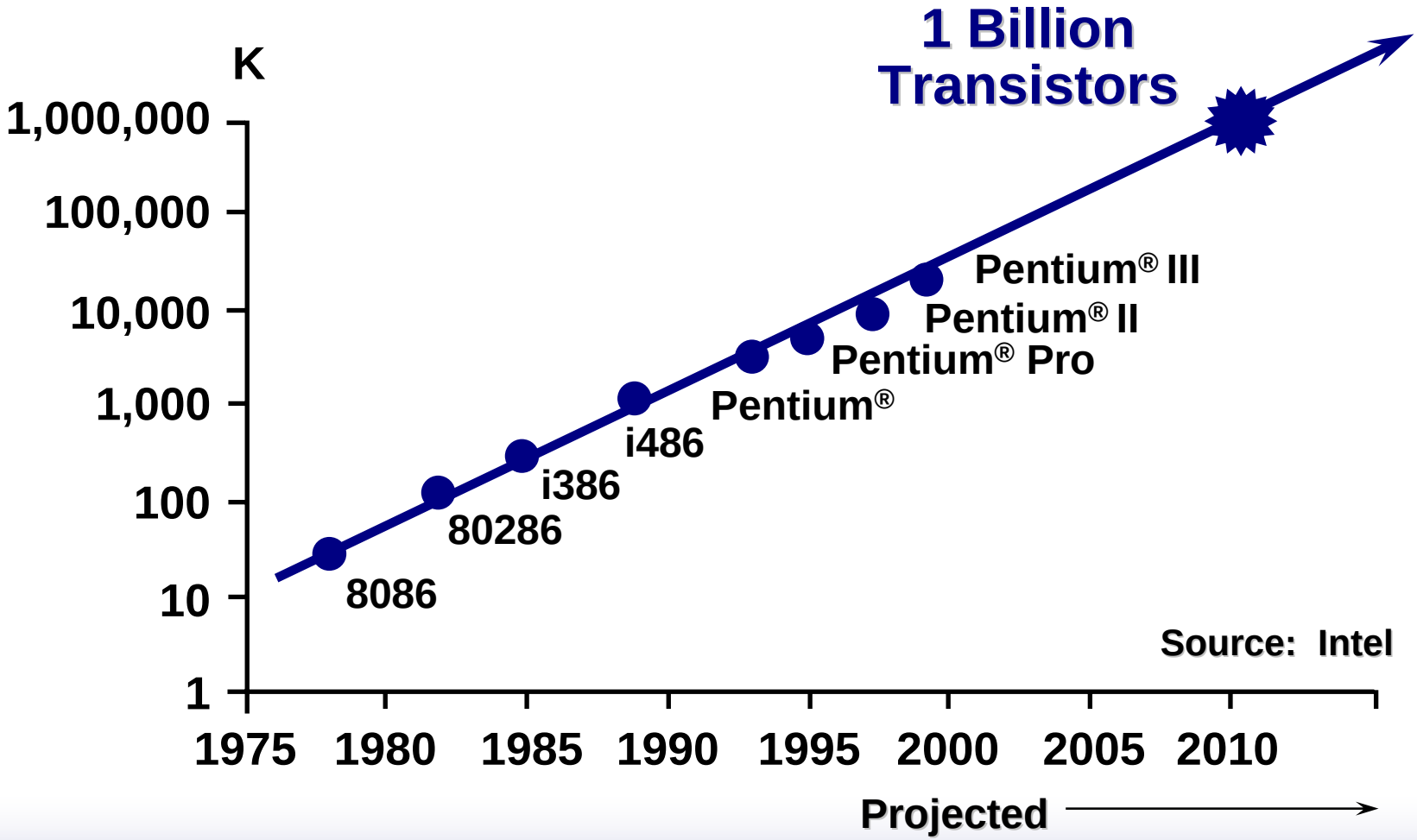


IC Classification

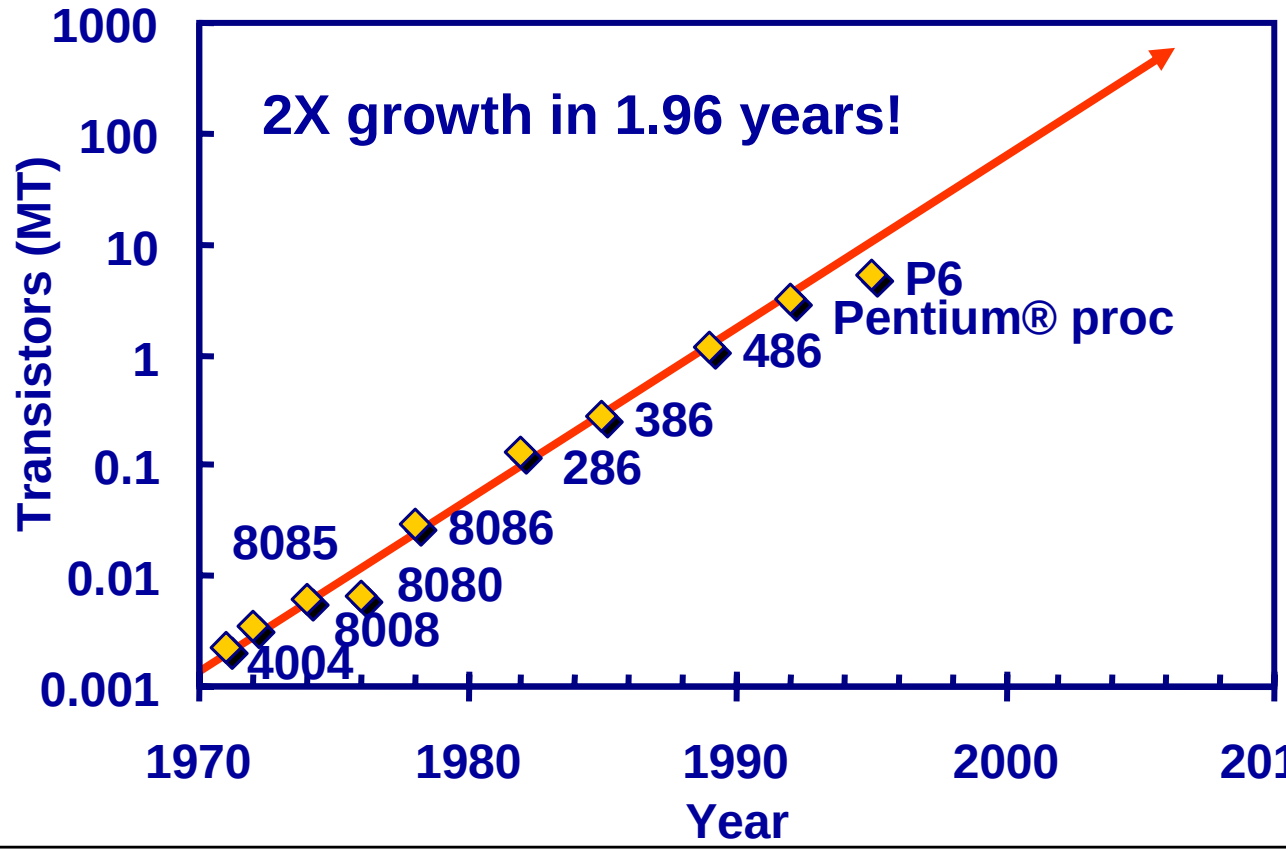
- Circuit size (transistor count)
- Circuit technology (BJT, BiCMOS, NMOS, CMOS)
- Design style
  - standard cell
  - gate array
  - custom
- Size classification (historical)

<100	SSI	1963
100-3000	MSI	1970
3000-30,000	LSI	1975
30,000-1,000000	VLSI	1980
>1,000000	ULSI	1990
>1 billion	GSI	2010

Transistor Counts



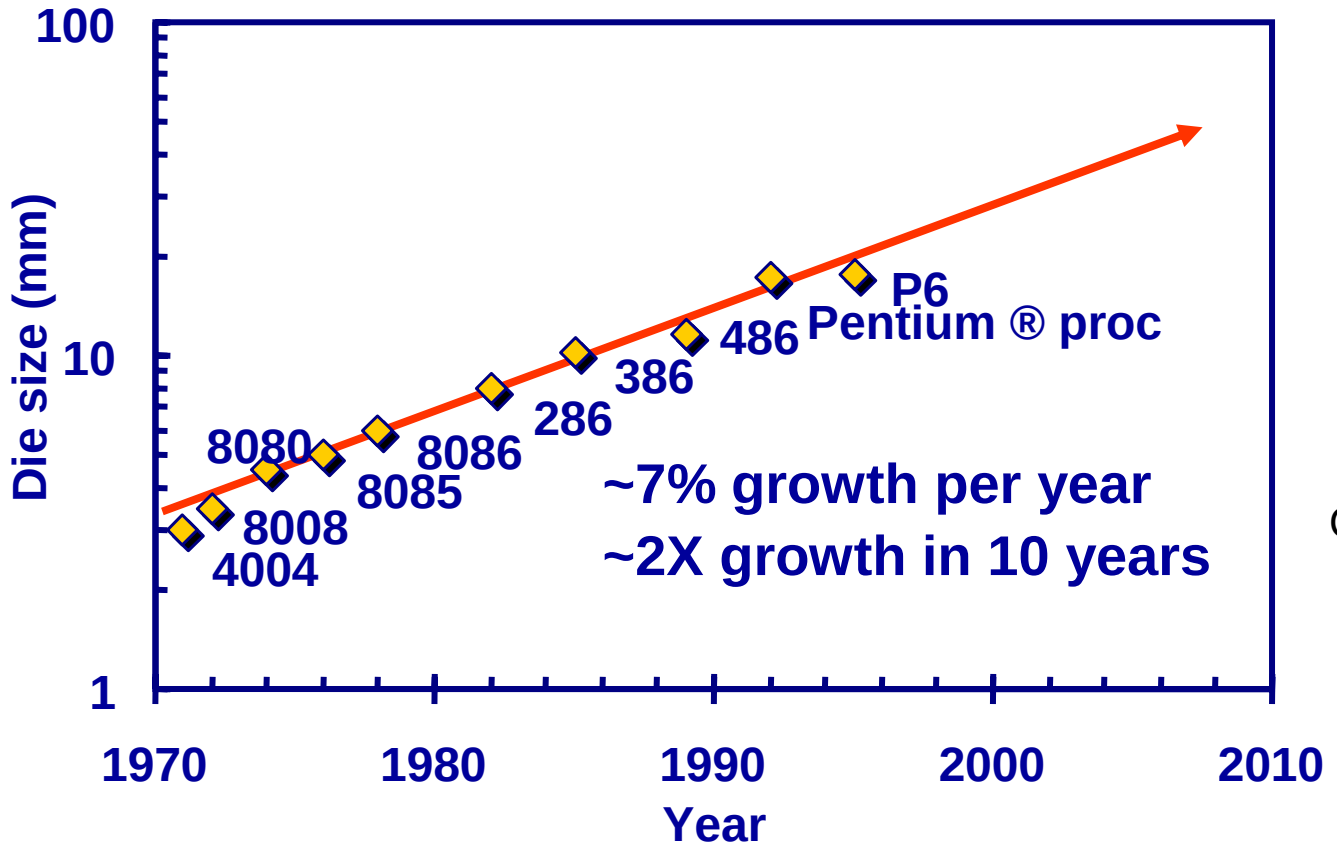
Moore's law in Microprocessors



Courtesy, Intel

Transistors on Lead Microprocessors double every 2 years

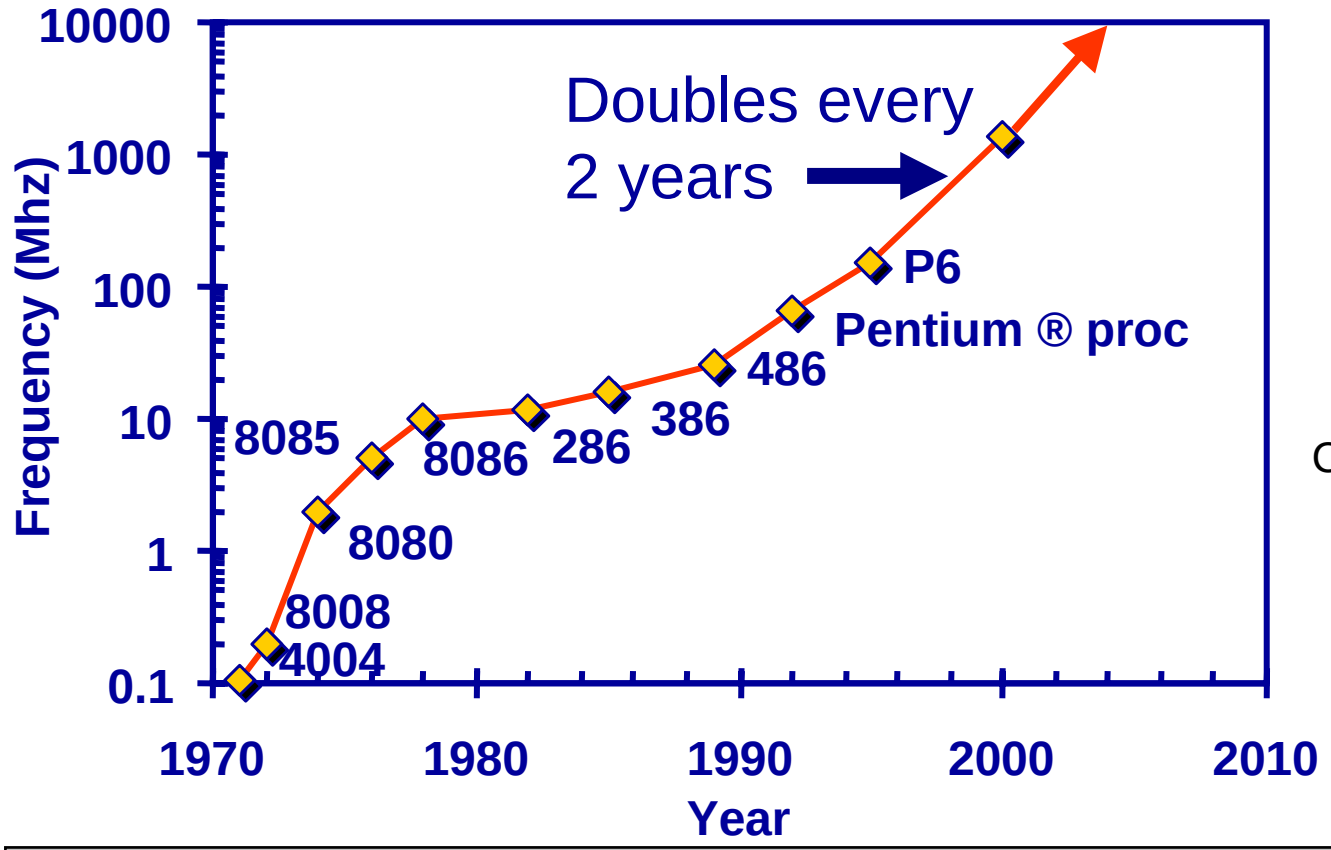
Die Size Growth



Courtesy, Intel

Die size grows by 14% to satisfy Moore's Law

Frequency



Courtesy, Intel

Lead Microprocessors frequency doubles every 2 years

Challenges in Digital Design

∝ DSM

"Microscopic Problems"

- Ultra-high speed design
- Interconnect
- Noise, Crosstalk
- Reliability, Manufacturability
- Power Dissipation
- Clock distribution.

∝ 1/DSM

"Macroscopic Issues"

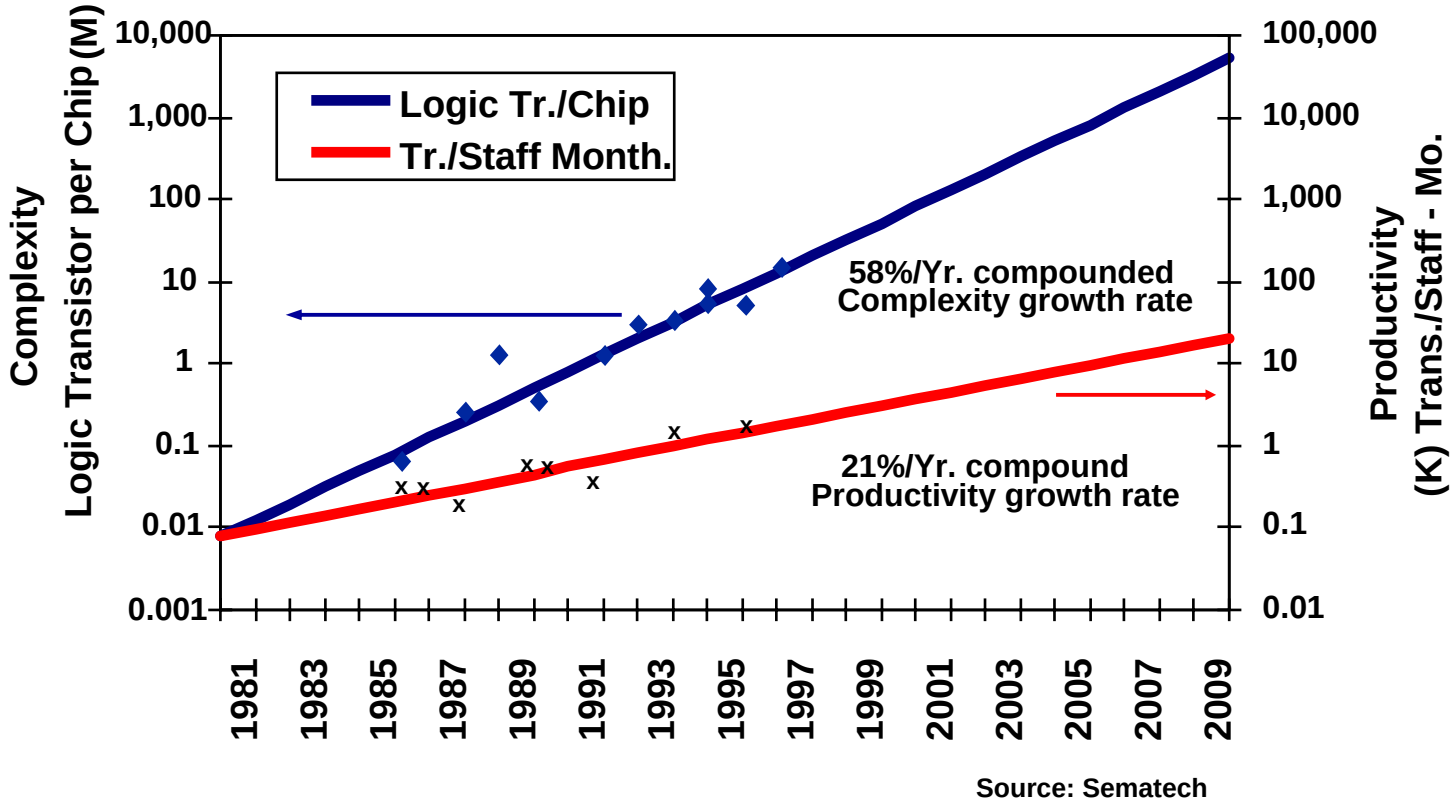
- Time-to-Market
- Millions of Gates
- High-Level Abstractions
- Reuse & IP: Portability
- Predictability
- etc.

Everything Looks a Little Different

?

…and There's a Lot of Them!

Productivity Trends



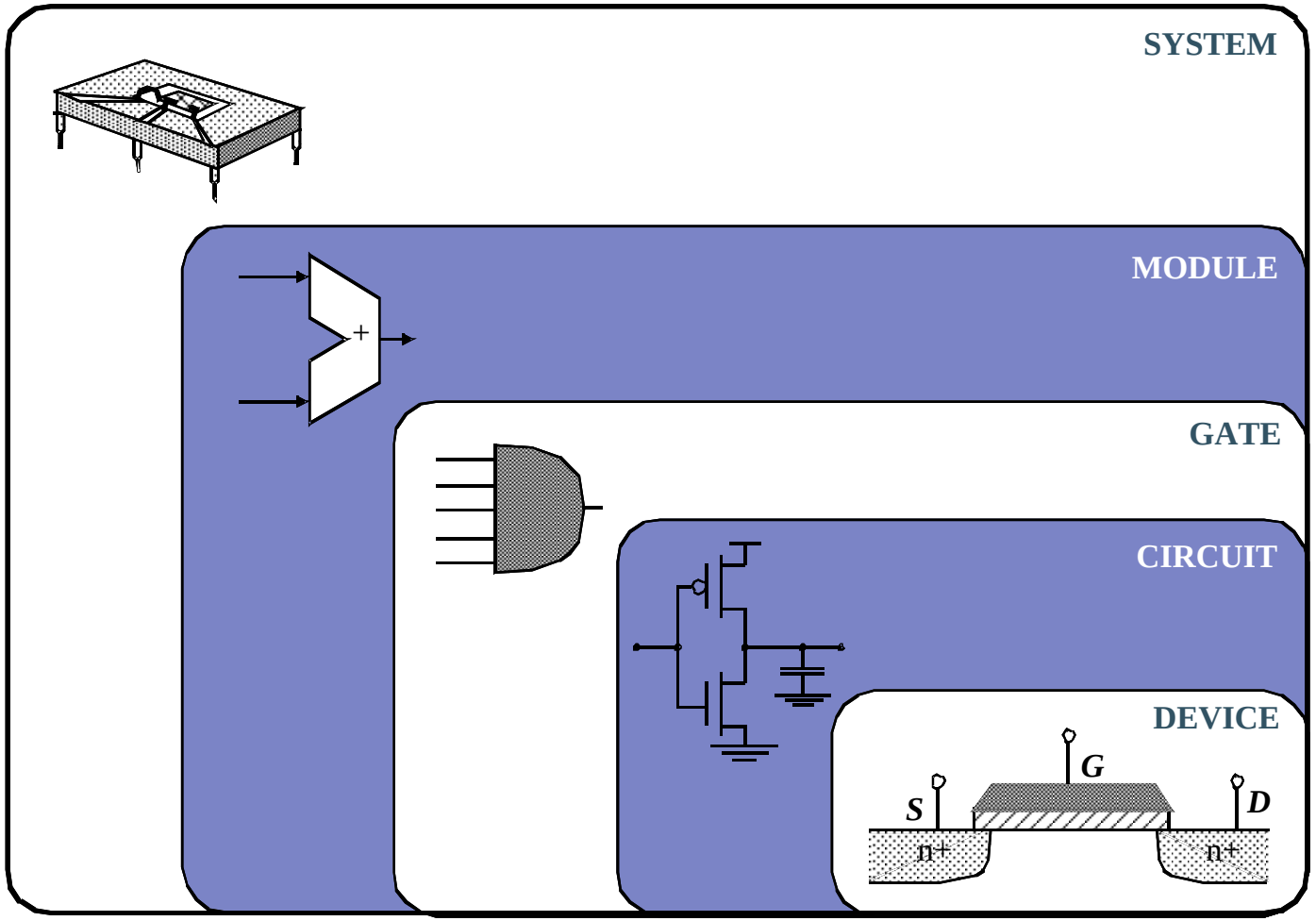
Complexity outpaces design productivity

Courtesy, ITRS Roadmap

Why Scaling?

- Technology shrinks by 0.7/generation
- With every generation can integrate 2x more functions per chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Design Abstraction Levels



VLSI Design Metrics

- How to evaluate performance of a digital circuit (gate, block, …)?
  - Cost
  - Reliability
  - Scalability
  - Robustness
  - Speed (delay, operating frequency)
  - Power dissipation
  - Energy to perform a function

VLSI Designer's Tasks

- Job of VLSI designer: design a circuit block to meet one or more objectives:
  - Maximize speed, performance
  - Minimize power consumption
  - Minimize area
  - Noise immunity (robustness)
- How?
  - Choice of circuit style (static, dynamic, etc)
  - Circuit design, transistor sizing
  - Interconnect design, efficient layout

VLSI Design Challenges

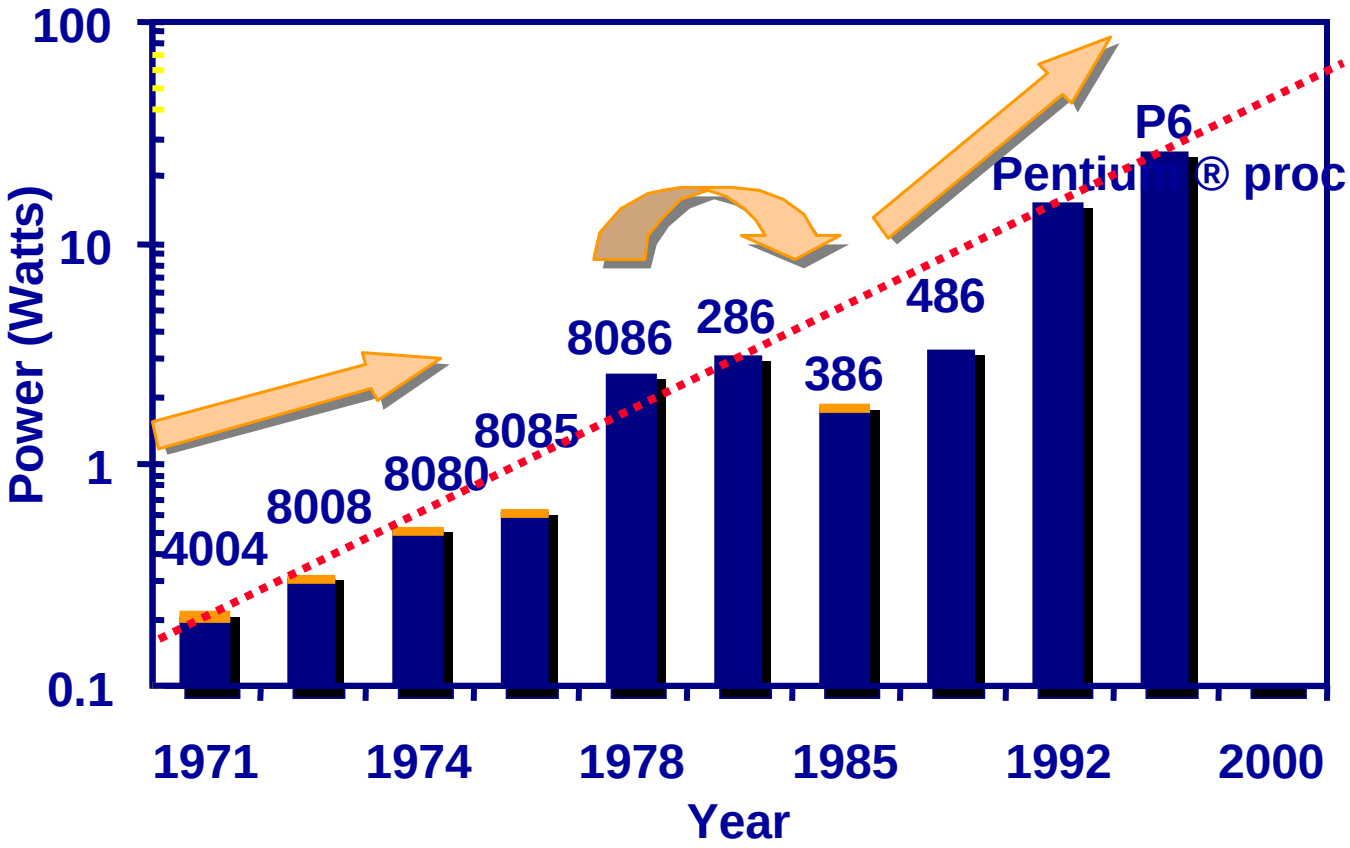
- design challenges
  - Power consumption, especially leakage power. Also affects chip cooling.
  - Noise issues, as transistors and wires move closer together. Design of noise-tolerant circuits.
  - Clocking: distributing high-frequency clock with minimum of skew (difference in clock arrival time between points on a chip)

Variability affects all of the above…..

VLSI Design Challenges

- design challenges, continued
  - Scaling: continue to make transistors smaller. Why? Smaller transistors are faster, can put more transistors on a die
  - Integration: combining large VLSI systems to form a “system-on-a-chip”
    - Design for reuse
    - Design for testability
    - Advanced CAD tools required

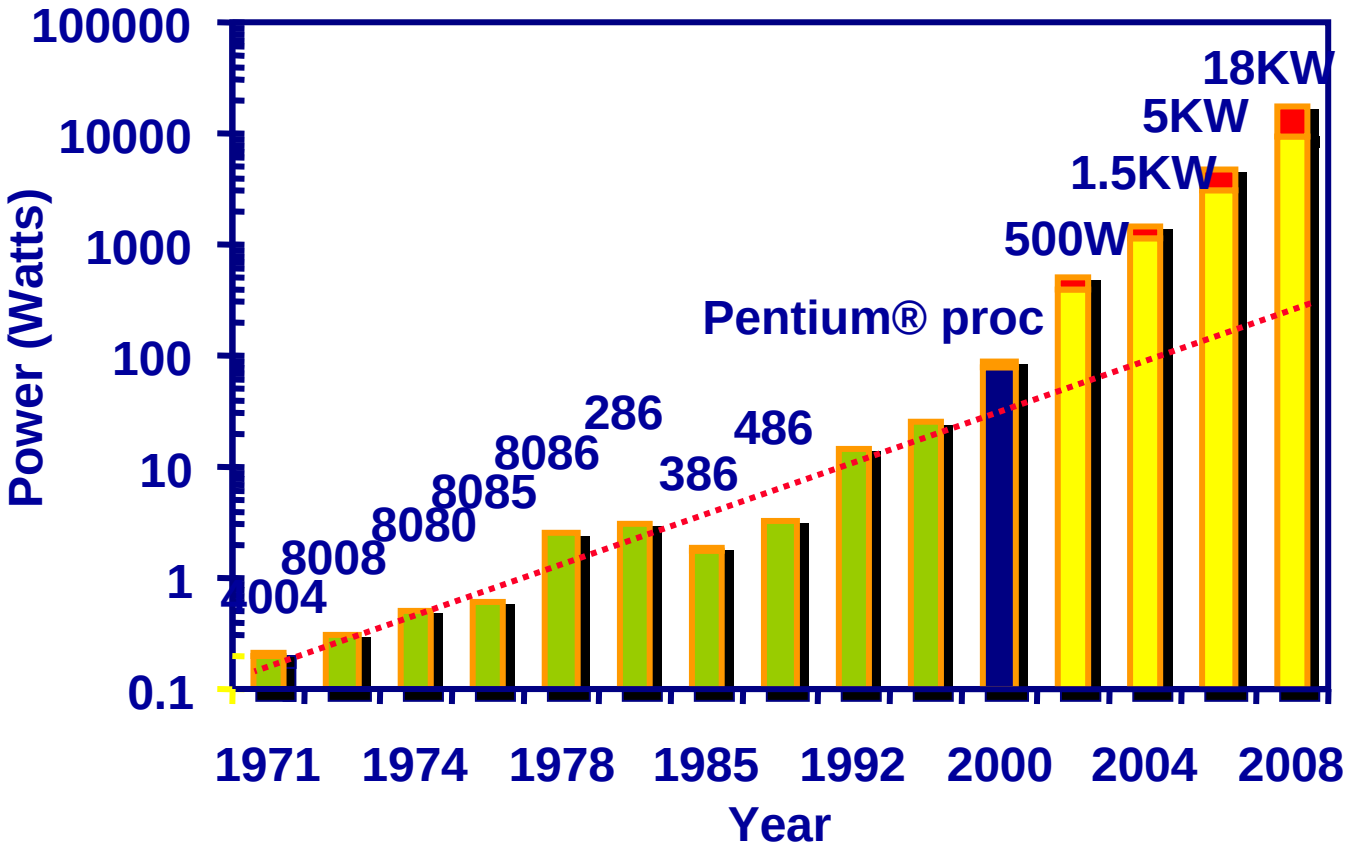
Power Dissipation



Courtesy, Intel

Lead Microprocessors power continues to increase

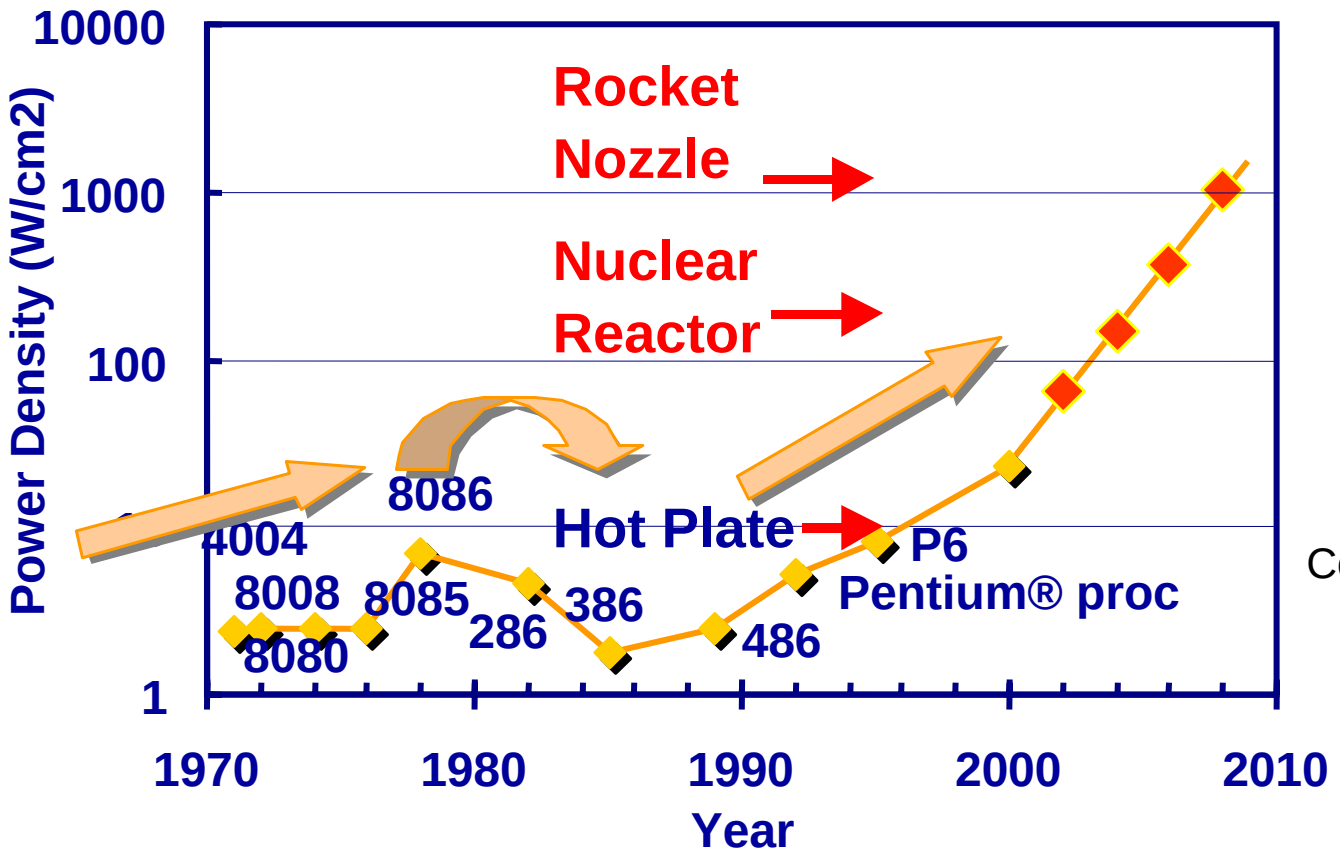
Power will be a major problem



Courtesy, Intel

Power delivery and dissipation will be prohibitive

Power density



Courtesy, Intel

Power density too high to keep junctions at low temp

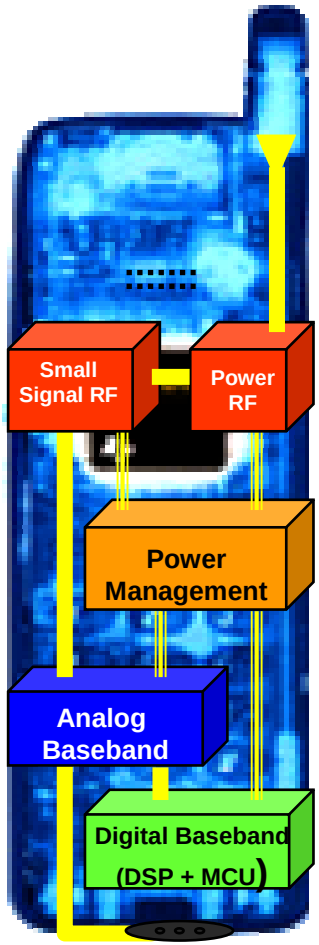
Not Only Microprocessors

Cell Phone

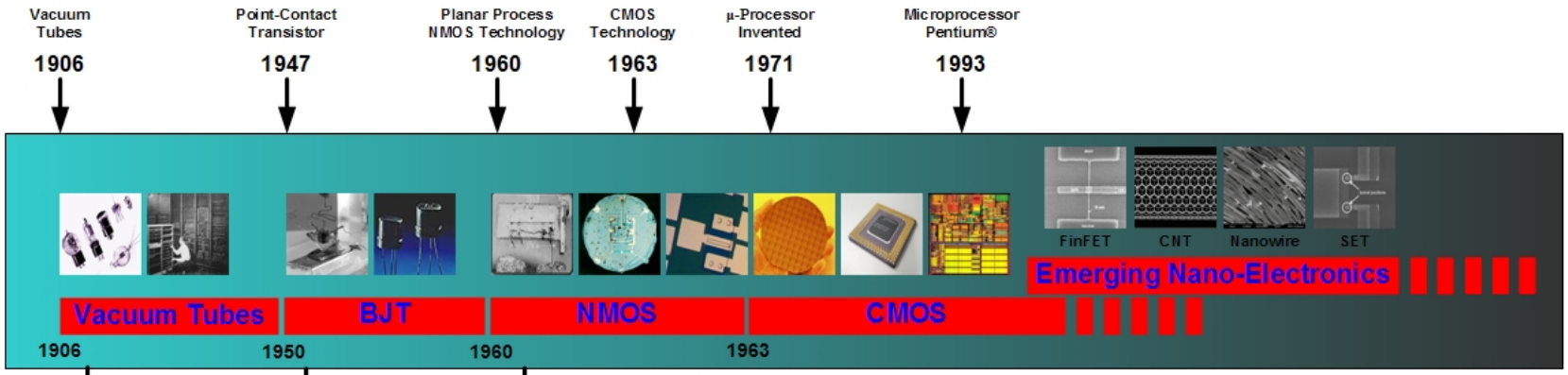
Digital Cellular Market (Phones Shipped)

	1996	1997	1998	1999	2000
Units	48M	86M	162M	260M	435M

(data from Texas Instruments)



Historical Perspective....



CMOS

(1) Easier control over processing (2) High circuit integration density (3) low cost (4) low power consumption
Due to technology scaling, leakage power dissipation and associated thermal problems are increasingly becoming major barriers in further advancement of CMOS technology.

Technology	Circuit level	System level
1. Scaling	1. Gate sizing	1. Heat sink
2. Copper wiring	2. Sleep transistor	2. Packaging materials
3. Low-k dielectrics	3. Stack forcing	3. Cooling techniques
	4. Variable Threshold CMOS (VTCMOS)	4. Heat pipes or folded fin assemblies
	5. Multi-Threshold CMOS (MTCMOS)	5. Refrigeration
	6. Input vector modification	
	7. Adaptive supply and body biasing	
	8. Optimal Vdd and Vth selection	

NMOS

(1) Easier control over processing (2) High circuit integration density (3) low cost (4) Lesser power dissipation than BJT (5) NMOS preferred over PMOS due to higher electron mobility (hence higher speed).
NMOS integrated circuits have large static power consumption.

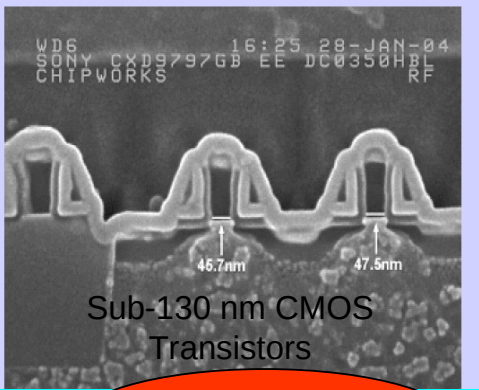
BJT

Bipolar junction transistors have high current drive capability and superior analog performance. This type of transistor is widely used as an amplifier and is also a key component in oscillators, high-speed integrated circuits, and switching circuits.
Device parameters for BJT are hard to control. Power consumption of BJT is extremely high limiting its integration density.

Vacuum Tube

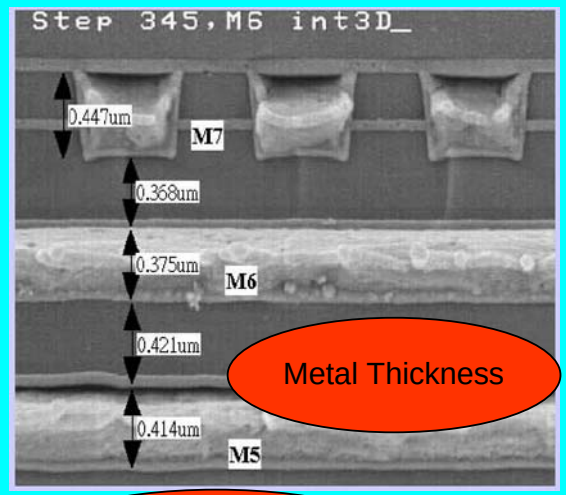
During World War II, urgent military requirements started to push the vacuum-tube technology. The technology had fully matured with a wide range of tubes—diodes, pentodes, CRT's, klystrons, and traveling-wave tubes—in high-volume manufacture. Vacuum tubes were the key component in an array of electronic equipment that seemed to meet all conceivable information needs. Radio equipment—AM, FM, and microwave—was in wide use.
Vacuum tubes had low speed, short life, high power consumption. They were bulky and fragile. These disadvantages eventually limited their further progress.

Process, Temperature and Voltage Variations

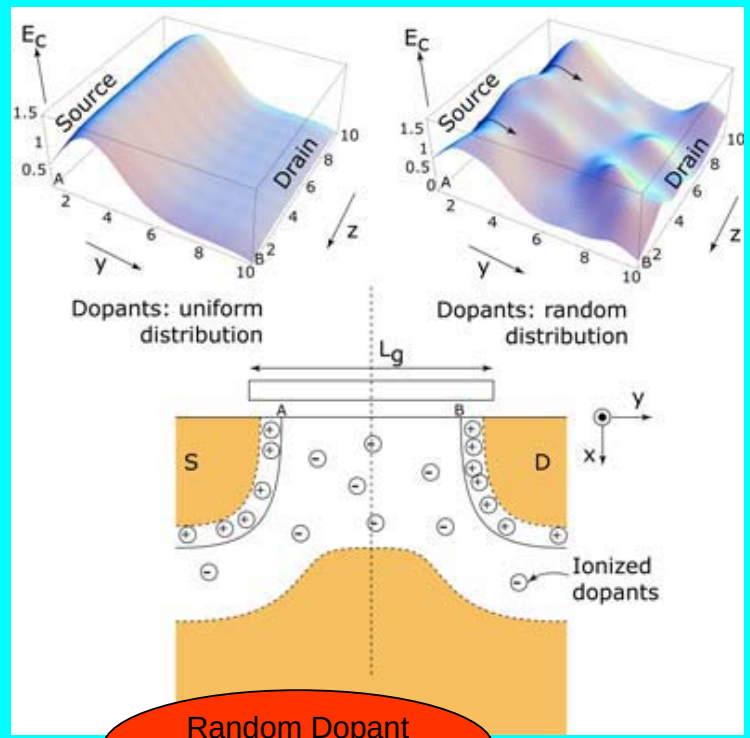


Sub-130 nm CMOS Transistors

Transistor channel length

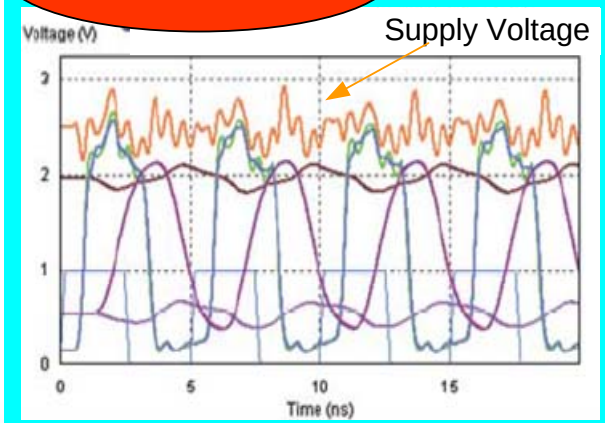


Metal Thickness

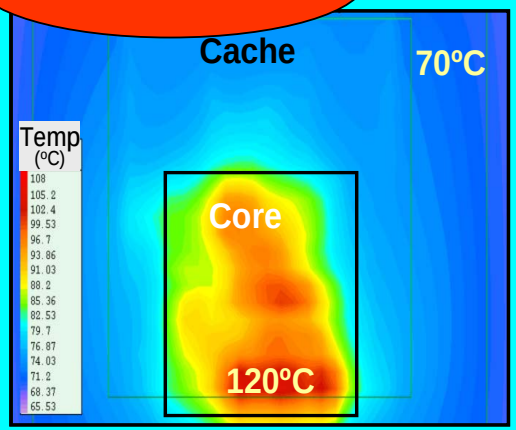


Random Dopant Fluctuations

Power Supply Voltage

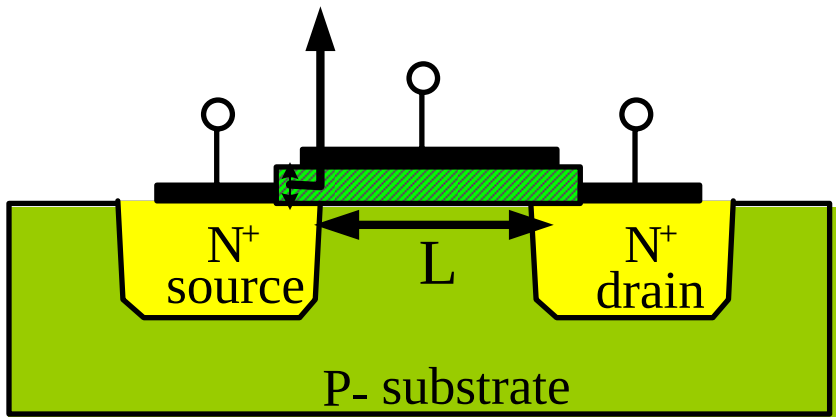


Chip Temperature



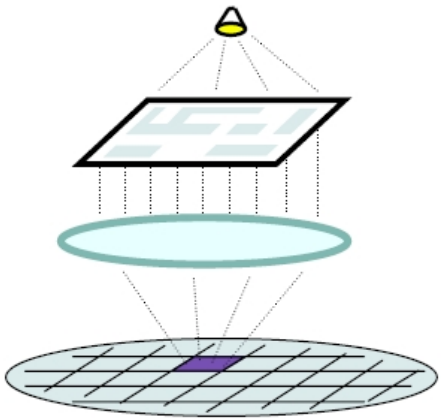
Key Parameter Variations

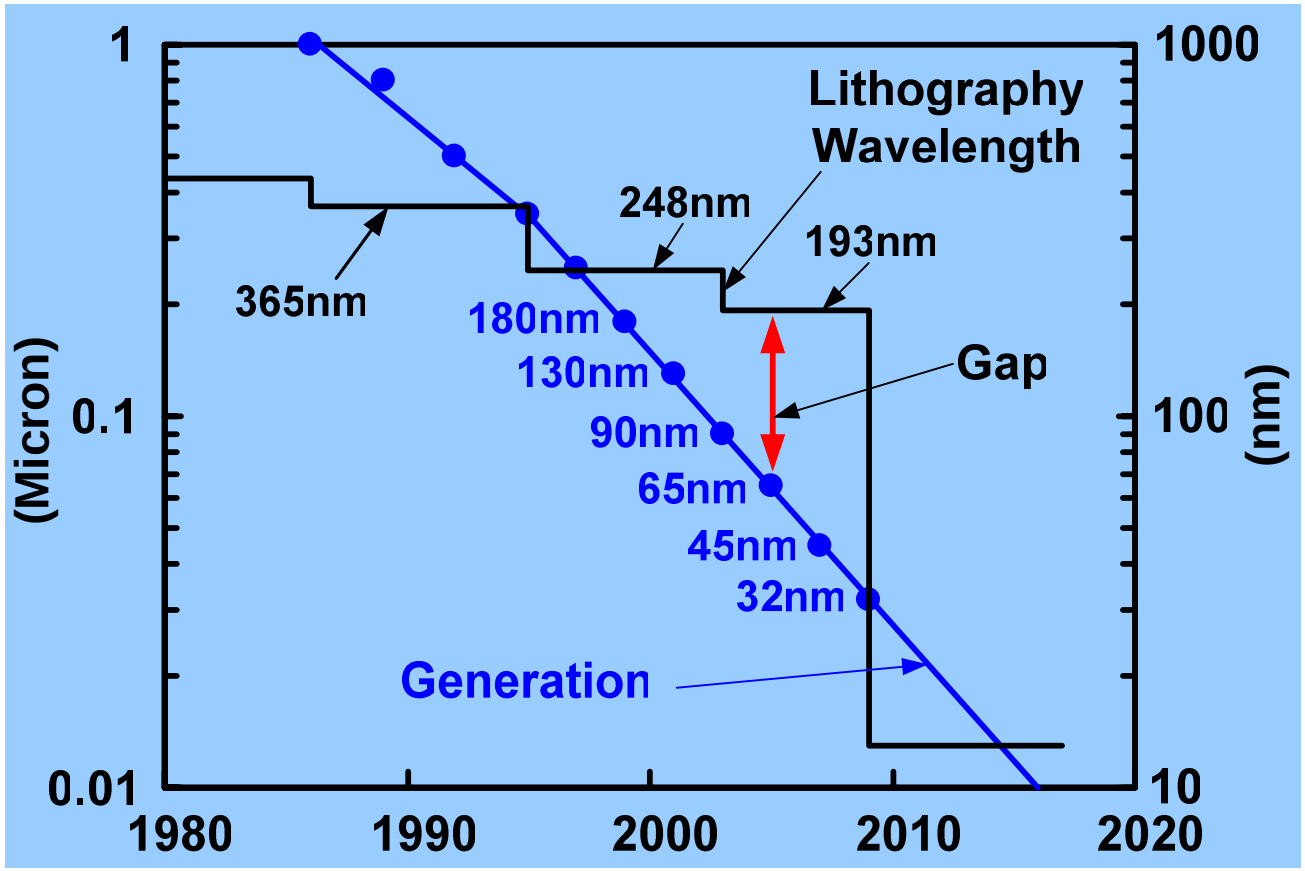
- Within-die Parameter Variations
  - Channel Length (*L*)
  - Oxide Thickness (*tox*)
  - Temperature (*T*)
  - Supply Voltage (V_{dd})



- Die-to-Die Parameter Variations
  - Channel Length (*L*)
  - Temperature (*T*)

Why Channel Length Variations are Increasing?



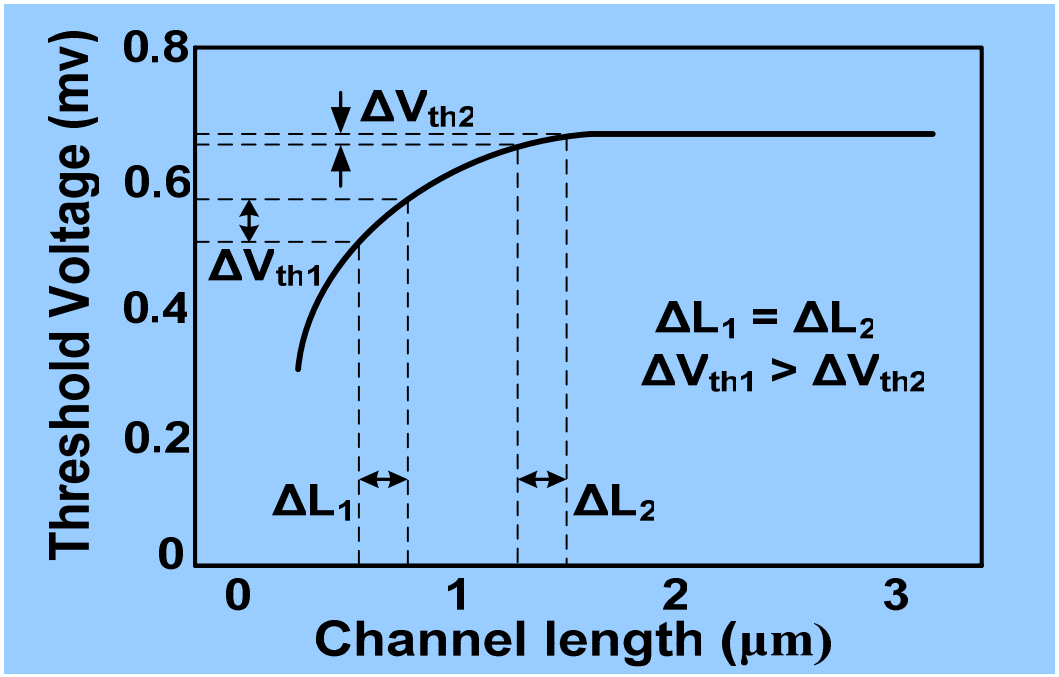


(S. Borkar et al. DAC2003)

- Minimum feature size is scaling faster than lithography wavelength
- Channel length exhibits significant amount of variations

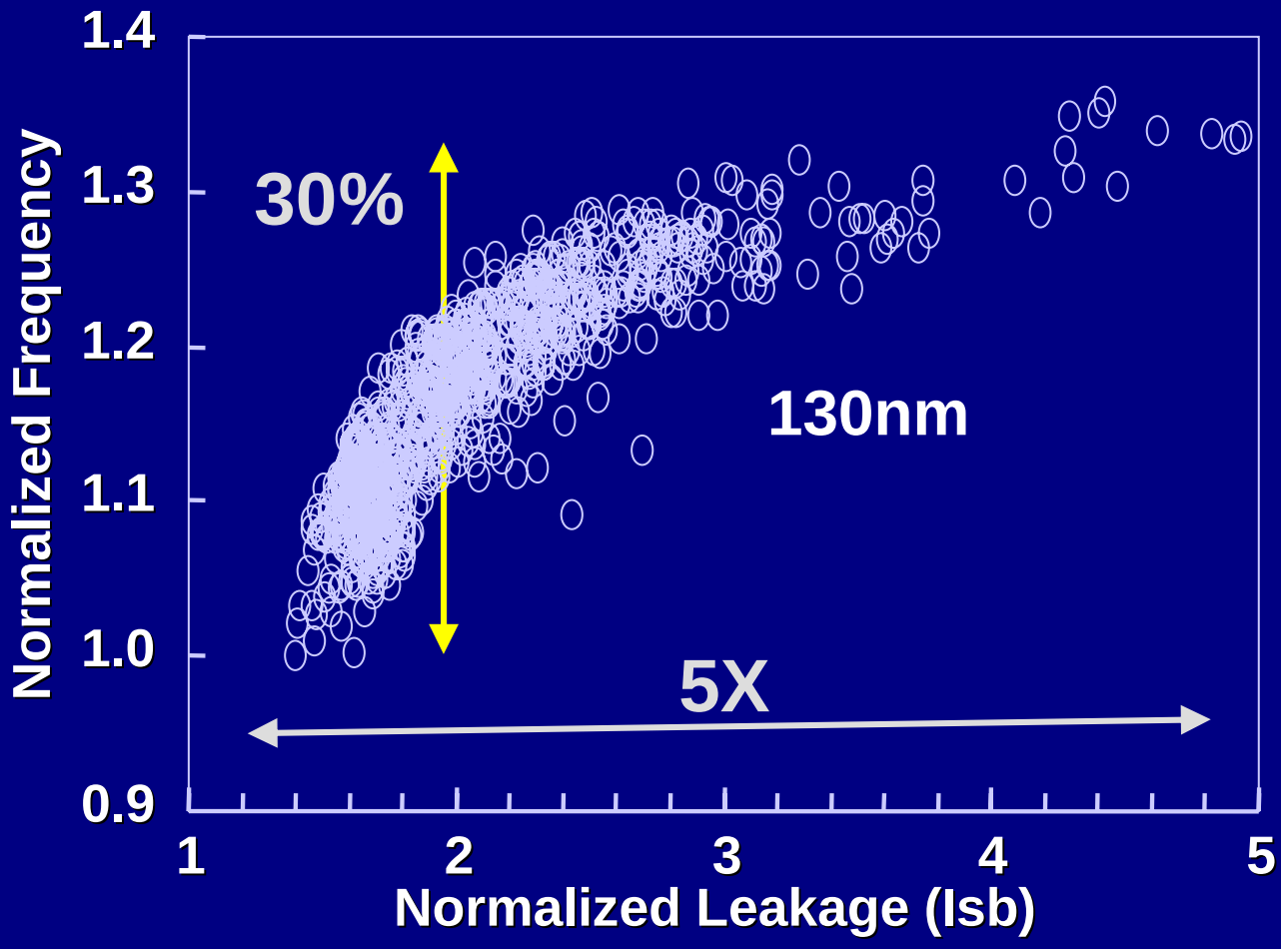
Impact of Device Scaling

Threshold voltage roll-off



- With technology scaling, the same amount of channel length variations result in greater variations in threshold voltage

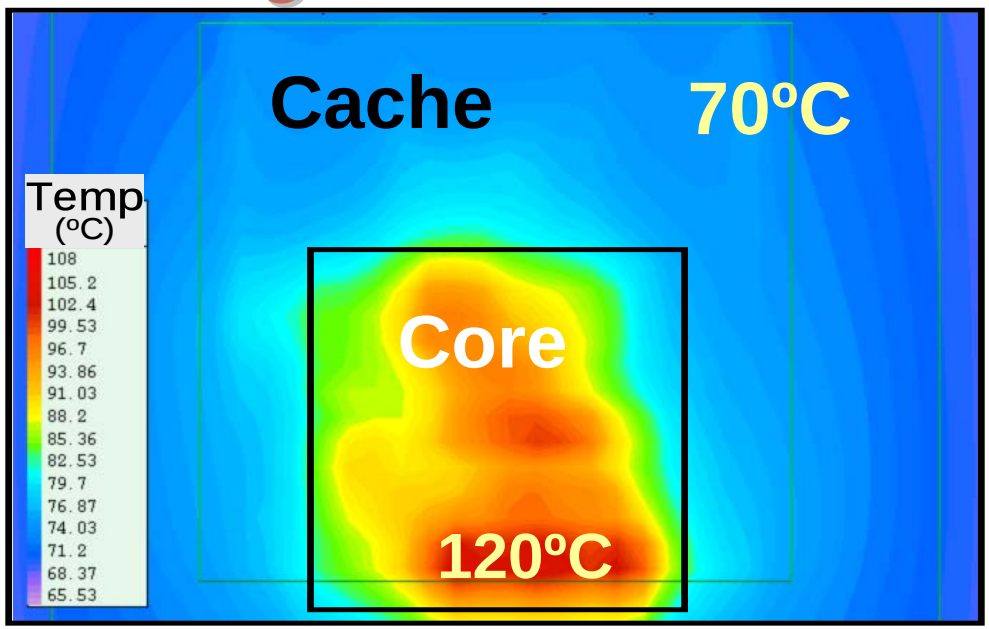
Impact of Static Variations



Frequency ~30%

Leakage Power ~5-10X

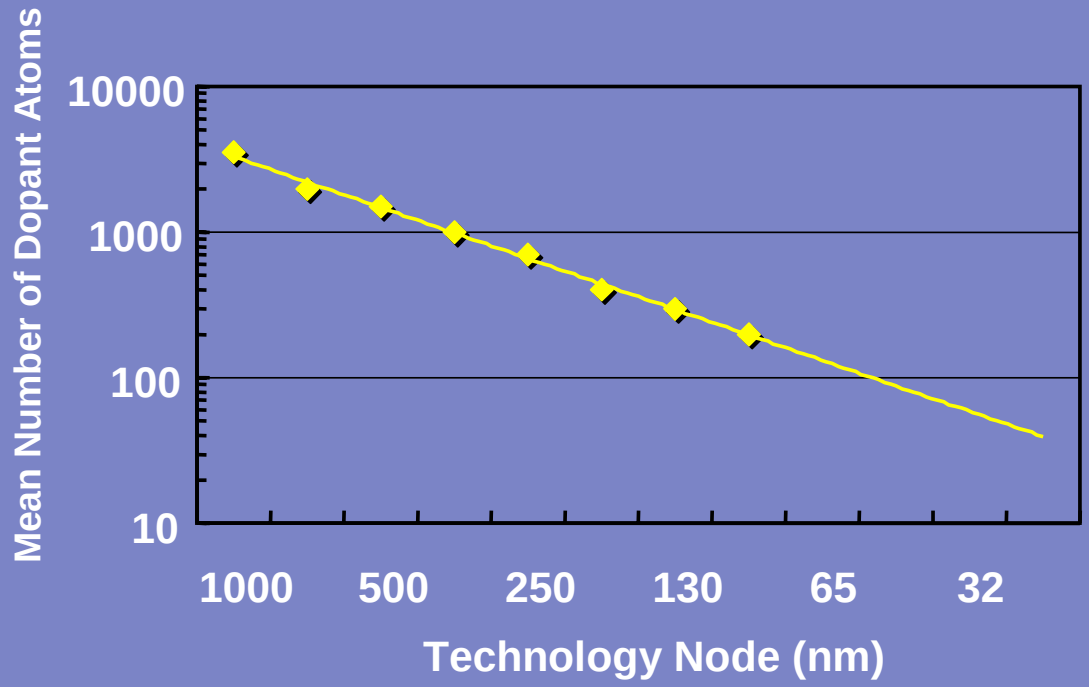
Why On-Chip Temperature Variations are Increasing?

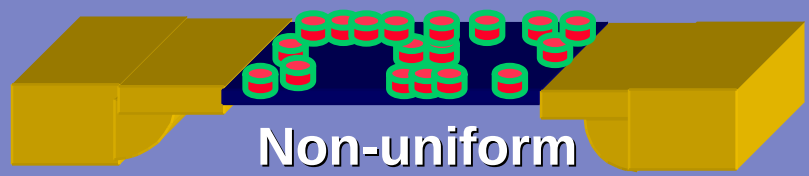


Temperature map of a high-performance microprocessor
Courtesy of S. Borkar, Intel Corporation.

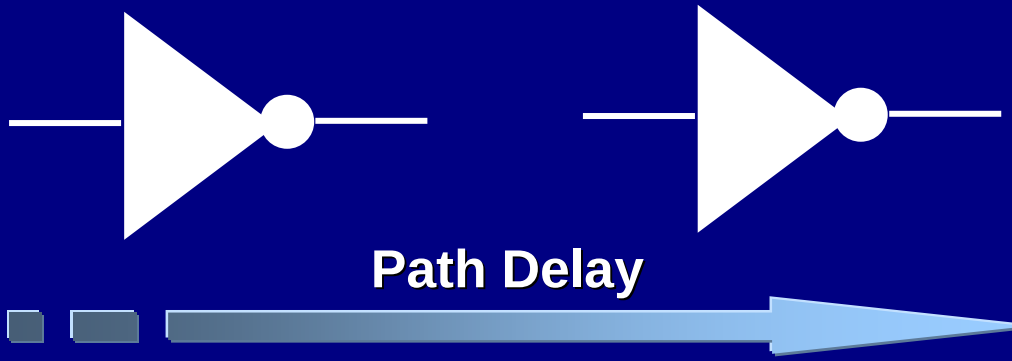
- Difference in power dissipation of various blocks
- Dynamic power management techniques such as clock gating
- Leakage power distribution

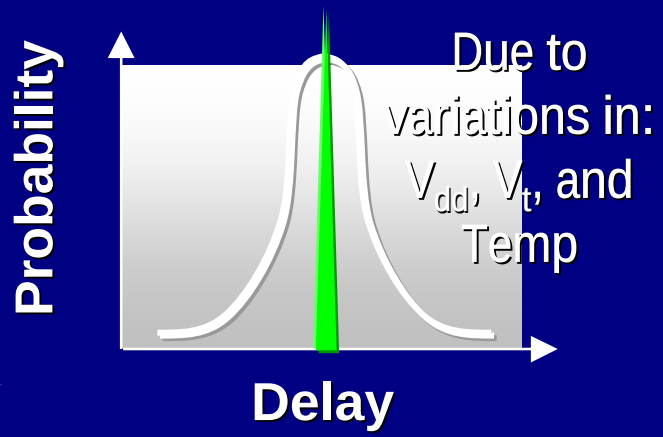
Random Dopant Fluctuations (Intrinsic)

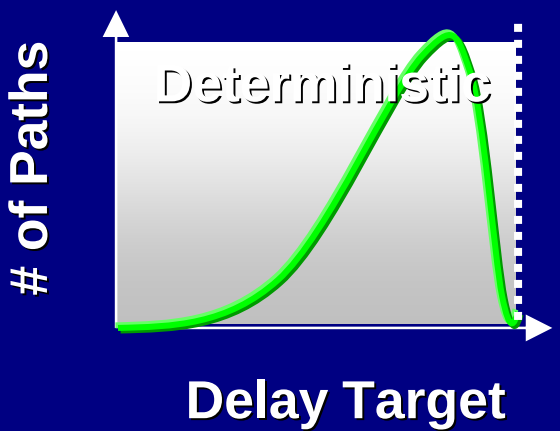


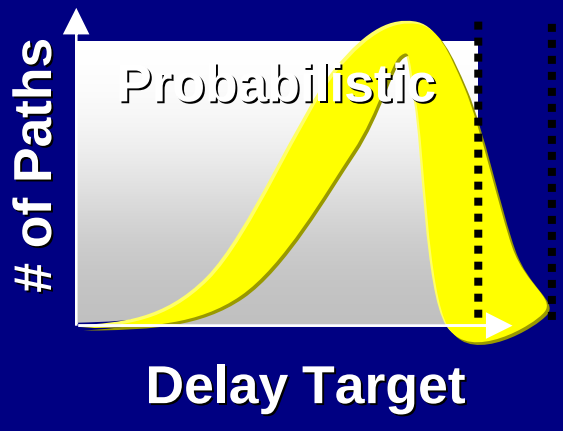


Probabilistic Design









Deterministic design techniques inadequate in the future

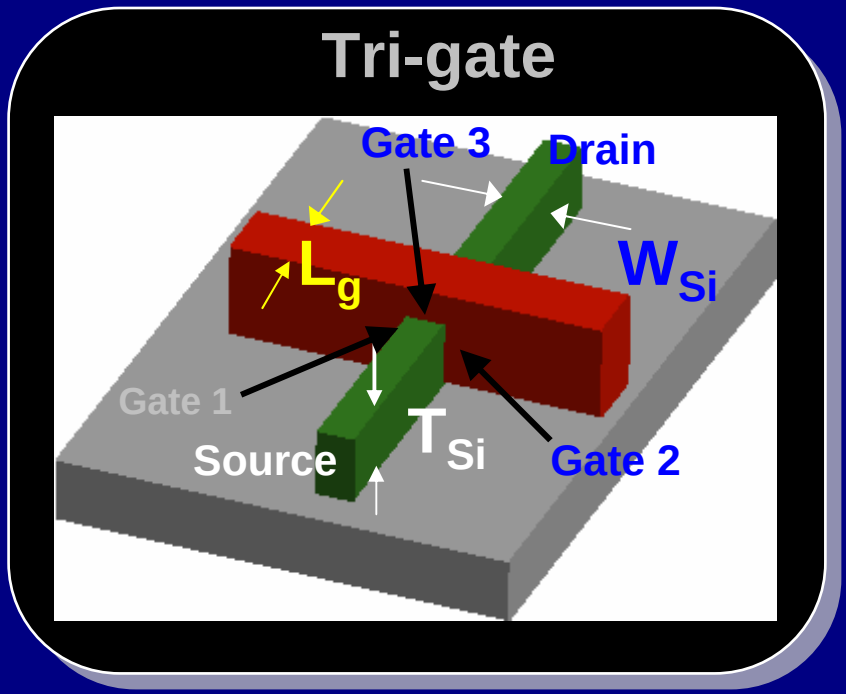
Shift in Design Paradigm

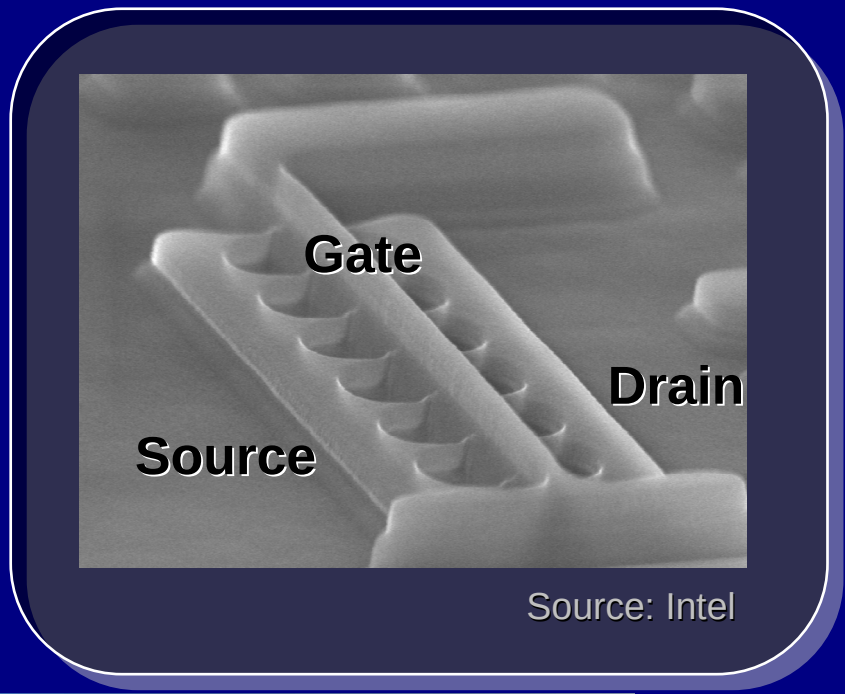
- Multi-variable design optimization for:
  - Yield and bin splits
  - Parameter variations
  - Active and leakage power
  - Performance

Today:
Local Optimization
Single Variable

Tomorrow:
Global Optimization
Multi-variate

New Transistors: Tri-Gate, Double Gate

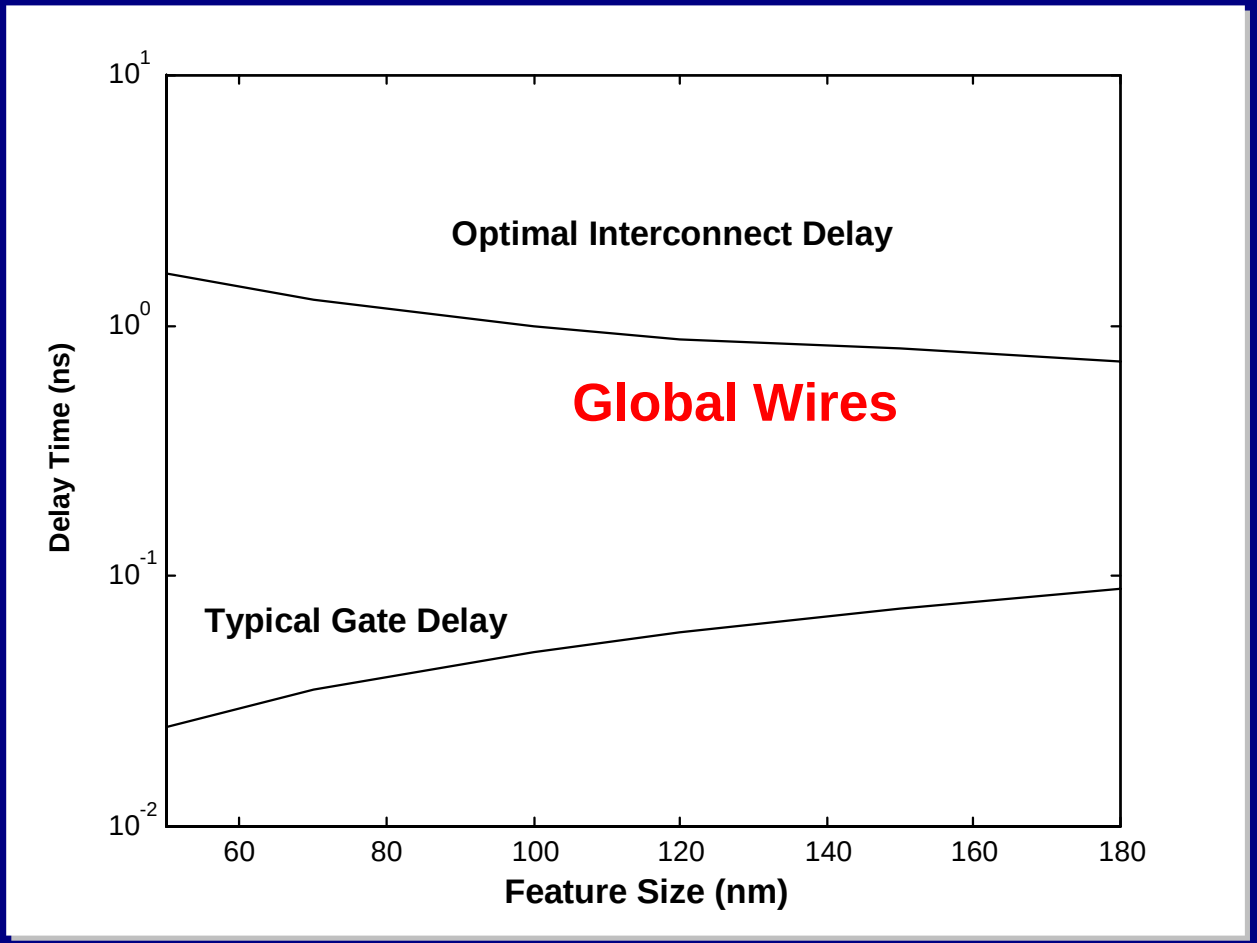




Improved short-channel effects
Higher ON current for lower SD Leakage

Identifying new parameters that may vary and impact circuit metrics

IC performance is being dominated by interconnects



K. Banerjee et al., Proc. IEEE, May 2001.

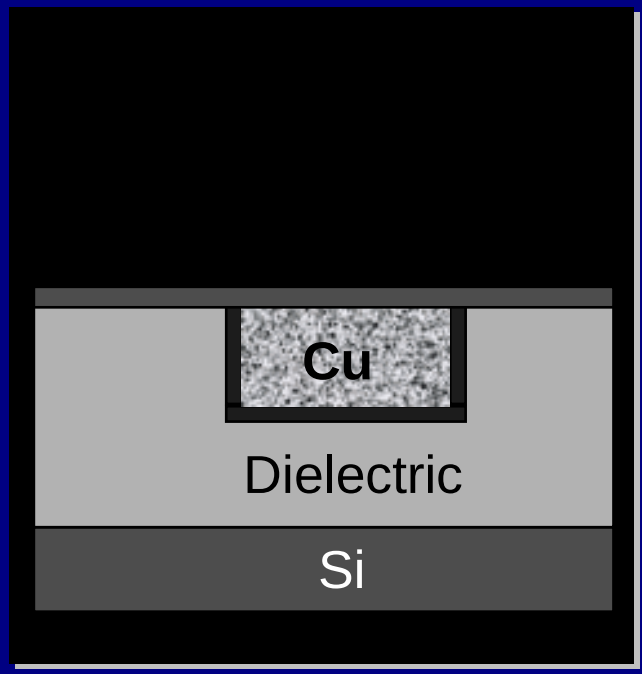
Cu Resistivity: Effect of Scaling

Effect of Cu Diffusion Barrier

- Barriers have higher resistivity
- Barriers can't be scaled below a minimum thickness

Effect of Grain Boundary Scattering

- e scattering from the G-bs
- increases effective resistivity

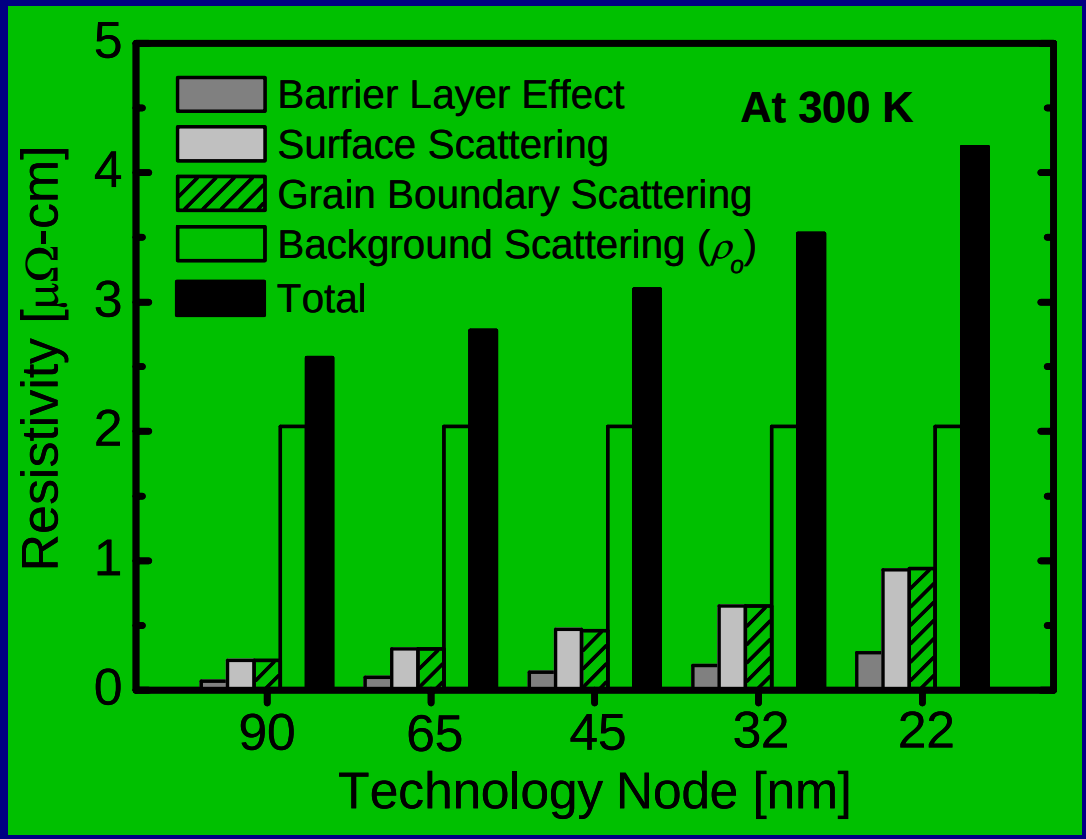


Effect of Electron Scattering

- e scattering from the surface
- further increase in effective resistivity

Problem is worse than anticipated in the ITRS roadmap

Cu Resistivity: Effect of Scaling



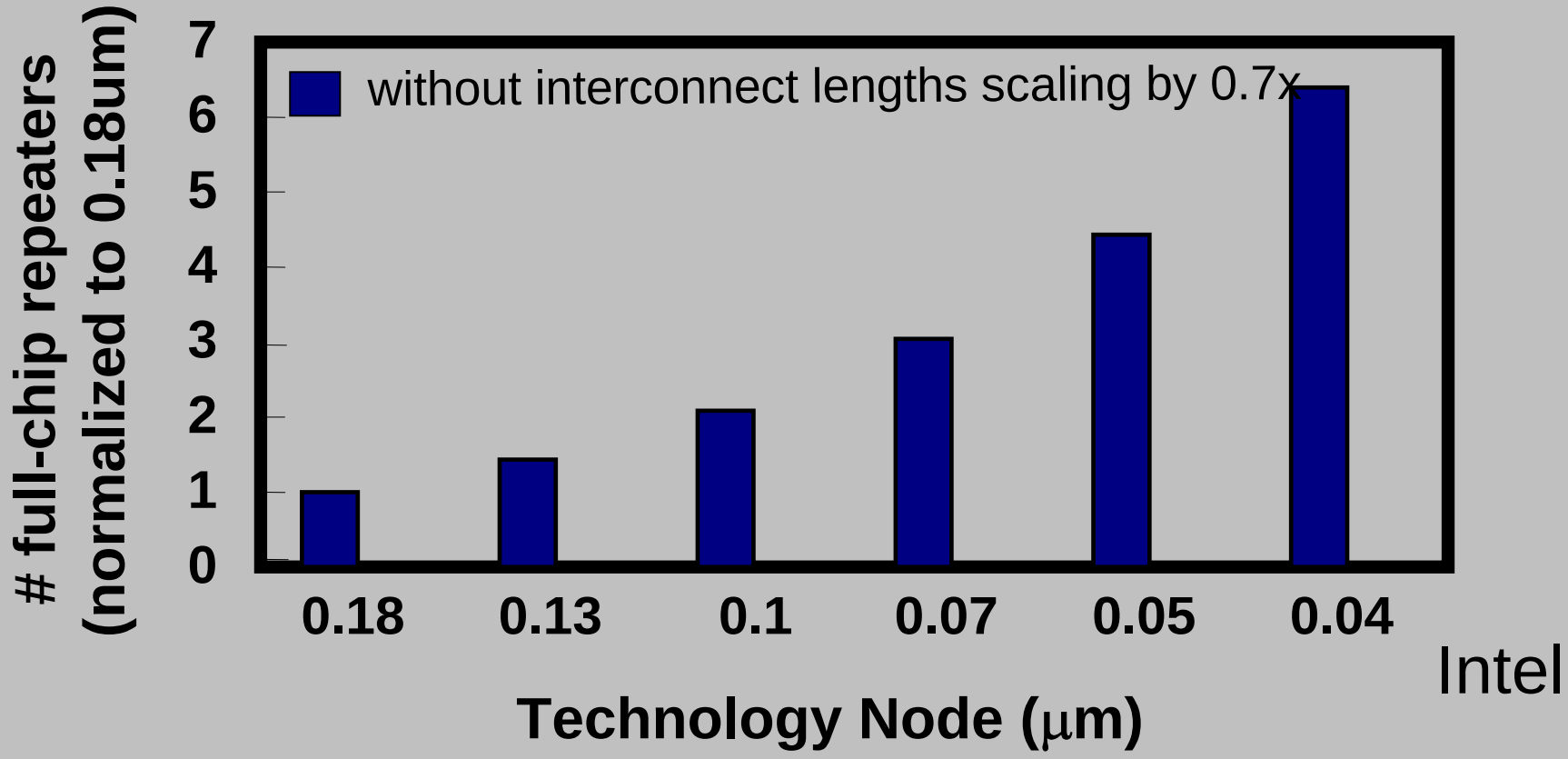
Based on analytical model in

W. Steinhogl et al., *J. Appl. Phys.*, 2005.

Im, Srivastava, Banerjee and Goodson, IEEE TED 2005 (in press)

Cu barrier layer, grain boundary and surface scattering leads to steep increase in Cu resistivity

Increasing Number of Repeaters



- **Increase in Cu resistivity will cause increase in size and number of repeaters**

Other Issues….

- Frequency of signals on interconnects is rising rapidly
- Frequency dependent impedance extraction is a major hurdle
  - Field solvers are unable to handle the complexity of VLSI interconnects
- Need to develop models for interconnect geometry dependent calculation of high frequency impedance
- Interconnect variability adds to the complexity of extraction….

Reliability Issues….affects design

- Electromigration in metal interconnects
- Self-heating issues
- Time-dependent dielectric breakdown
- NBTI
- Electrostatic discharge (ESD)