ECE 124A
VLSI Principles

Lecture 10

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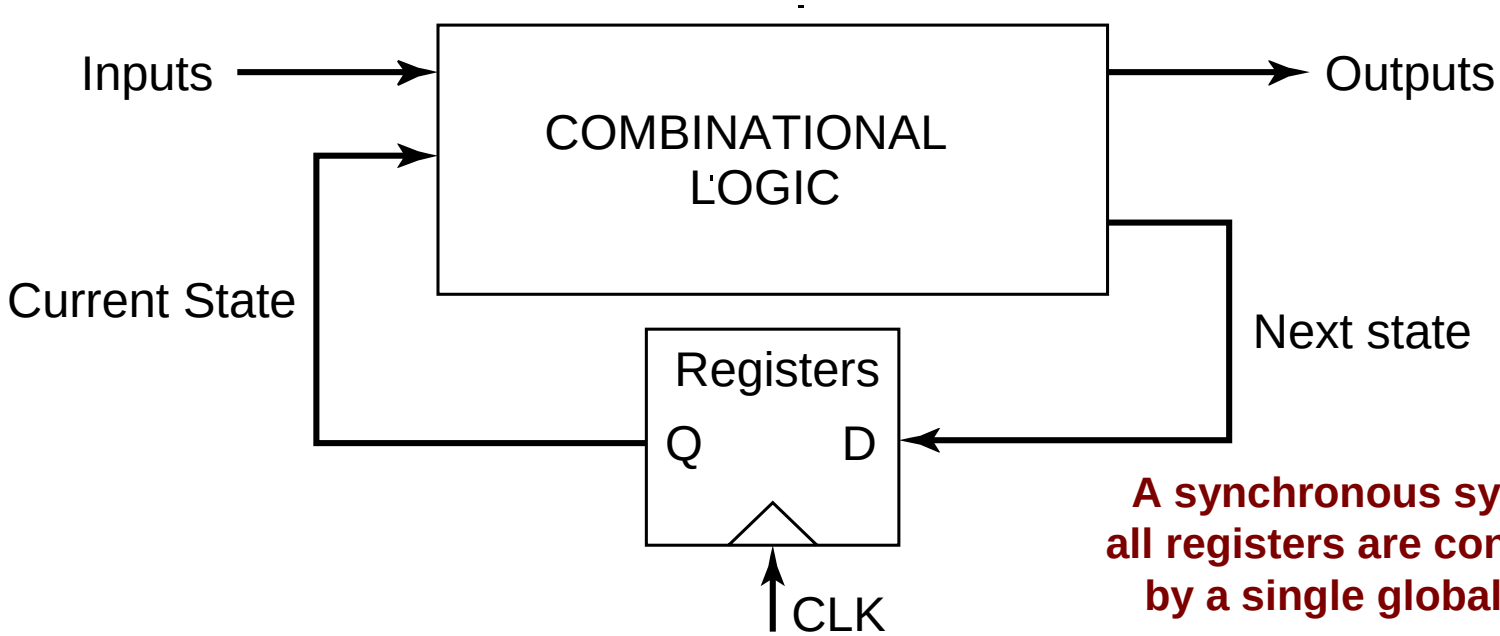
Designing Sequential Logic Circuits

Kaustav Banerjee

Sequential Logic

All useful systems require storage of state information….



A synchronous system: all registers are controlled by a single global CLK

A generic Finite State Machine (FSM) consisting of combinational logic and registers.

Output of the FSM = *F*(*current inputs*, *current state*)

Next State is determined based on current state and current inputs—fed to the input (D) of the registers

Note: There are 2 storage mechanisms: 1) positive feedback and 2) charge storage

Classification of Memory Elements

- Background Memory: large centralized memory core (high density array structures)---SRAMs and DRAMs
- Foreground Memory: embedded in a logic (individual registers or register banks)—focus of this section

Classification of Memory Elements

Static Memory:

- preserves state as long as power is ON
- built by using positive feedback or regeneration where the circuit consists of intentional connections between the output and input of a combinational circuit
- most useful when register will not be updated for extended periods of time (eg., configuration data loaded at power-up time).
- Condition also holds for most processors that use conditional clocking, (gated CLK) where the CLK is turned off for unused modules----**no guarantee on how frequently the registers will be clocked and static memories are needed to state information.**
- bistable element is the most popular form

Classification of Memory Elements

Dynamic Memory:

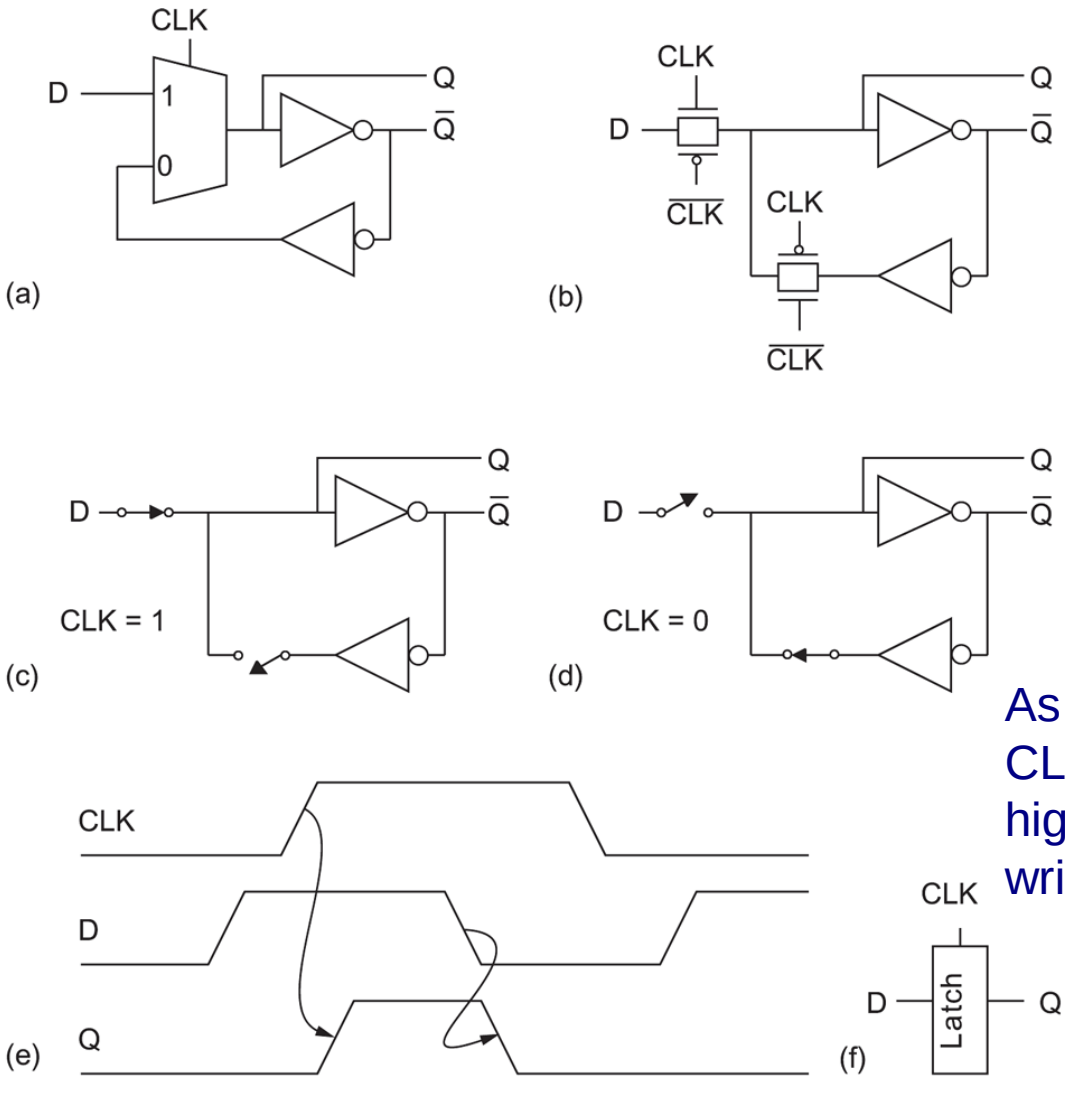
- store data for short (ms) period of time
- based on the principle of temporary charge storage on parasitic capacitors in MOS devices
- similar to dynamic logic….. capacitors need to be refreshed periodically to compensate for charge leakage
- significantly simpler----hence, provide higher performance and lower power dissipation
- most useful in datapath circuits that require higher performance levels and are **periodically clocked**

Naming Conventions

- Definitions:
  - a latch is a level sensitive device
  - a register is an edge-triggered storage element
- There are many different naming conventions
  - For instance, many books call edge-triggered elements flip-flops
  - This may lead to confusion however…
  - Any bistable component formed by the cross coupling of gates is a flip-flop (FF)

Latches

Multiplexer based



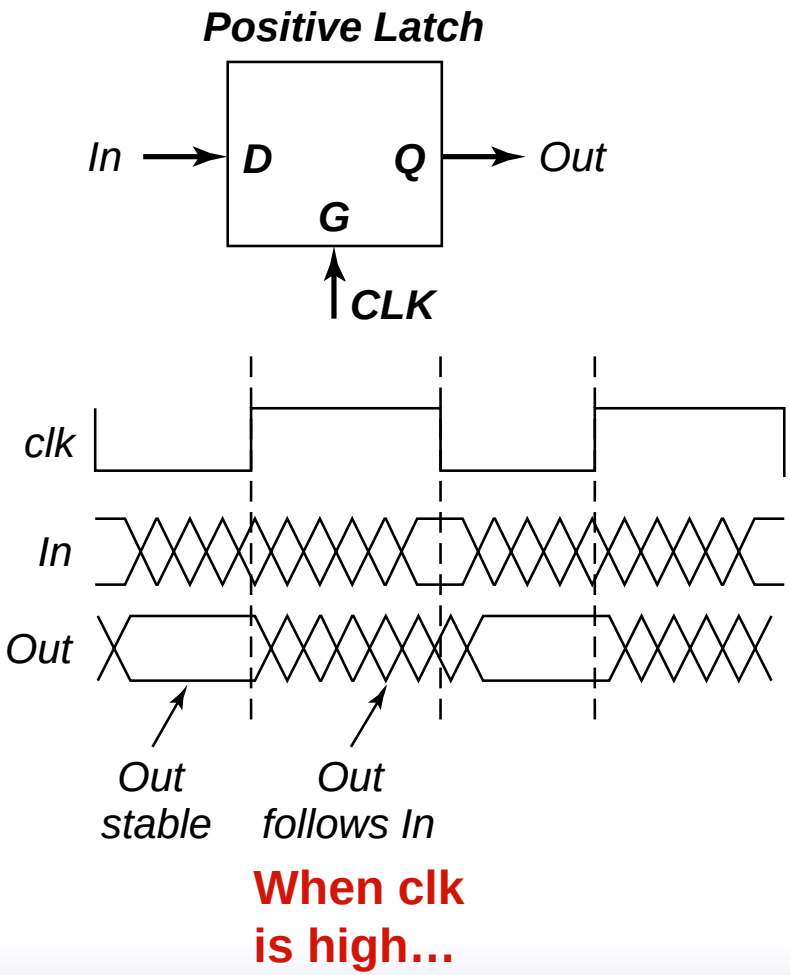
CLK=1: D to Q

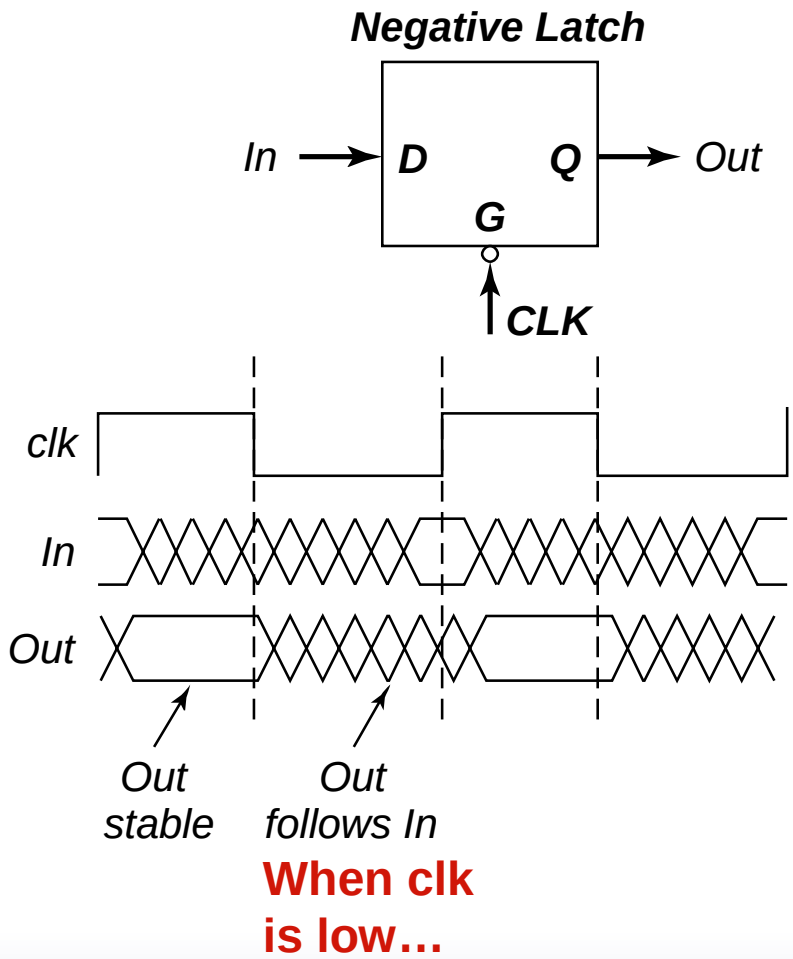
CLK=0:Holds state of Q

As long as CLK remains high, D will be written on Q

FIG 1.30 CMOS positive-level-sensitive D latch

Timing of P/N Latches

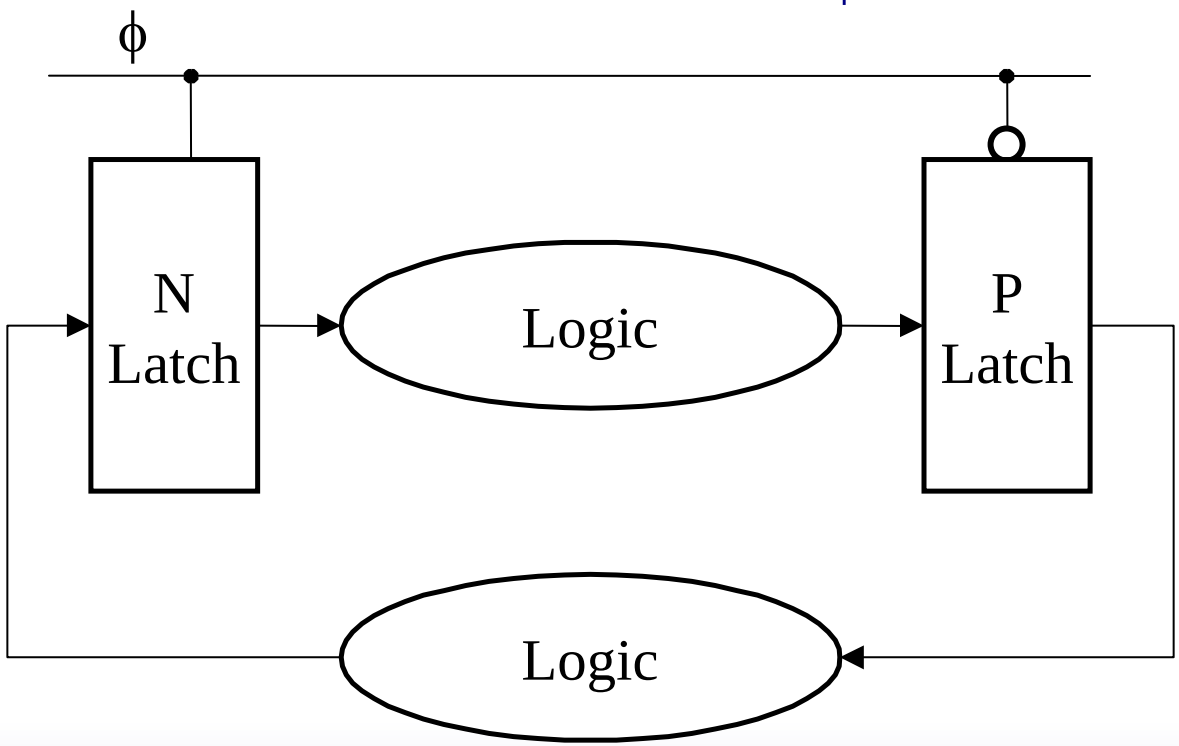




Latch-Based Design

• N (negative) latch is transparent when $\phi = 0$

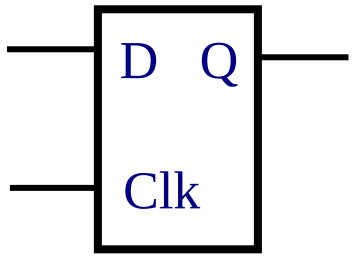
• P (positive) latch is transparent when $\phi = 1$

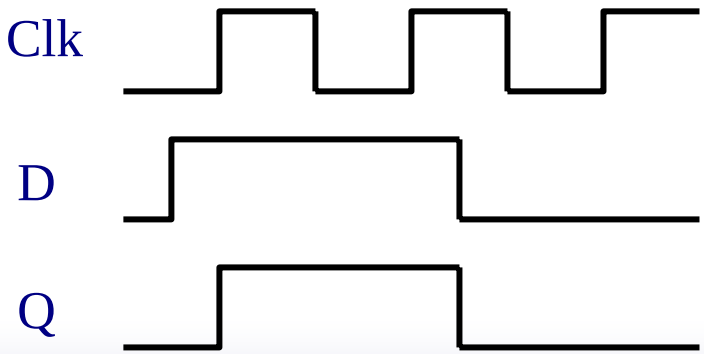


Latch versus Register

- Latch

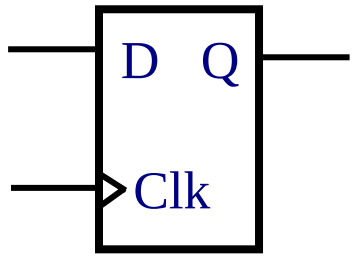
  stores data when clock is low (or high)

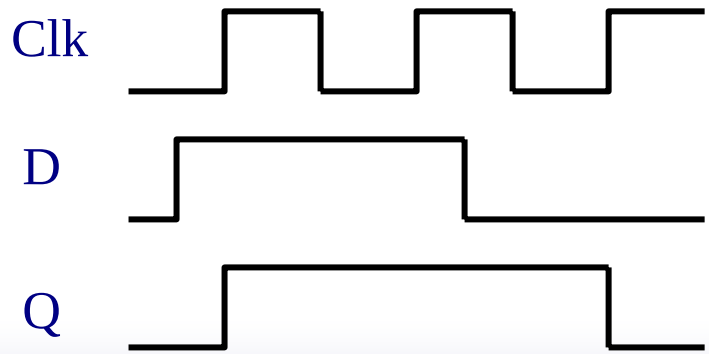




- Register

  stores data when clock rises (or falls)





Registers or Flip-Flops

Combines two latches:

One +ve sensitive (slave) and one –ve sensitive latch (master)

Edge Triggered FF or Master-Slave FF

CLK=0: D to QM

$\overline{QM} = \overline{D}$

Slave holds previous value of Q

CLK=1: master can't sample input and holds value of D

Slave opens and QM=(D) =Q

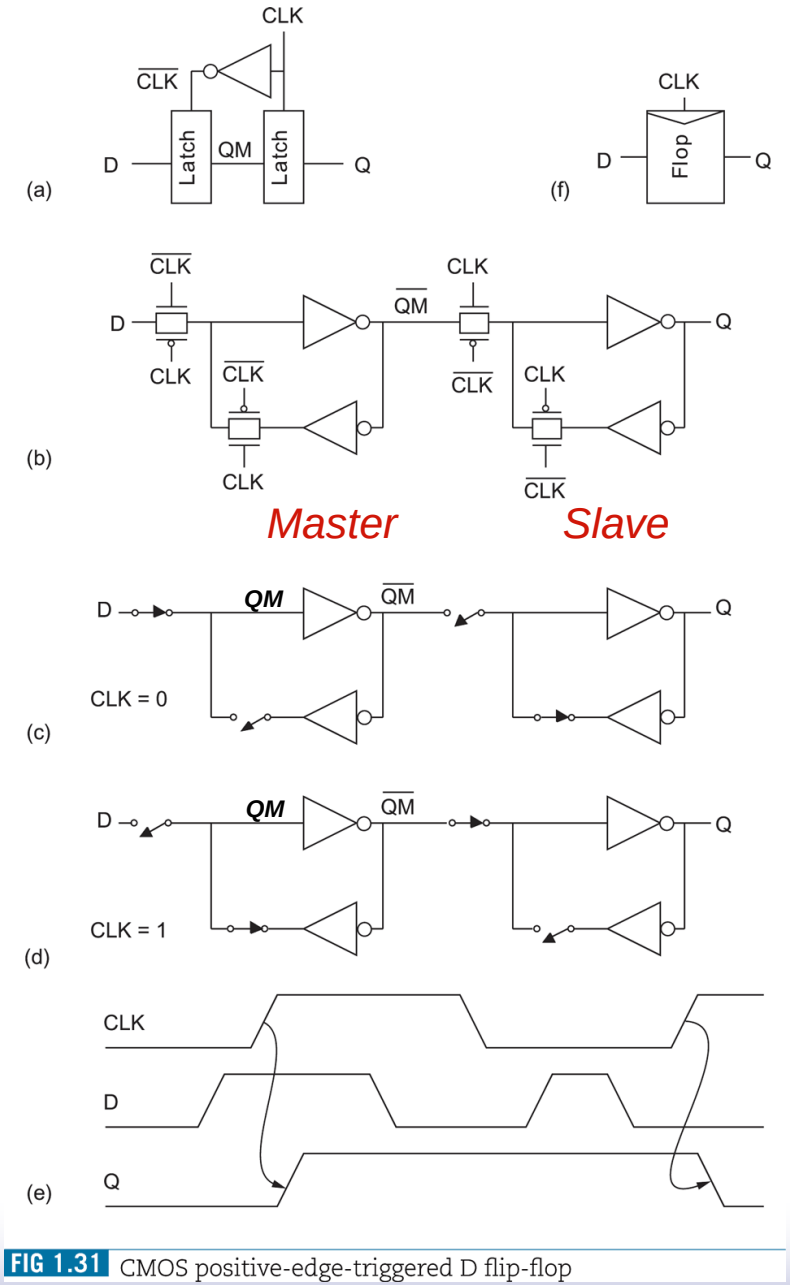
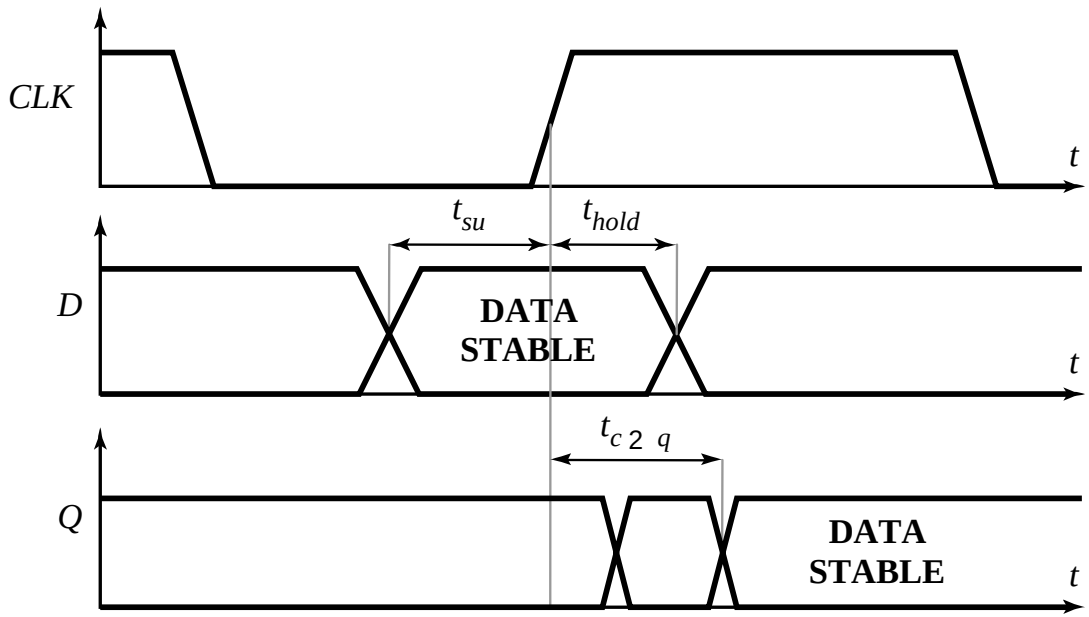
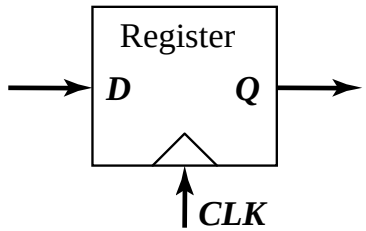


FIG 1.31 CMOS positive-edge-triggered D flip-flop

Timing Definitions





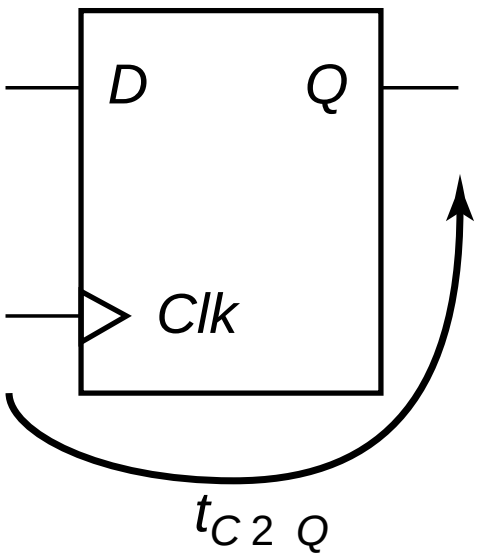
t_{su}= setup time =time for which the data inputs (D) must be valid before the CLK edge

t_{hold}= hold time =time for which data input must remain valid after the CLK edge

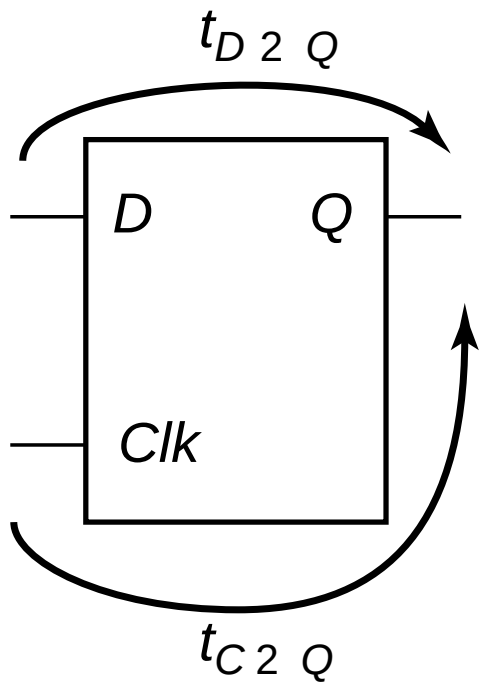
t_{c2q}= worst case propagation time through the Register (w.r.t the CLK edge)

Characterizing Timing

Register

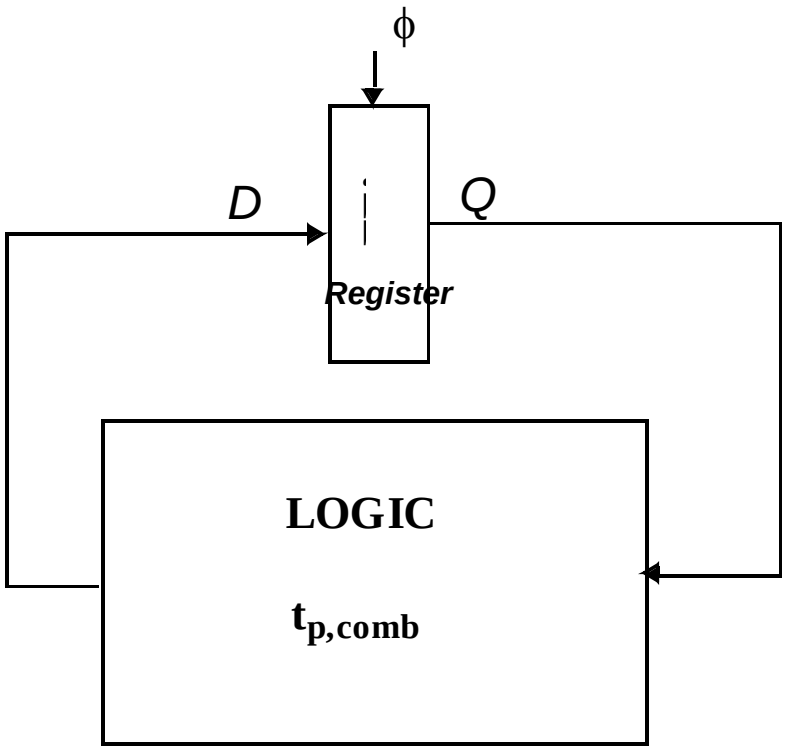


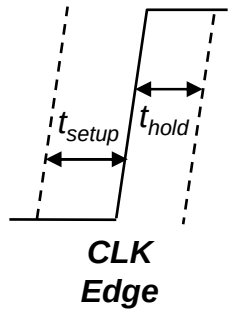
Latch



Requires an extra timing parameter…

Maximum Clock Frequency





To ensure that the input data of the sequential elements is held long enough after the CLK edge and is not modified too soon by the new wave of data coming in:

$$1)\ T_{min} = t_{clk\text{-}Q} + t_{p,comb} + t_{setup}$$

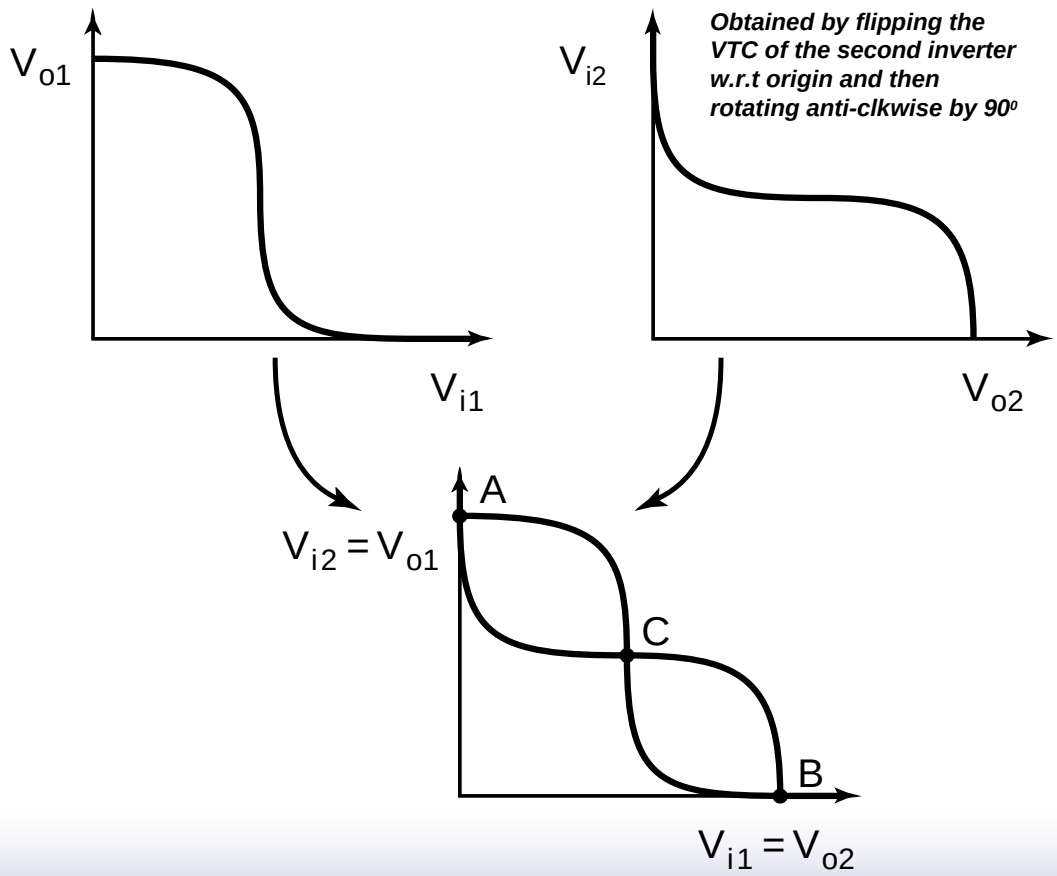
Clk period must accommodate the longest delay of any stage in the network

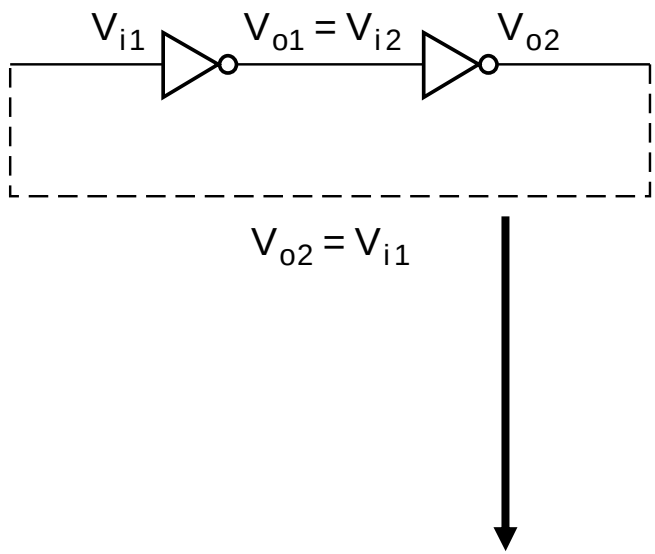
$$2)\ t_{cdreg} + t_{cdlogic} > t_{hold}$$

t_{cd}: contamination delay = minimum delay

Static Latches and Registers

Positive Feedback: Bi-Stability



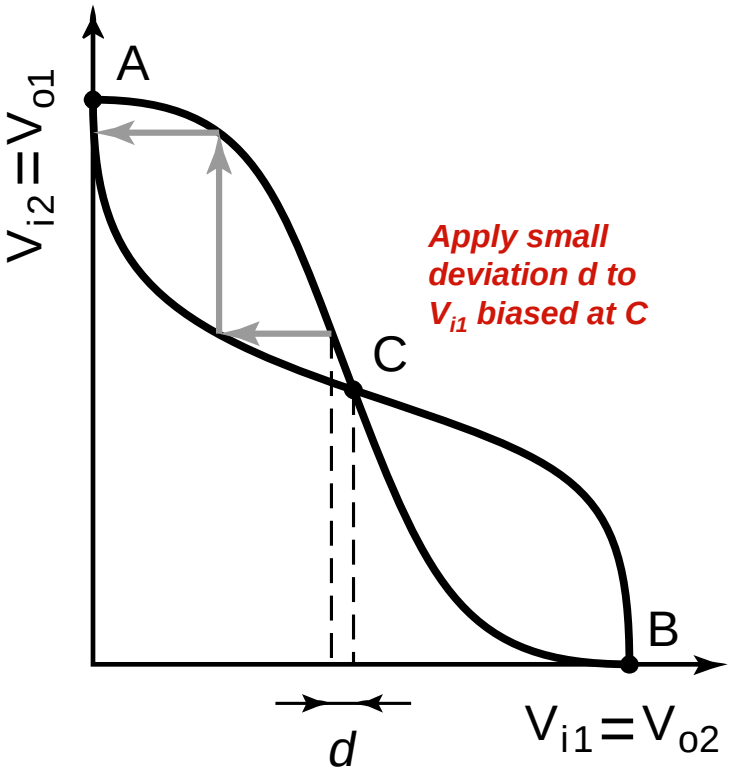


A, B, and C are the three possible operating points

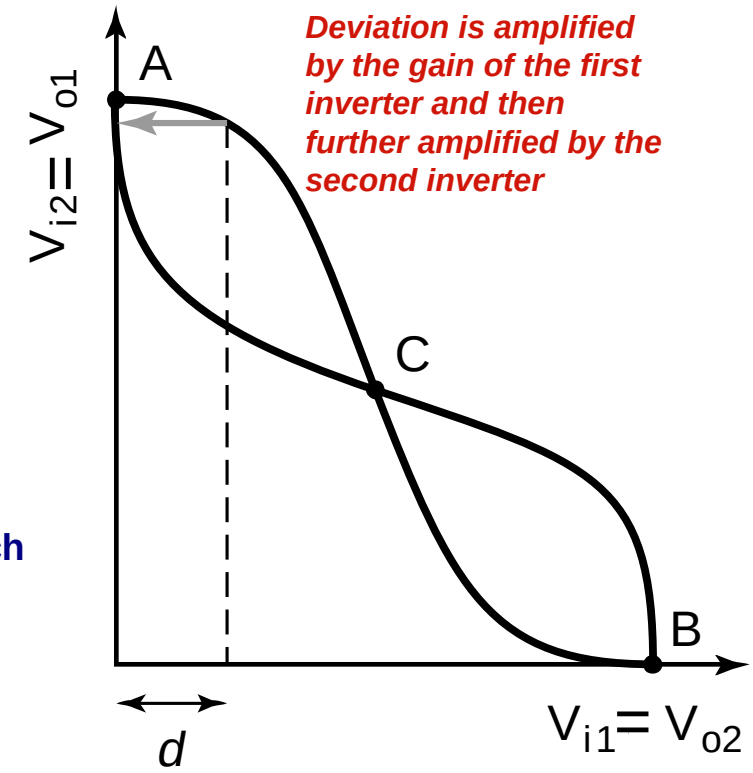
If gain>1 in the transient region: A and B are the only stable operating points, C is a metastable point

Meta-Stability

A: $V_{i1}=0$, $V_{i2}=1$



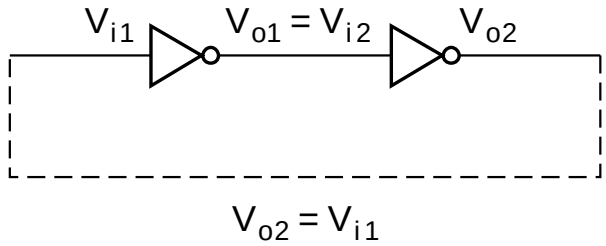
At A and B the loop gain is much smaller than 1



- **Gain is larger than 1 in the transition region**
- **Every small deviation causes the operation point to move away from its original bias point, C ---metastable**

Flip-Flop

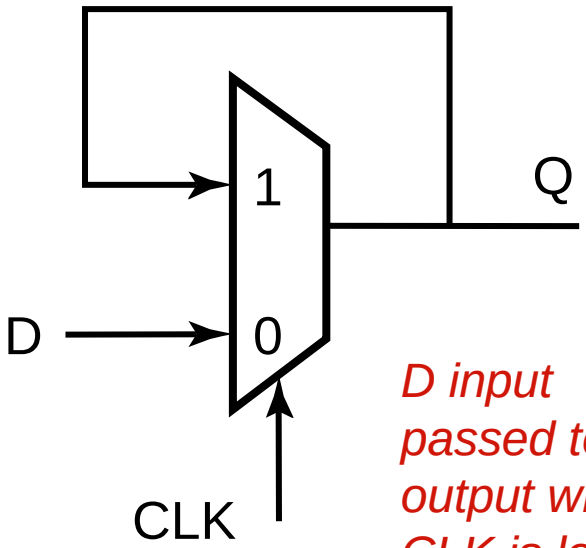
A cross coupled pair of inverters results in a bistable circuit…



- A FF is a bistable circuit, which has 2 stable states
- In the absence of triggering the circuit remains in a single state
- The state can be changed by applying an external trigger
- Two ways to achieve a change of state:
  - Cut the feedback loop: so that a new value can be written into **out** or **Q**
    - **This is MUX based: Q=CLK . Q + CLK . In (most common)**
  - Overpower the feedback loop
    - Apply a trigger signal at the input of the FF and force the new value into the cell by overpowering the stored value
    - Needs careful sizing of transistors in the feedback loop and the trigger circuit
    - Used mostly in static background memories

Mux-Based Latches

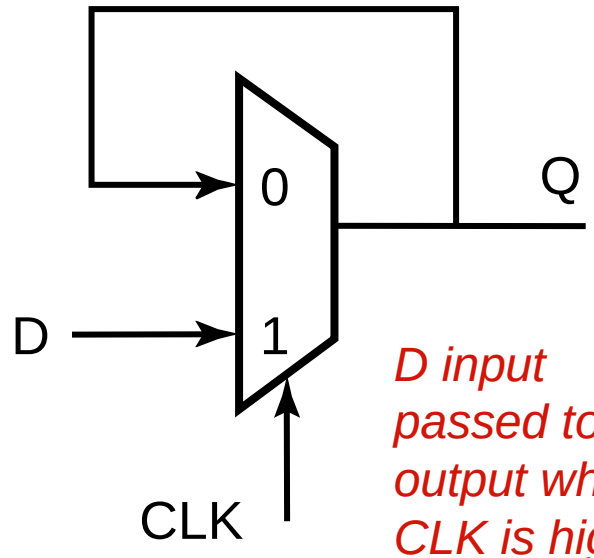
Negative latch (transparent when CLK= 0)



D input passed to output when CLK is low

$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

Positive latch (transparent when CLK= 1)

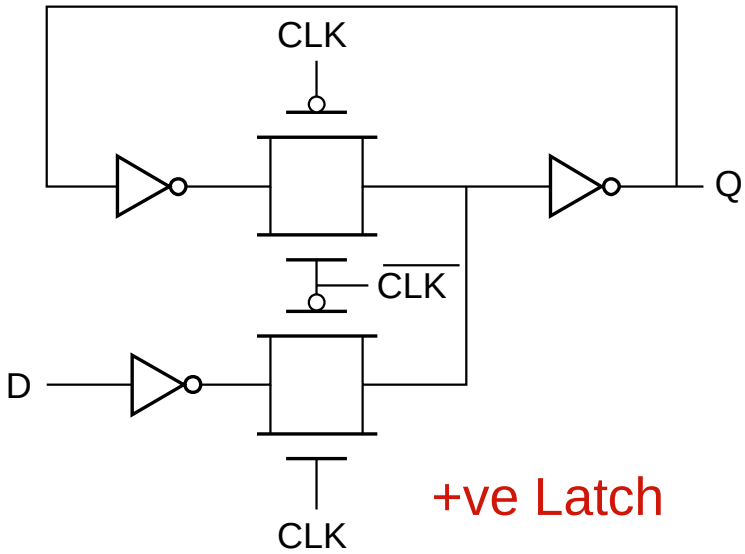


D input passed to output when CLK is high

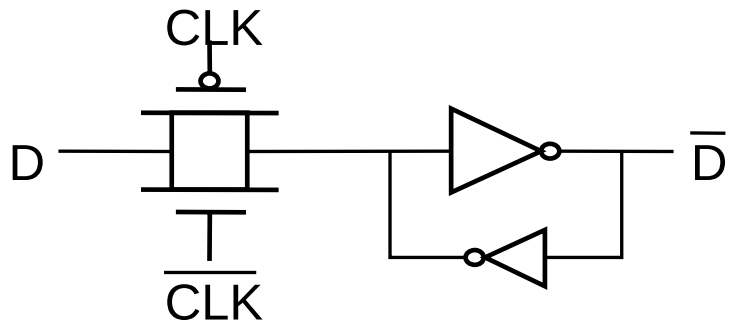
$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

Writing into a Static Latch

Use the clock as a decoupling signal,
that distinguishes between the transparent and opaque states



+ve Latch

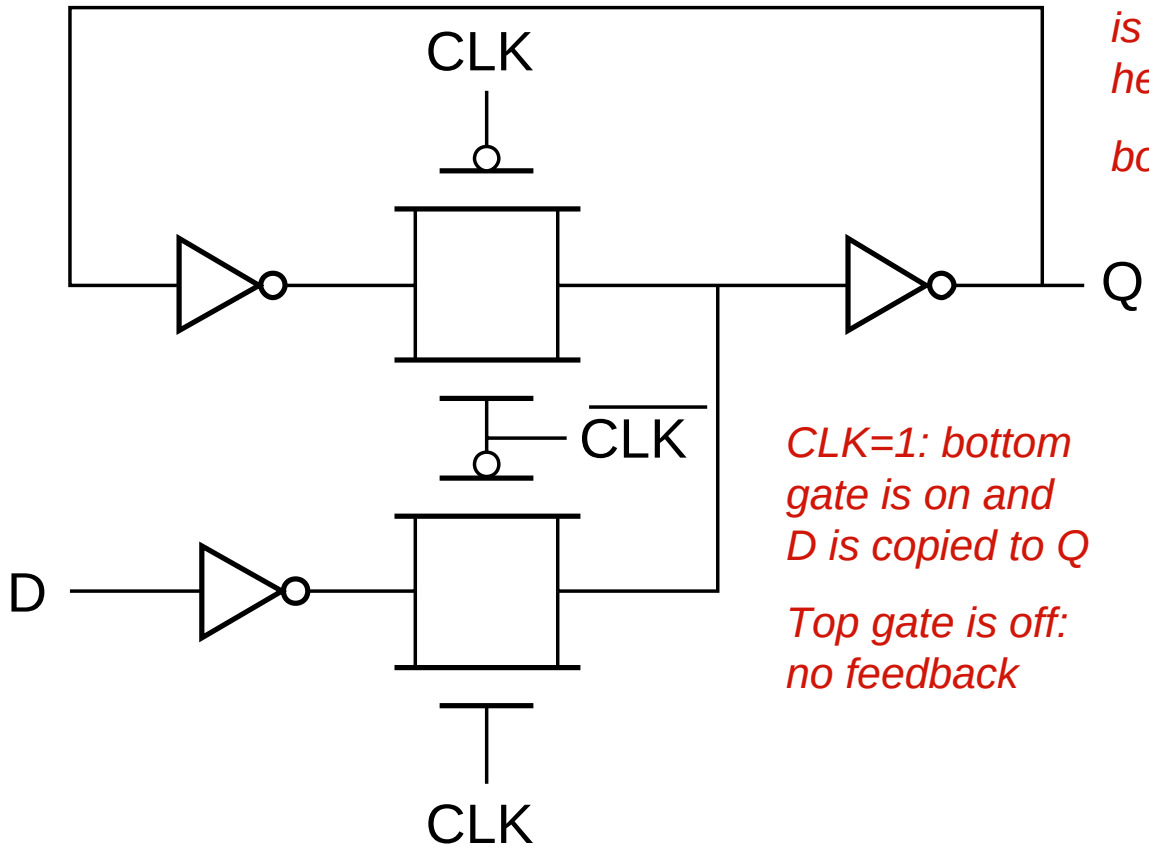


Forcing the state

MUX based (not so efficient..# of transistors driven by CLK is high= 4)

→ (can implement as NMOS-only)

Mux-Based Latch



CLK=0: top gate is on and Q is held stable

bottom gate is off

CLK=1: bottom gate is on and D is copied to Q

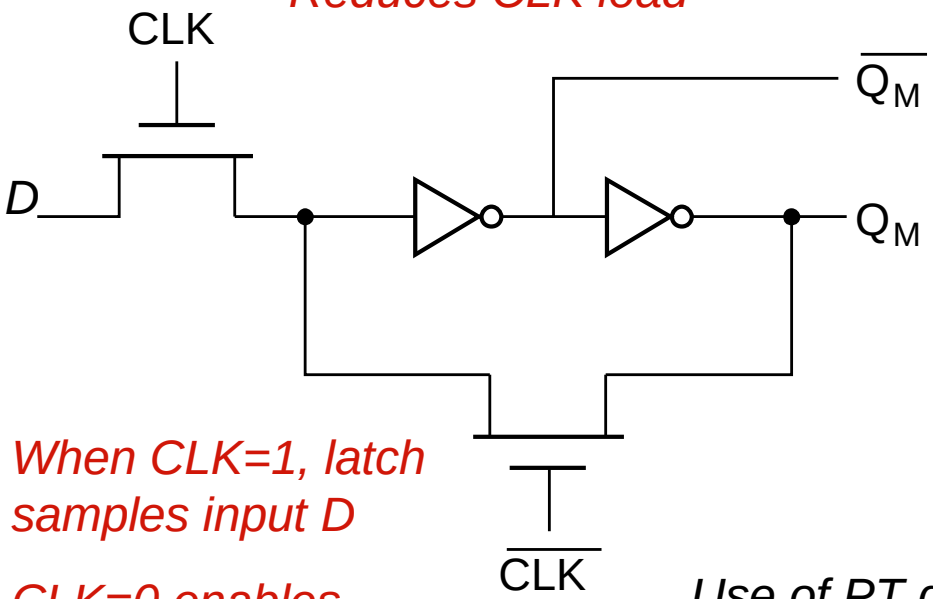
Top gate is off: no feedback

CLK is driving several transistors with activity=1 (not good from power perspective!)

Mux-Based Latch

NMOS only Pass Transistor

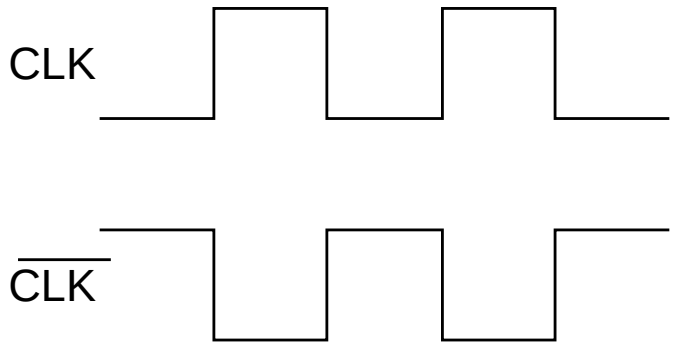
Reduces CLK load



When CLK=1, latch samples input D

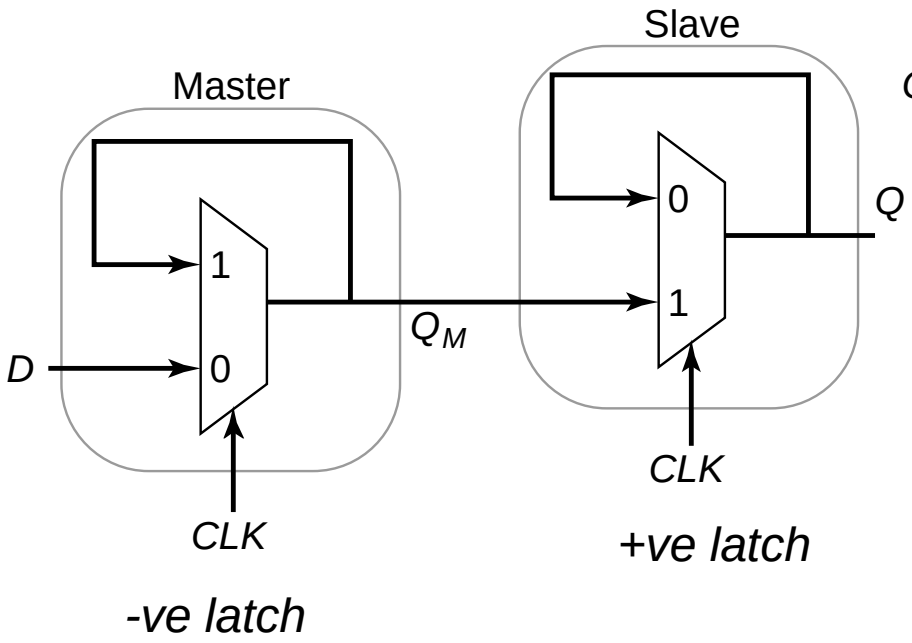
CLK=0 enables feedback loop, puts latch in hold mode

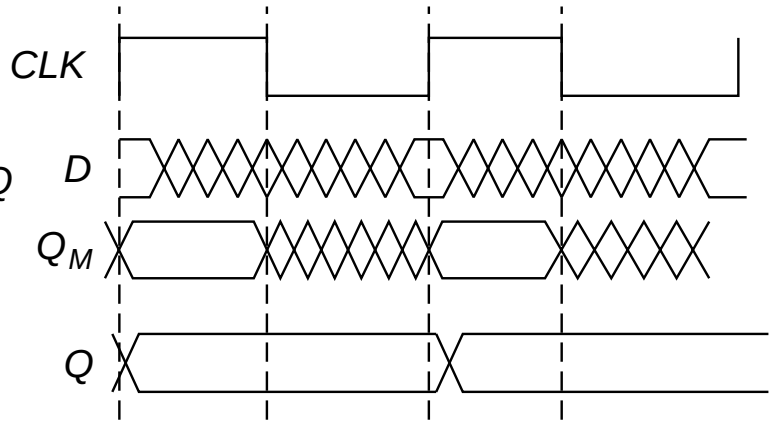
Non-overlapping clocks



Use of PT degrades NM and switching performance by passing V_{dd}-V_{Tn} to the input of first inverter + static power (PMOS of inverter is never fully turned off)

Master-Slave (Edge-Triggered) Register





Two opposite latches trigger on edge
Also called master-slave latch pair

CLK=0: master is transparent and D is copied to QM

During this time slave is in hold mode

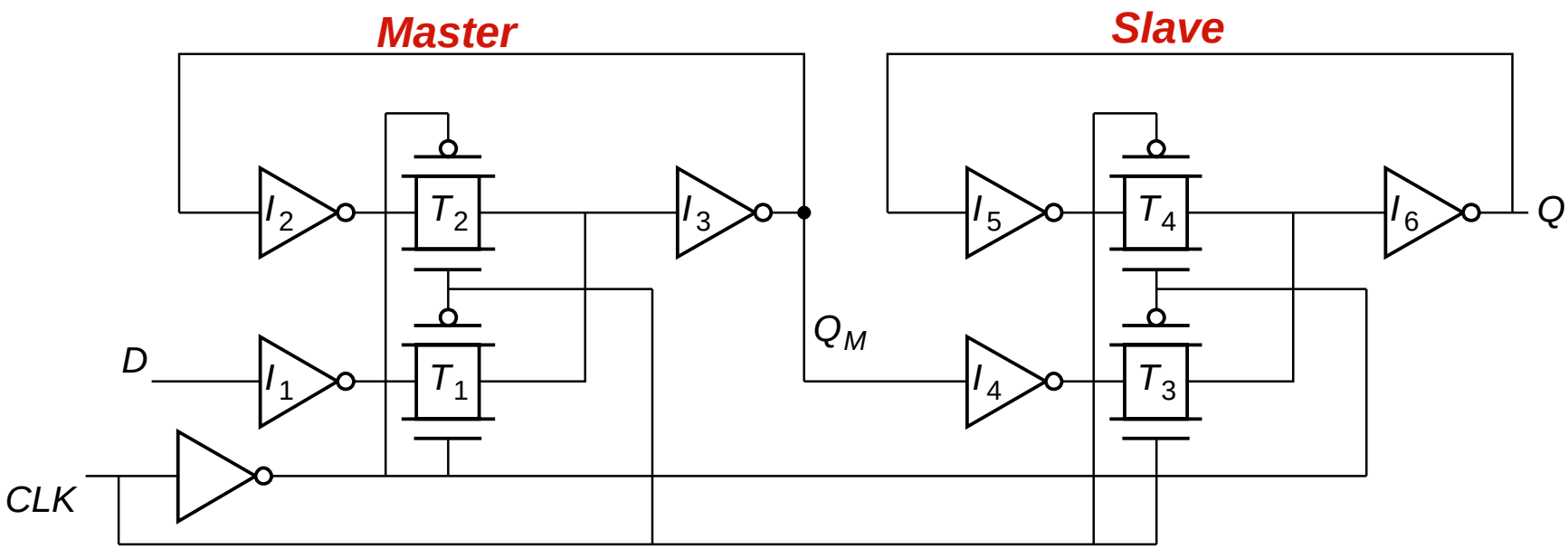
As CLK=1: slave starts sampling, master in hold mode

Value of Q=Value of D right before the rising edge of the CLK: **+ve edge triggered effect**

Master-Slave +ve Edge Triggered Register

Transistor Level Implementation

X-gate Multiplexer-based latch pair



***CLK=0**: T1 is on, T2 is off, D input sampled onto QM*

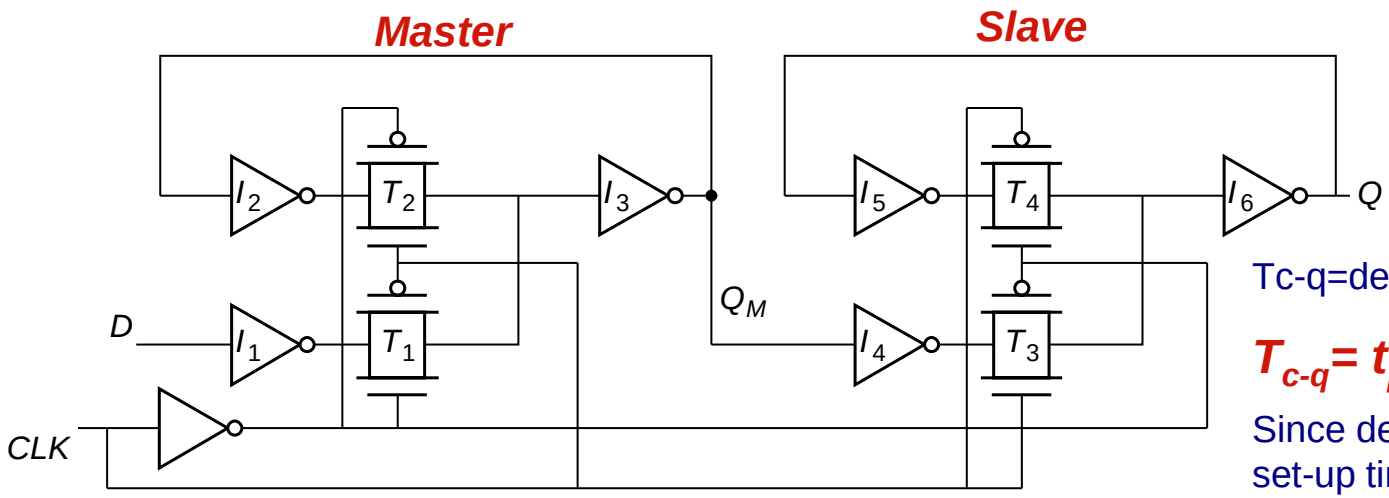
T3 off and T4 on: I5 and I6 hold the state of the Slave

***CLK=1**: T3 is on, T4 is off, QM sampled onto Q*

T2 on and T1 off: I2 and I3 hold the state of QM

Master-Slave +ve Edge Triggered Register

Transistor Level Implementation



Tc-q=delay through T3 and I6=

$T_{c\text{-}q} = t_{pd\_inv} + t_{pd\_tx}$

Since delay of I2 is included in set-up time output of I4 is valid before the rising edge of CLK

tsu=set-up time=time before the rising edge of the CLK during which the D input should remain stable so that QM samples the value reliably

Since D must propagate through I1, T1, I3, and I2 before the rising edge

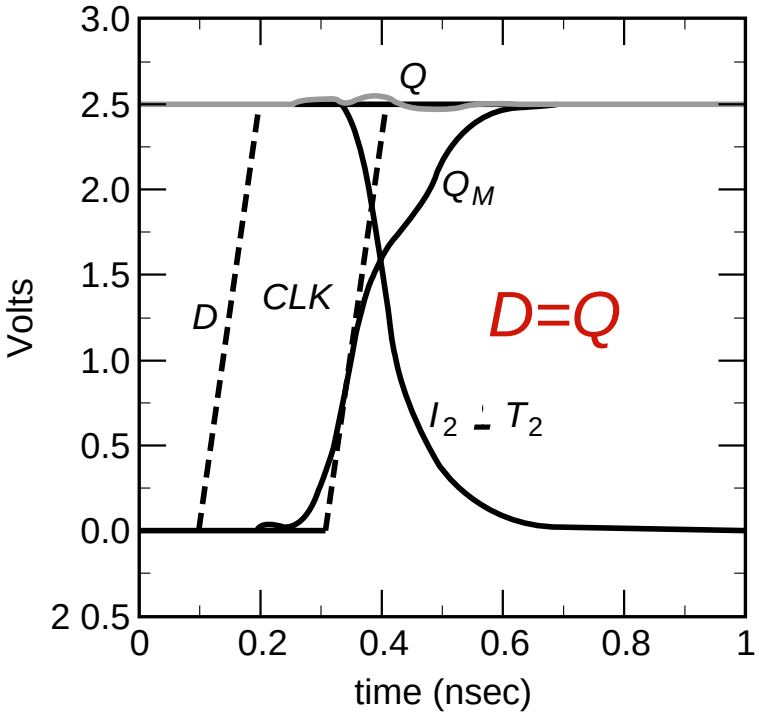
To ensure equal node voltages on both sides of the Xgate

$t_{su} = 3t_{pd\_inv} + t_{pd\_tx}$

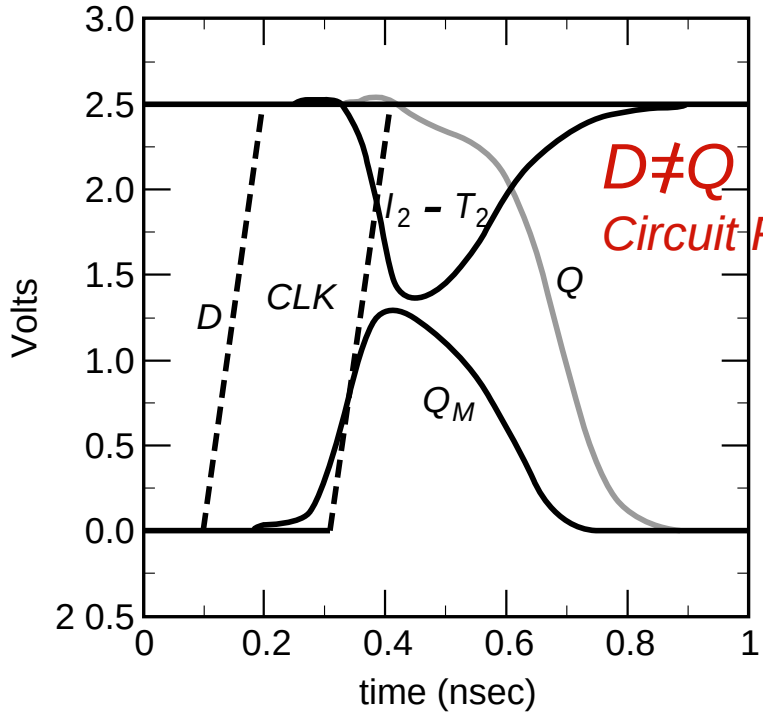
$t_{hold} = 0$ (since T1 is cut off after CLK edge)

Timing Analysis: Setup Time

SPICE Simulations: progressively skew the input w.r.t CLK edge until the circuit fails



(a) T_{setup} = 0.21 nsec



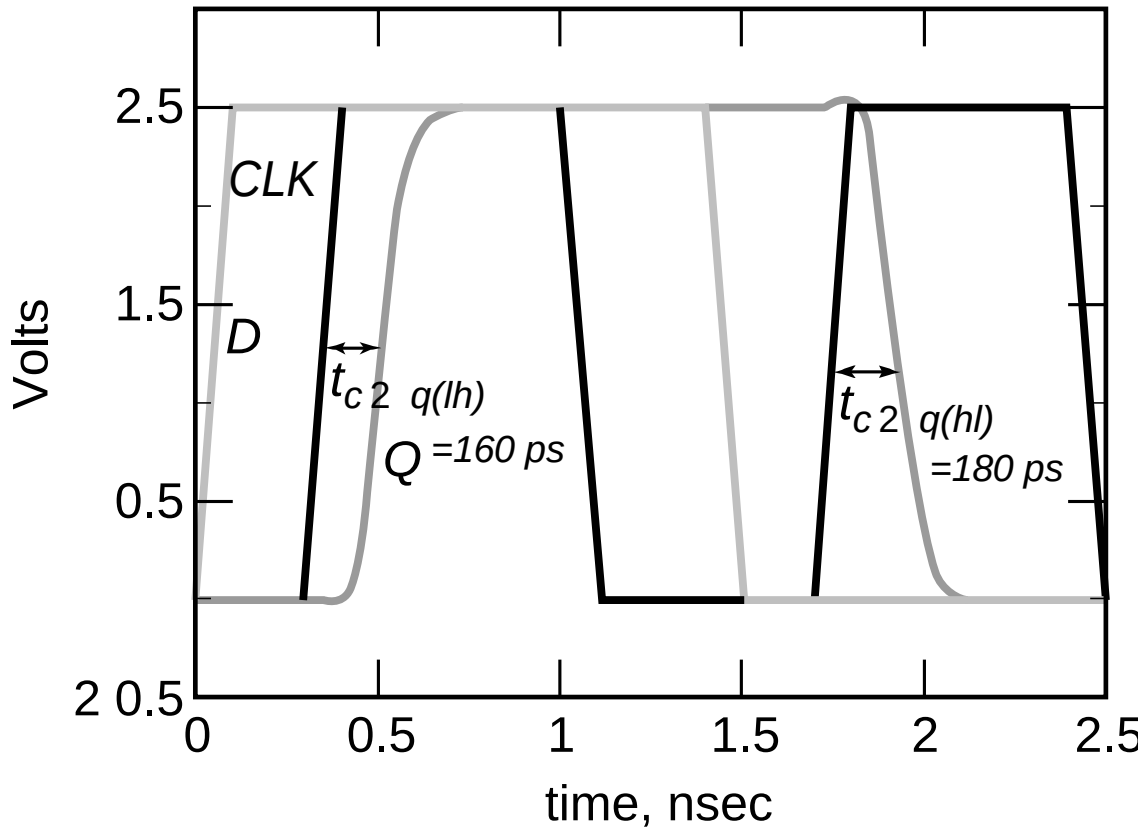
(b) T_{setup} = 0.20 nsec

CLK is enabled before the voltage across T2 settles to the same value

Set-up time for this circuit = 210 ps and hold time =0

Clk-Q Delay

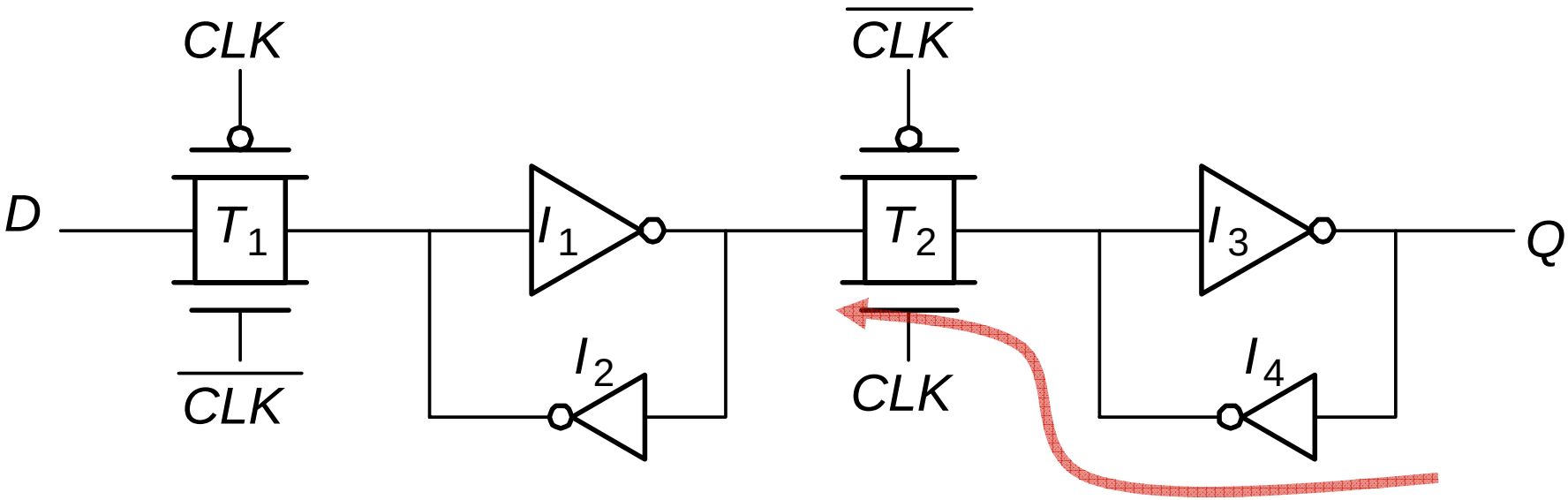
$t_{c\text{-}q}$ = 50% point of CLK to 50% point of Q



Reduced Clock Load Master-Slave Register

Ratioed circuit: provides reduced load at the cost of NM

Note: X-gate register presents high capacitive load to the CLK signal

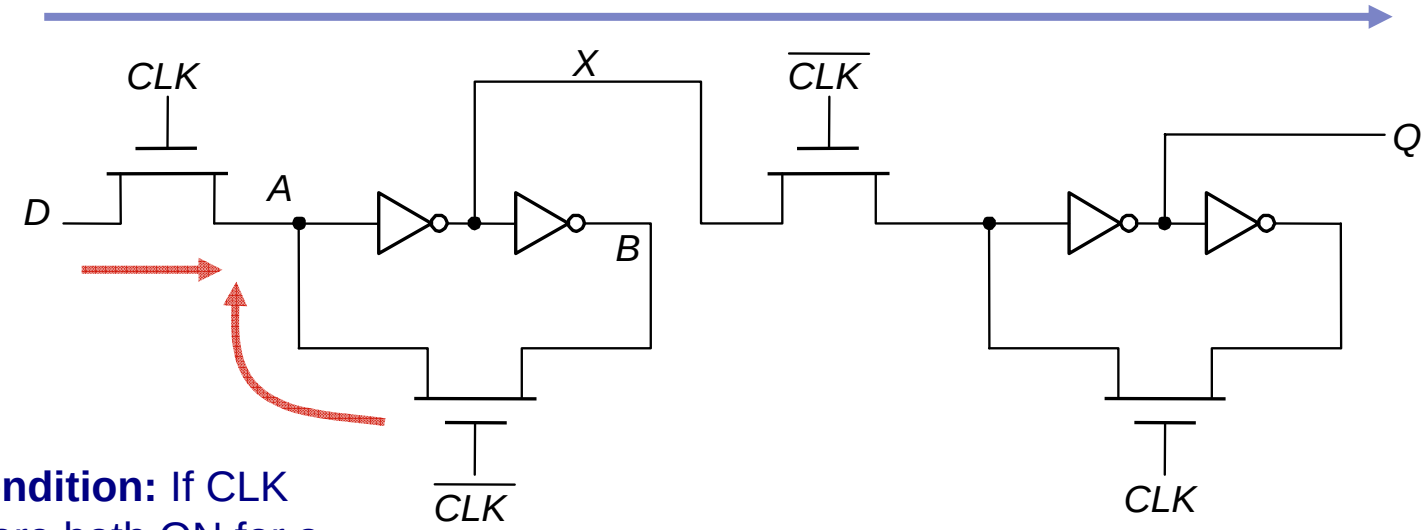


Cons: *1) I1 must overpower I2 to switch the state of the cross-coupled inverter*

2) Reverse conduction-second stage can affect the state of the first latch (I1-I2)

I4 must be a weak gate….

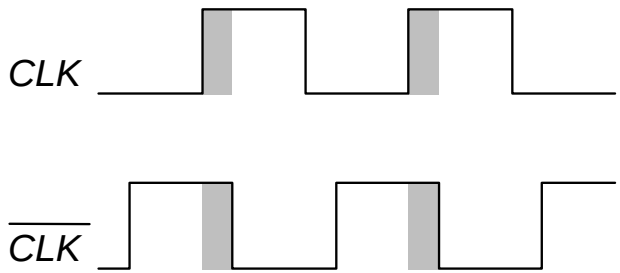
Avoiding Clock Overlap



(a) Schematic diagram of an NMOS only –ve M-S register

RACE Condition: If CLK and $\overline{CLK}$ are both ON for a short time, both sampling pass transistors are ON providing a direct path from D to Q. Hence, data at the output can change at the rising CLK edge

Also node A can be driven by both D and B: undefined state



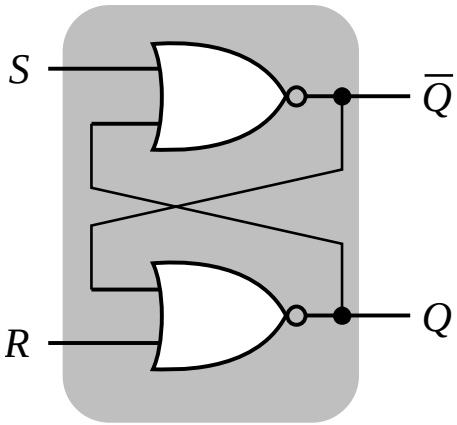
(b) Overlapping clock pairs

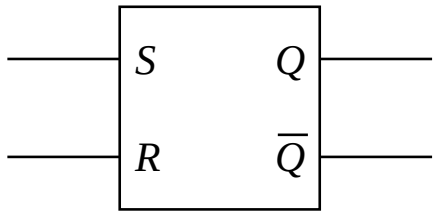
Clock skew is a problem!

One Solution: use non-overlapping CLKs

Overpowering the Feedback Loop — Cross-Coupled Pairs

NOR-based set-reset





S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

Forbidden State

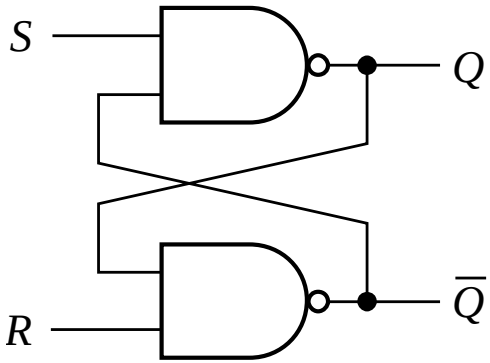
Use external triggers, S and R to change state:

S=1 forces Q=1,

R=1 forces Q=0

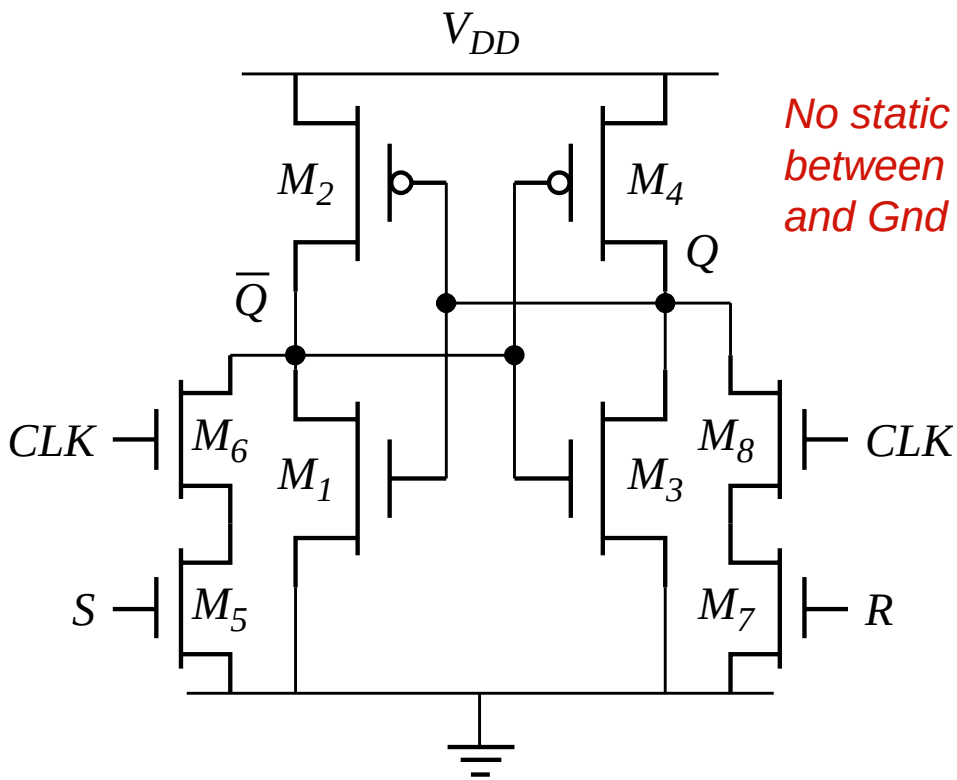
Cross-Coupled NAND

Cross-coupled NANDs



This is not used in datapaths any more, but is a basic building memory cell

Added clock



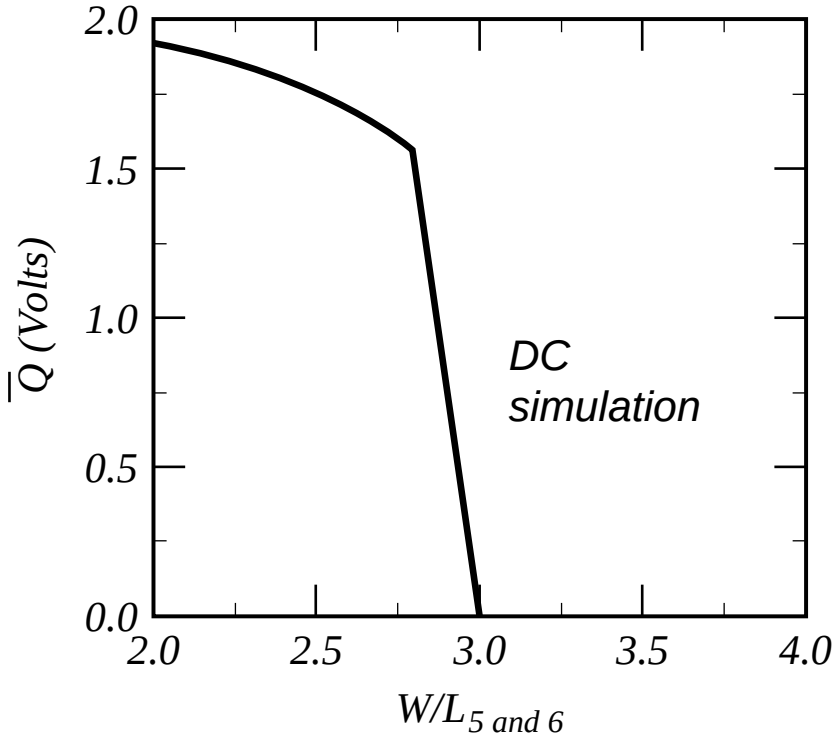
No static path between Vdd and Gnd

Transistor sizing is essential to ensure FF transition:

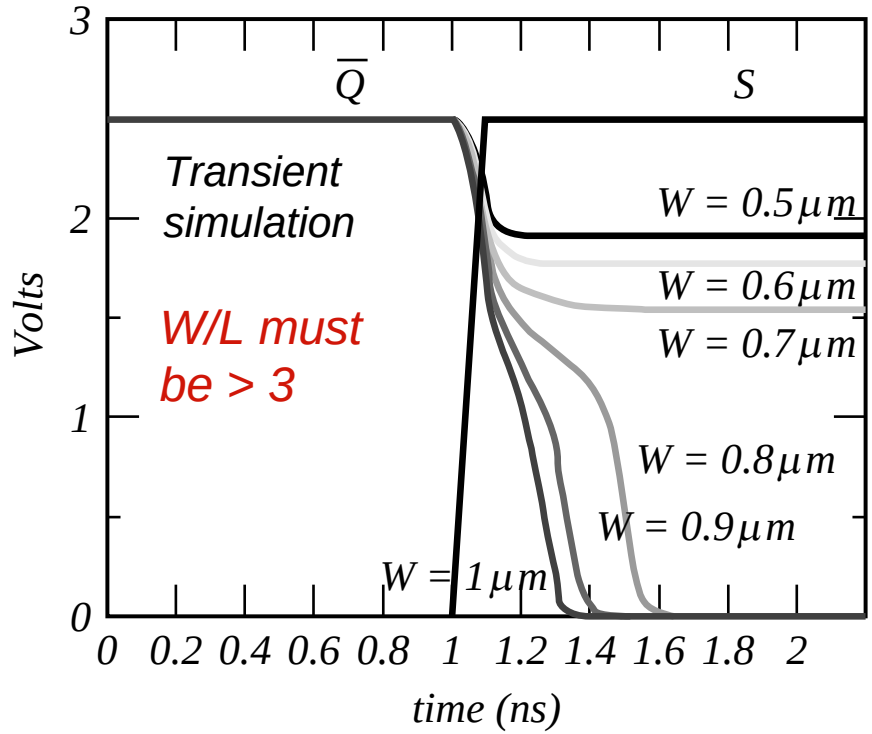
If Q is high and R=1, then VQ must be < VM of INV M1-M2. Similar condition is needed to switch INV M3-M4 for S=1. This means we must increase the sizes of M5, M6, M7 and M8. M4-M7-M8 (and M5-M6-M2) form ratioed inverters.

Sizing Issues

0.25um process



(a)



(b)

Output voltage dependence on transistor width

Transient response