ECE 225
High-Speed Digital IC Design

Lecture 4

Prof. Kaustav Banerjee
Electrical and Computer Engineering
E-mail: kaustav@ece.ucsb.edu

MOS Transistor as a Switch

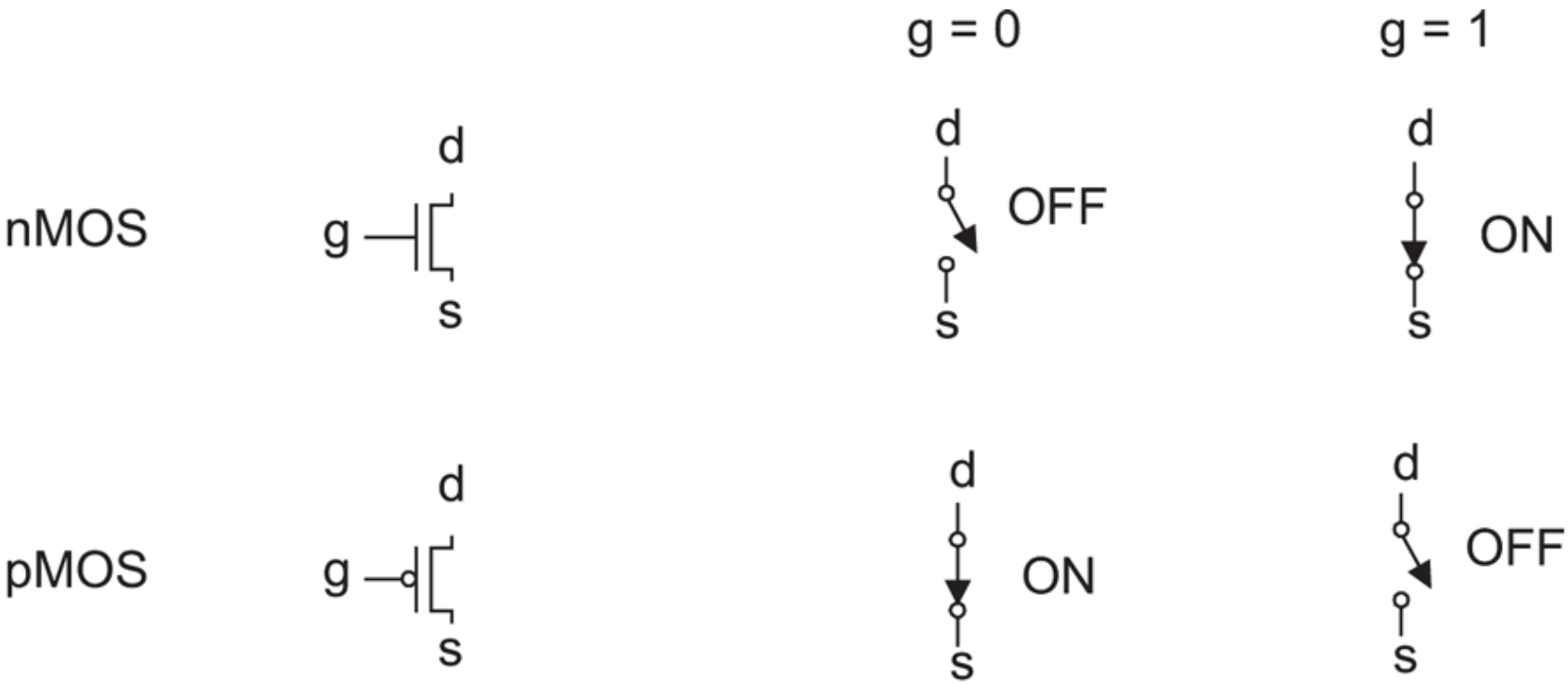


FIG 1.9 Transistor symbols and switch-level models

Inverter (NOT Gate)

Table 1.1 Inverter truth table

A	Y
0	1
1	0

Transistor Level Implementation

CMOS: Complementary MOS

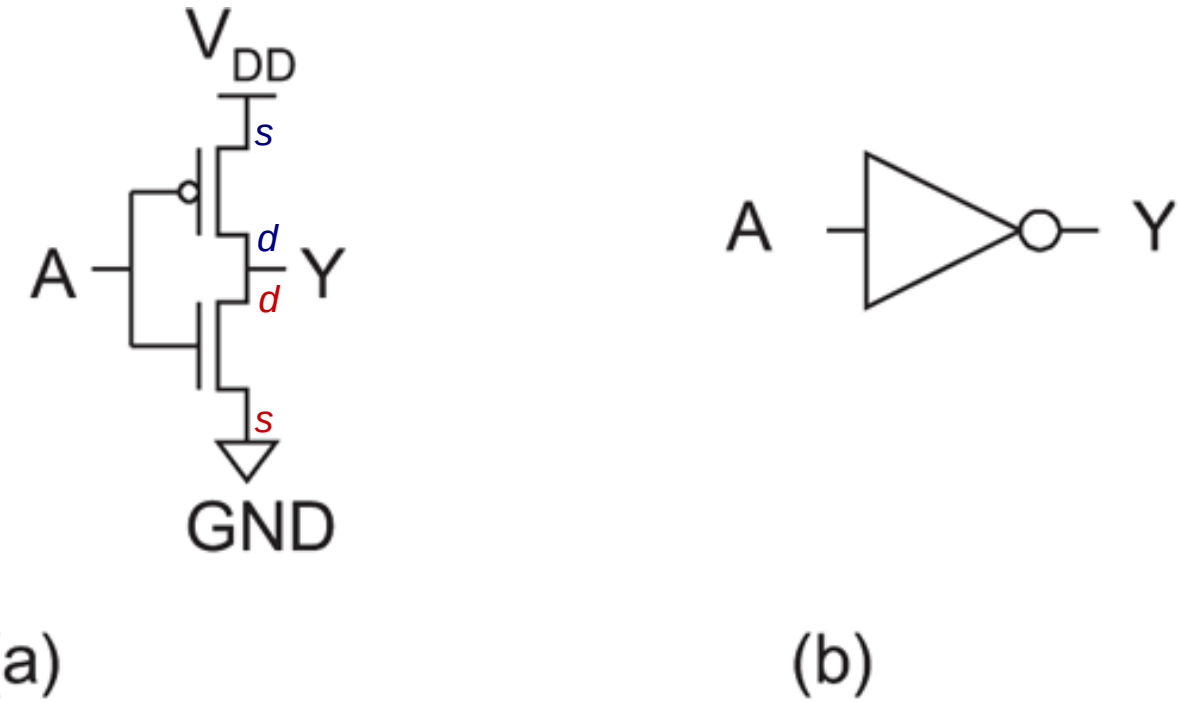
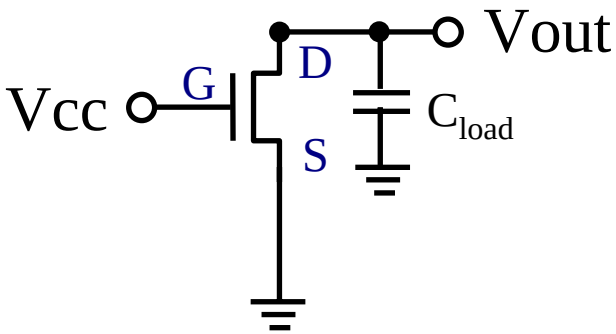


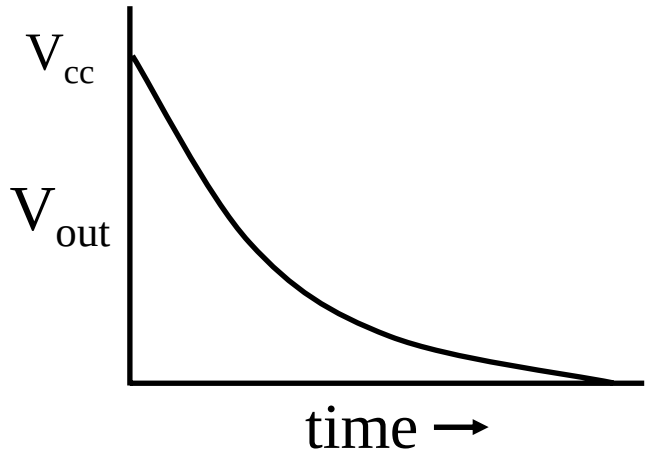
FIG 1.10 Inverter schematic (a) and symbol (b) $Y = \overline{A}$

MOS voltage levels

Case 1: NMOS discharges capacitor

- Initially: Vout = Vcc (capacitor fully charged)
- V_{GS} of NMOS = Vcc
- What is final Vout?



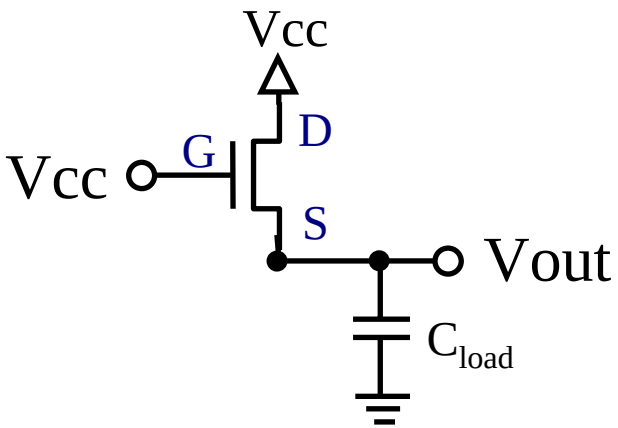


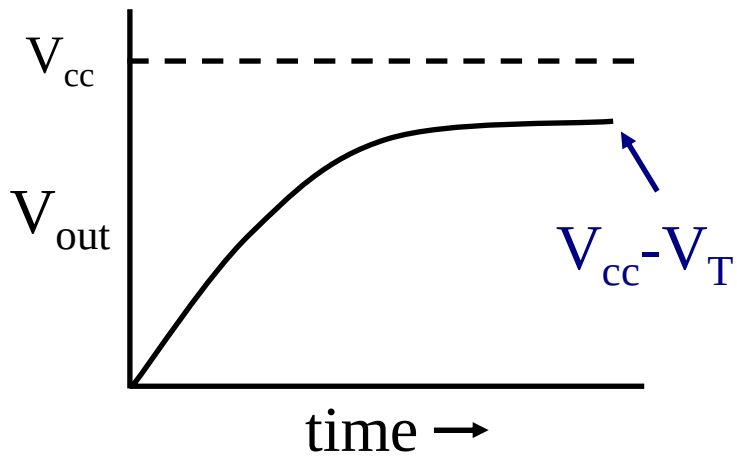
- NMOS remains on since $V_{GS} > V_T$
- Final output voltage V_{out} = 0V

MOS voltage levels

Case 2: NMOS charges capacitor

- Initially: Vout = 0
- Initial V_{GS} of NMOS = Vcc
- What is final Vout?



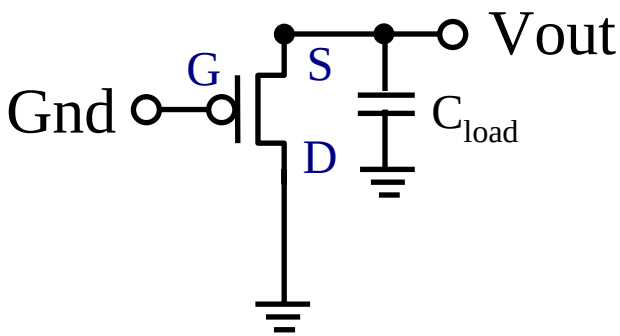


- NMOS remains on until $V_{GS} = V_T$
- Final output voltage $V_{out} = V_{cc} - V_T$

MOS voltage levels

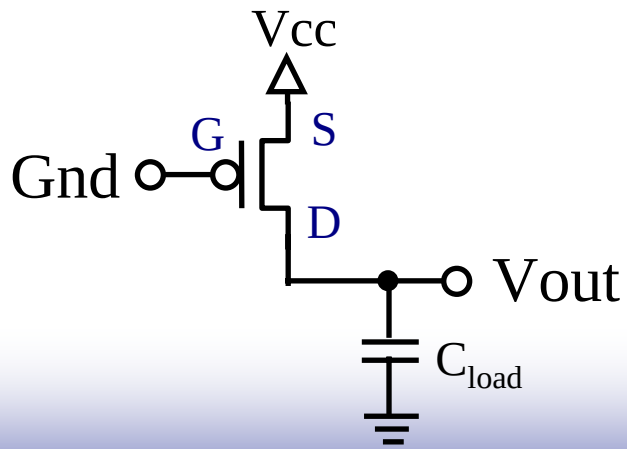
Repeat for PMOS:

- Case 1: PMOS discharging capacitor



- PMOS on until $V_{GS} = V_T$
- Vout = $|V_T|$

- Case 2: PMOS charging capacitor



- PMOS always on ($V_{GS} = -V_{CC}$)
- Vout = V_{CC}

MOS voltage levels

- NMOS summary
  - Transfers logic ‘0’ completely (good for discharging a node)
  - Does not transfer logic ‘1’ completely (bad for charging a node)
- PMOS summary
  - Transfers logic ‘1’ completely
  - Does not transfer logic ‘0’ completely
- Result:
  - NMOS used for pull-down, PMOS for pull-up

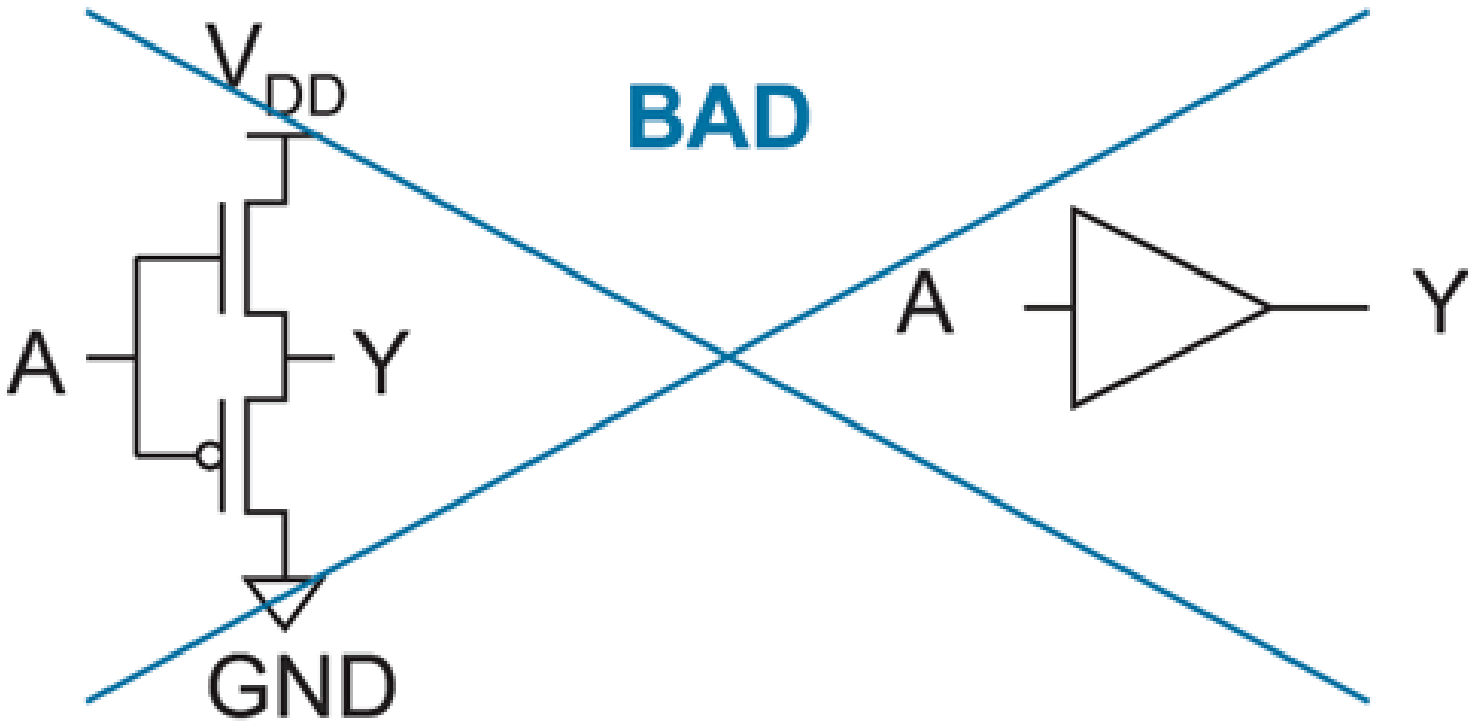


FIG 1.21 Bad noninverting buffer

CMOS Inverter

The most widely used gate….

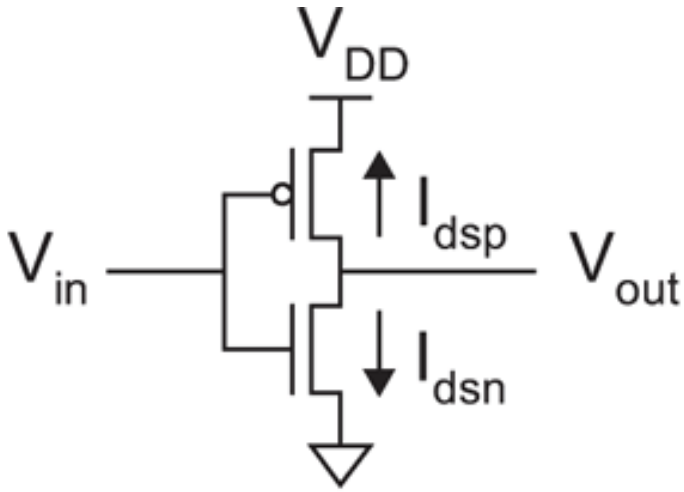
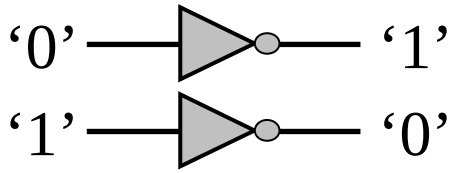


FIG 2.23 A CMOS inverter

Inverter Operation

- Inverter is simplest digital logic gate

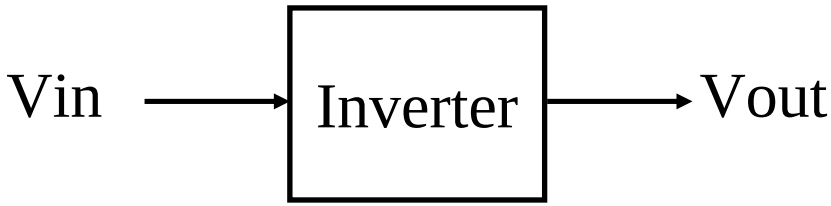


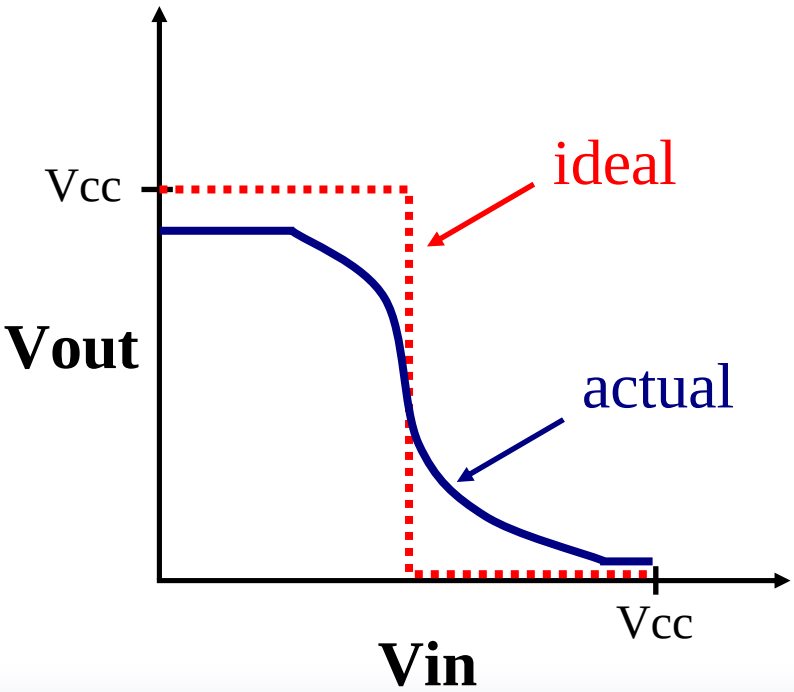
In	Out
0	1
1	0

- Many different circuit styles possible
  - Resistive-load
  - Pseudo-NMOS
  - CMOS
- Important characteristics
  - Speed (delay through the gate)
  - Power consumption
  - Robustness (tolerance to noise)
  - Area and process cost

Inverter model: VTC

Voltage transfer curve (VTC): plot of output voltage Vout vs. input voltage Vin

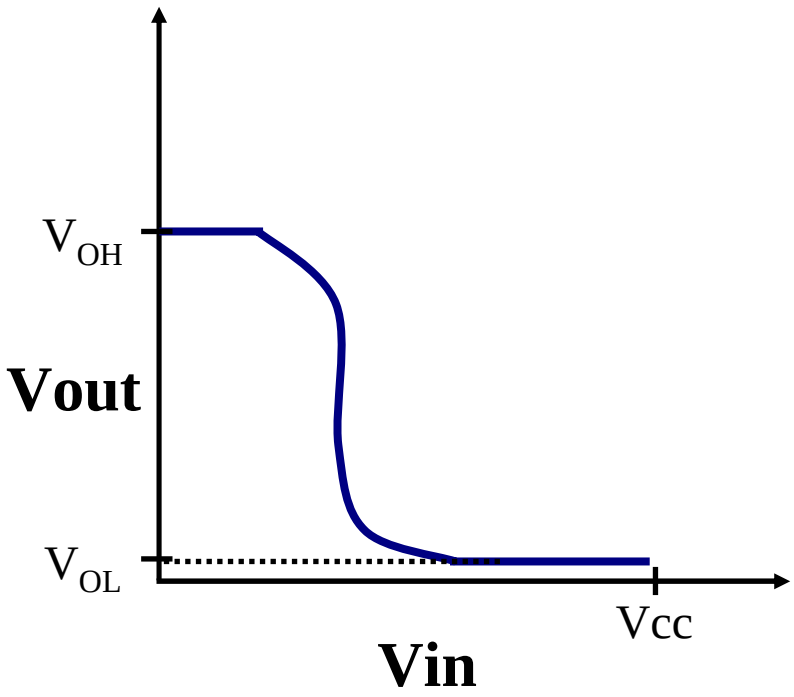




Ideal digital inverter:

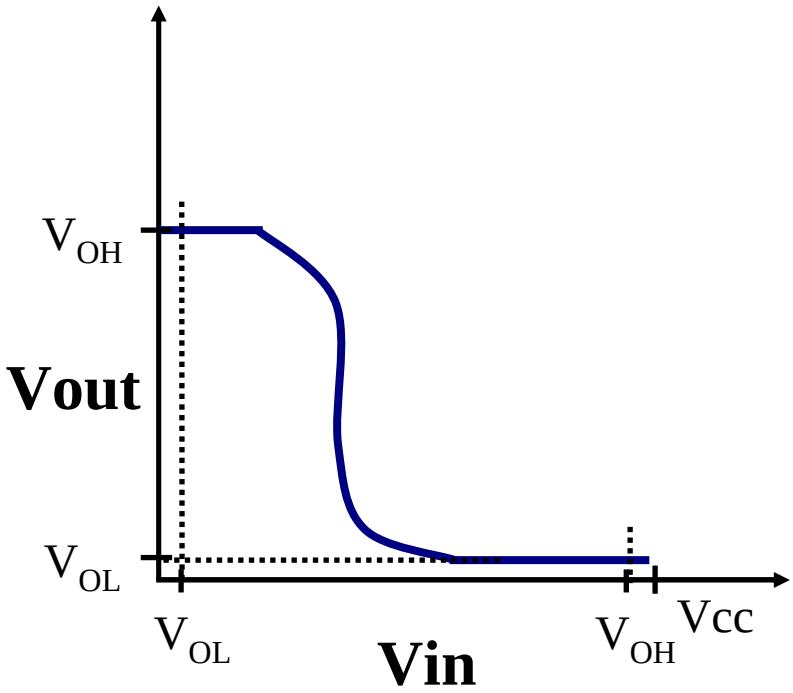
- When Vin=0, Vout=Vcc
- When Vin=Vcc, Vout=0
- Sharp transition region

Actual inverter: V_{OH} and V_{OL}



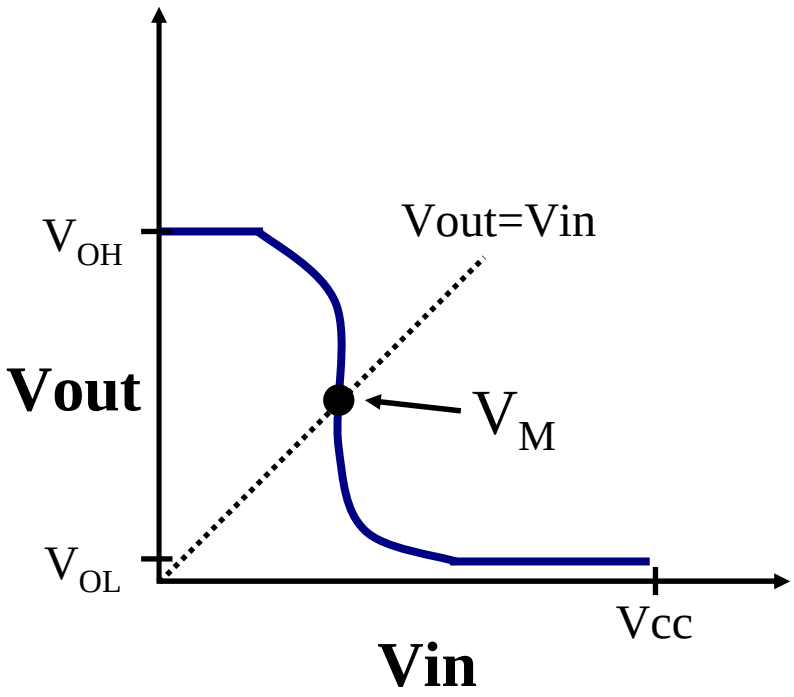
- V_{OH} and V_{OL} represent the "high" and "low" output voltages of the inverter
- V_{OH} = output voltage when Vin = '0'
- V_{OL} = output voltage when Vin = '1'
- Ideally,
  - V_{OH} = Vcc
  - V_{OL} = 0

VOL and VOH



- In transfer function terms:
  - $V_{OL} = f(V_{OH})$
  - $V_{OH} = f(V_{OL})$
  - f = inverter transfer function
- Difference (V_{OH}-V_{OL}) is the *voltage swing* of the gate
  - *Full-swing logic* swings from ground to Vcc

Inverter Threshold



Inverter switching threshold:

- Point where voltage transfer curve intersects line Vout=Vin
- Represents the point at which the inverter switches state
- Normally, $V_M \approx Vcc/2$

CMOS Inverter Noise Margins

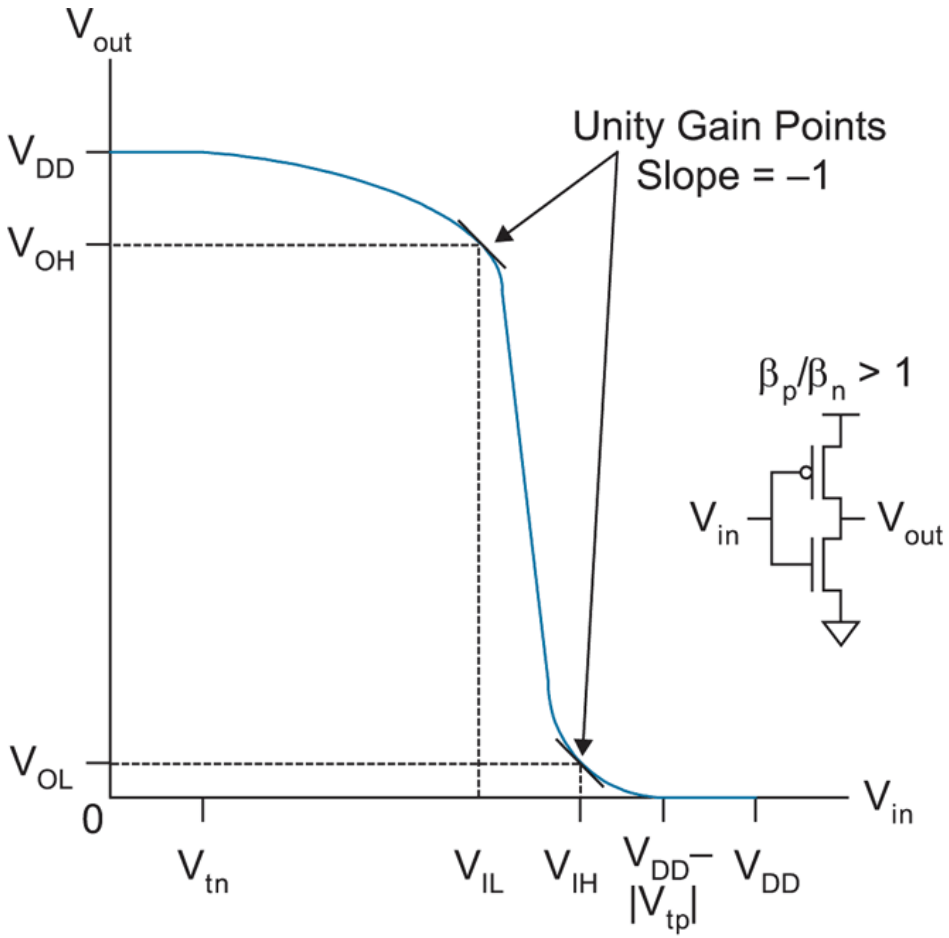
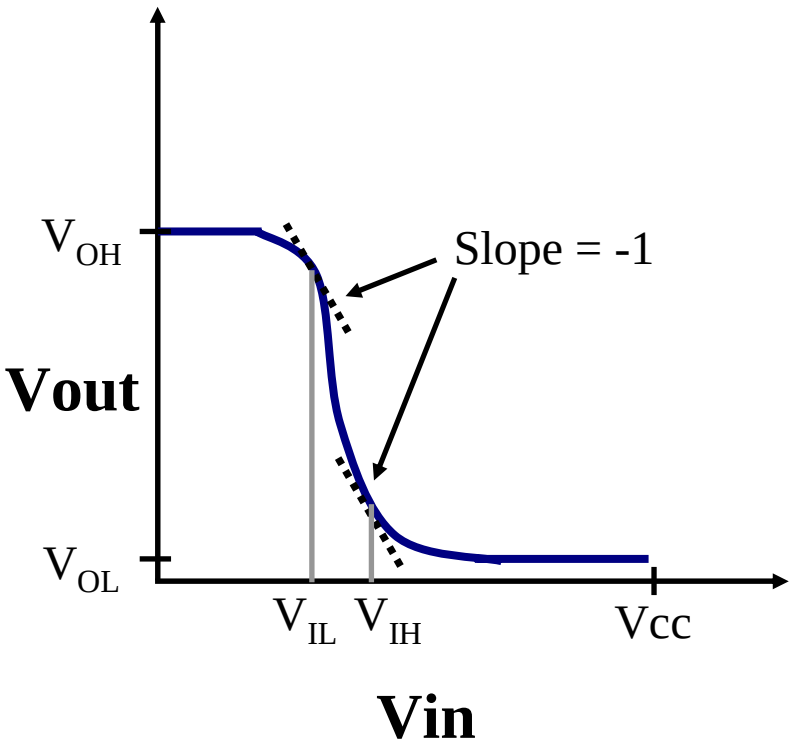


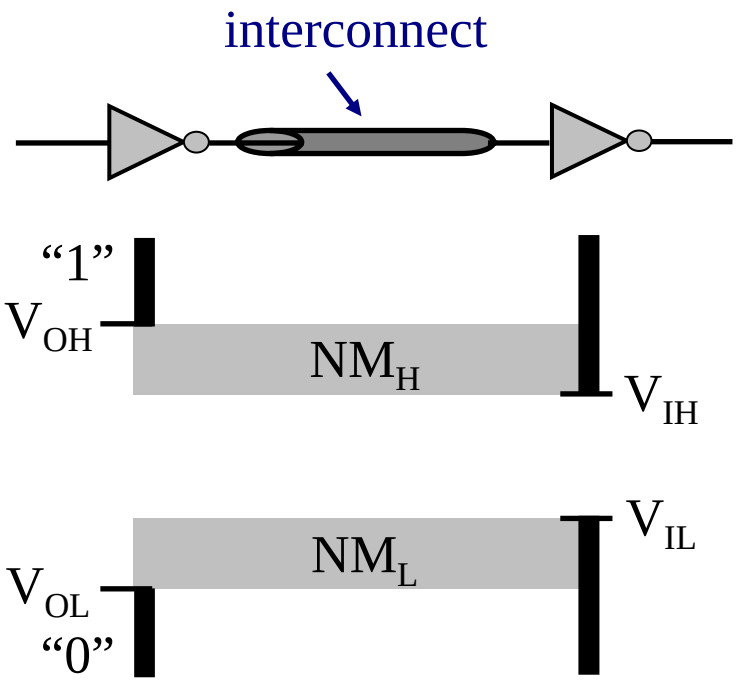
FIG 2.28 CMOS inverter noise margins

Noise Margins



- V_{IL} and V_{IH} measure effect of input voltage on inverter output
- V_{IL} = largest input voltage recognized as logic ‘0’
- V_{IH} = smallest input voltage recognized as logic ‘1’
- Defined as point on VTC where slope = -1

Noise Margin (cont)



Ideally, noise margin should be as large as possible

- Noise margin is a measure of the *robustness* of an inverter
  - $N_{ML} = V_{IL} - V_{OL}$
  - $N_{MH} = V_{OH} - V_{IH}$
- Models a chain of inverters. Example:
  - First inverter output is V_{OH}
  - Second inverter recognizes input $> V_{IH}$ as logic '1'
  - Difference V_{OH}-V_{IH} is "safety zone" for noise

Noise Margin (cont)

- Why are V_{IL}, V_{IH} defined as unity-gain point on VTC curve?
  - Assume there is noise on input voltage V_{in}

$$V_{out} = f\left(V_{in} + V_{noise}\right)$$

  - First-order approximation (Taylor Series):

$$V_{out} = f\left(V_{in}\right) + \frac{dV_{out}}{dV_{in}} V_{noise}$$

  - If gain (dV_{out}/dV_{in}) > 1, noise will be amplified.
  - If gain < 1, noise is filtered. Therefore V_{IL}, V_{IH} ensure that gain < 1

Noise Margin (summary)

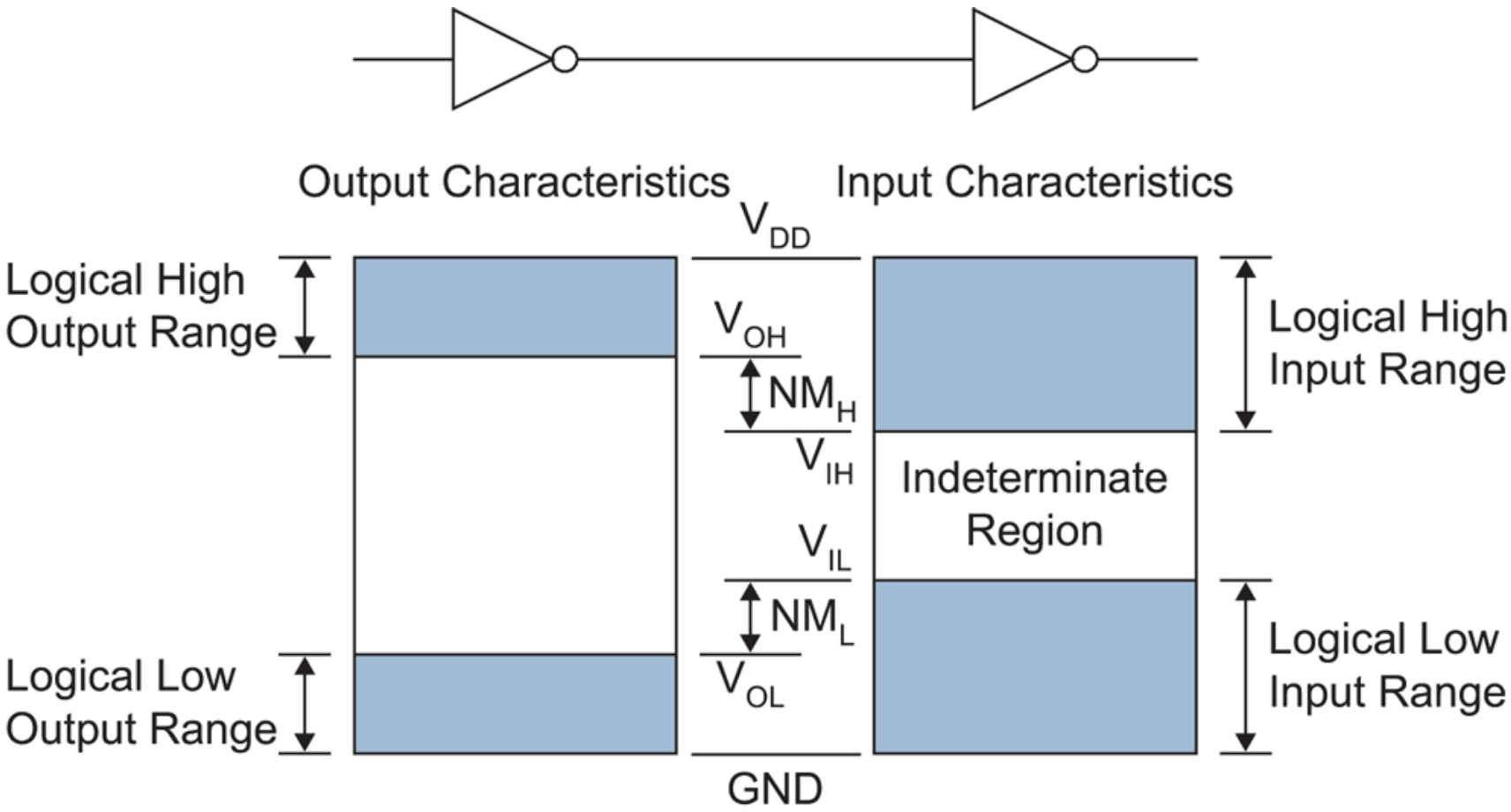
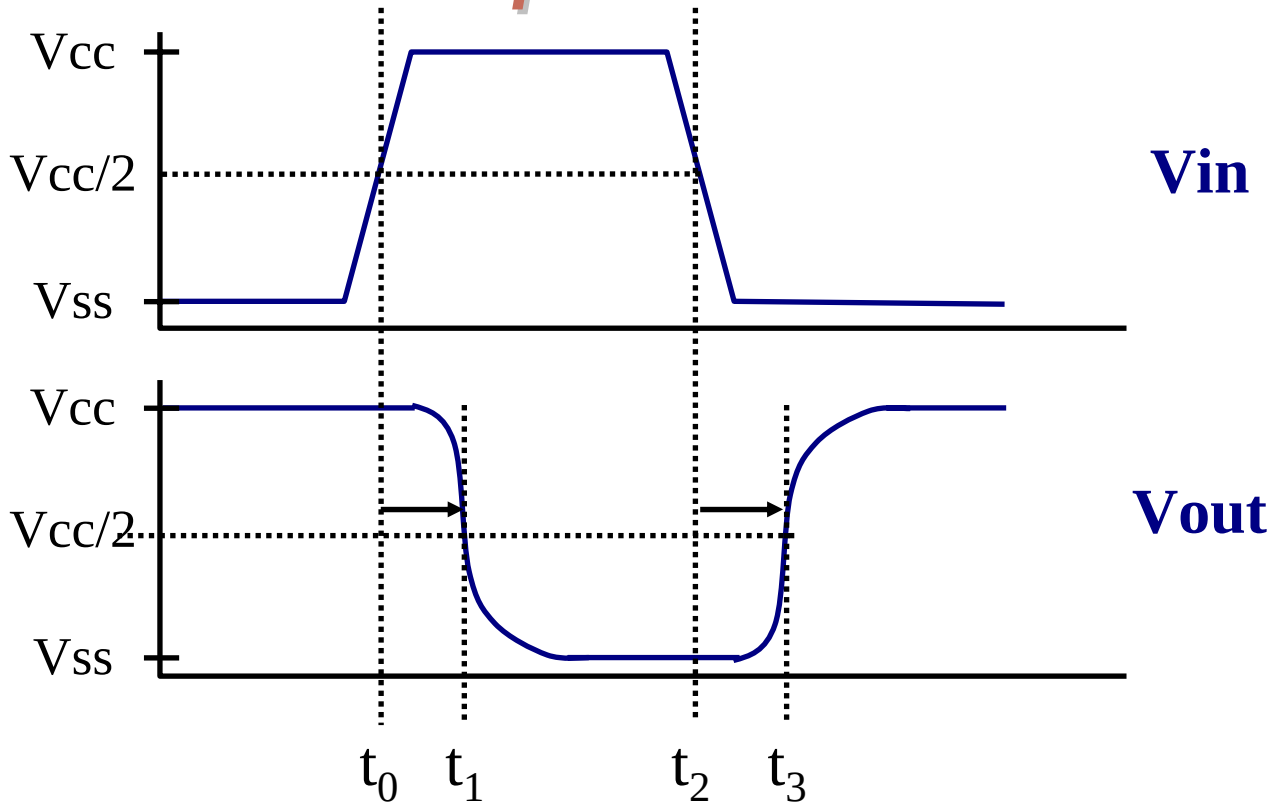


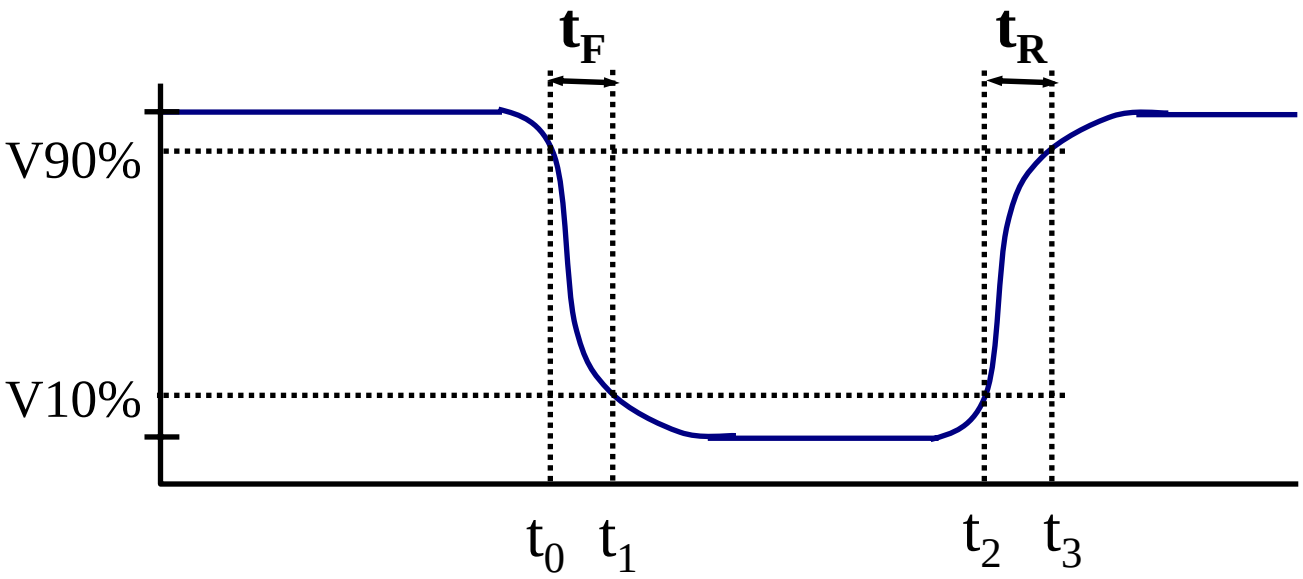
FIG 2.27 Noise margin definitions

Inverter Time Response



- Propagation delay measured from 50% point of Vin to 50% point of Vout
- $t_{phl} = t_1 - t_0$, $t_{plh} = t_3 - t_2$, $t_p = \frac{1}{2}(t_{phl}+t_{plh})$

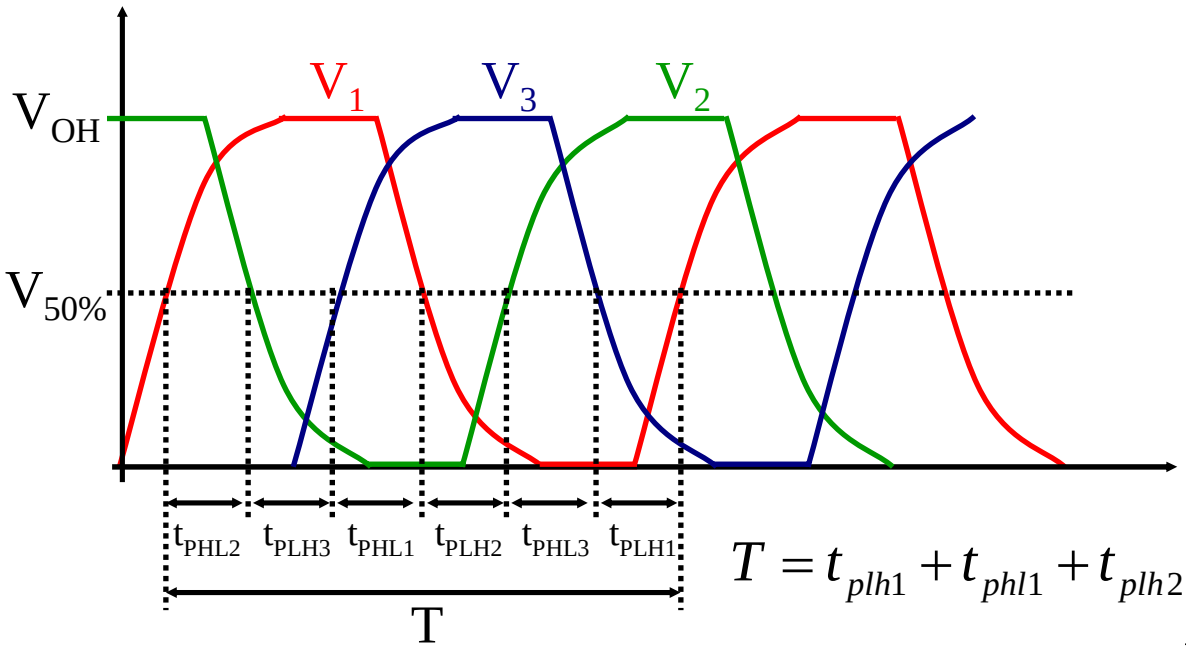
Rise and Fall Time

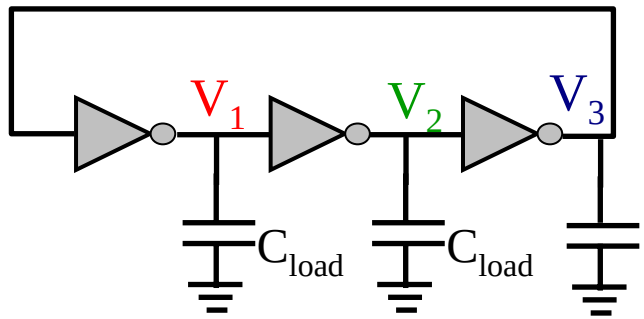


- Fall time: measured from 90% point to 10% point
  - $t_F = t_1 - t_0$
- Rise time: measured from 10% point to 90% point
  - $t_R = t_3 - t_2$
- Alternately, can define 20%-80% rise/fall time

Ring Oscillator

- *Ring oscillator circuit*: standard method of comparing delay from one process to another
- Odd-number n of inverters connected in chain: oscillates with period T (usually n >> 5)





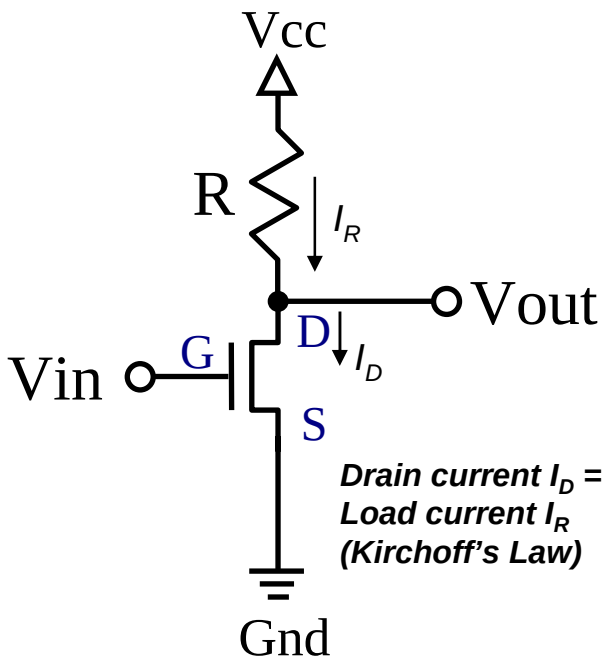
$$T = t_{plh1} + t_{phl1} + t_{plh2} + t_{phl2} + t_{plh3} + t_{phl3} + \cdots$$

$$T = 2nt_p, \qquad f = \frac{1}{T} = \frac{1}{2nt_p}, \qquad t_p = \frac{1}{2nf}$$

Resistive-load Inverter

- Requires only NMOS transistor and resistor
- When Vin = 0:
  - NMOS is OFF (V_{GS} = 0)
  - No current through NMOS or resistor
  - Vout ≈ Vcc
- When Vin = Vcc:
  - NMOS is ON (V_{GS} = Vcc)
  - NMOS on resistance << R
  - Vout ≈ 0

Not suitable for VLSI: large area of R, DC power dissipation.



Remember: if body terminal not shown, it is connected to gnd for NMOS, vcc for PMOS

Resistive-load Inverter

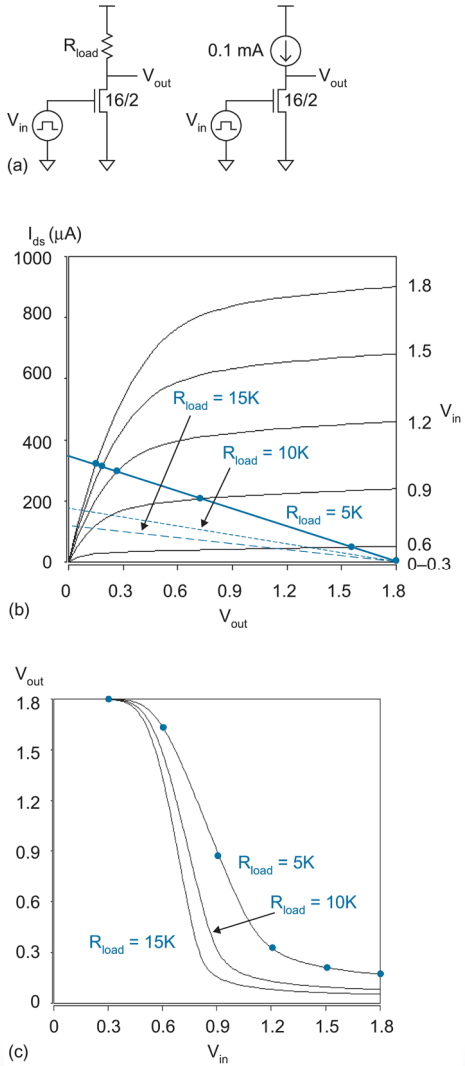
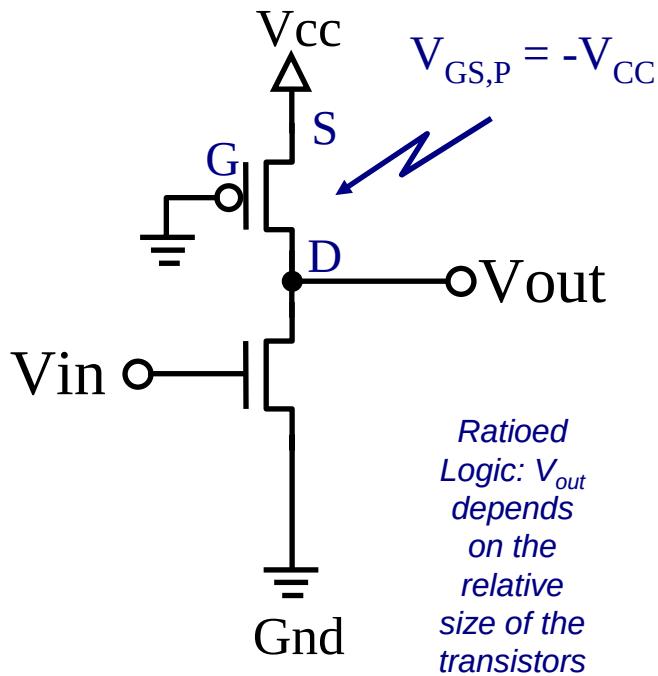


FIG 2.29 Generic nMOS inverters with resistive or constant current load

Pseudo-NMOS Inverter

- Replace resistor with "always-on" PMOS transistor
- Easier to implement in standard process than large resistance value
- PMOS load transistor:
  - On when $V_{GS} < V_T \rightarrow$ $V_{GS} = -V_{CC}$: transistor always on
  - Linear when $V_{DS} > V_{GS}-V_T \rightarrow$ $V_{out}-V_{cc} > -V_{cc}-V_T \rightarrow V_{out} > -V_T$
  - Saturated when $V_{DS} < V_{GS}-V_T \rightarrow$ $V_{out}-V_{cc} < -V_{cc}-V_T \rightarrow V_{out} < -V_T$



Remember:
$V_T(PMOS) < 0$

Pseudo-NMOS Inverter

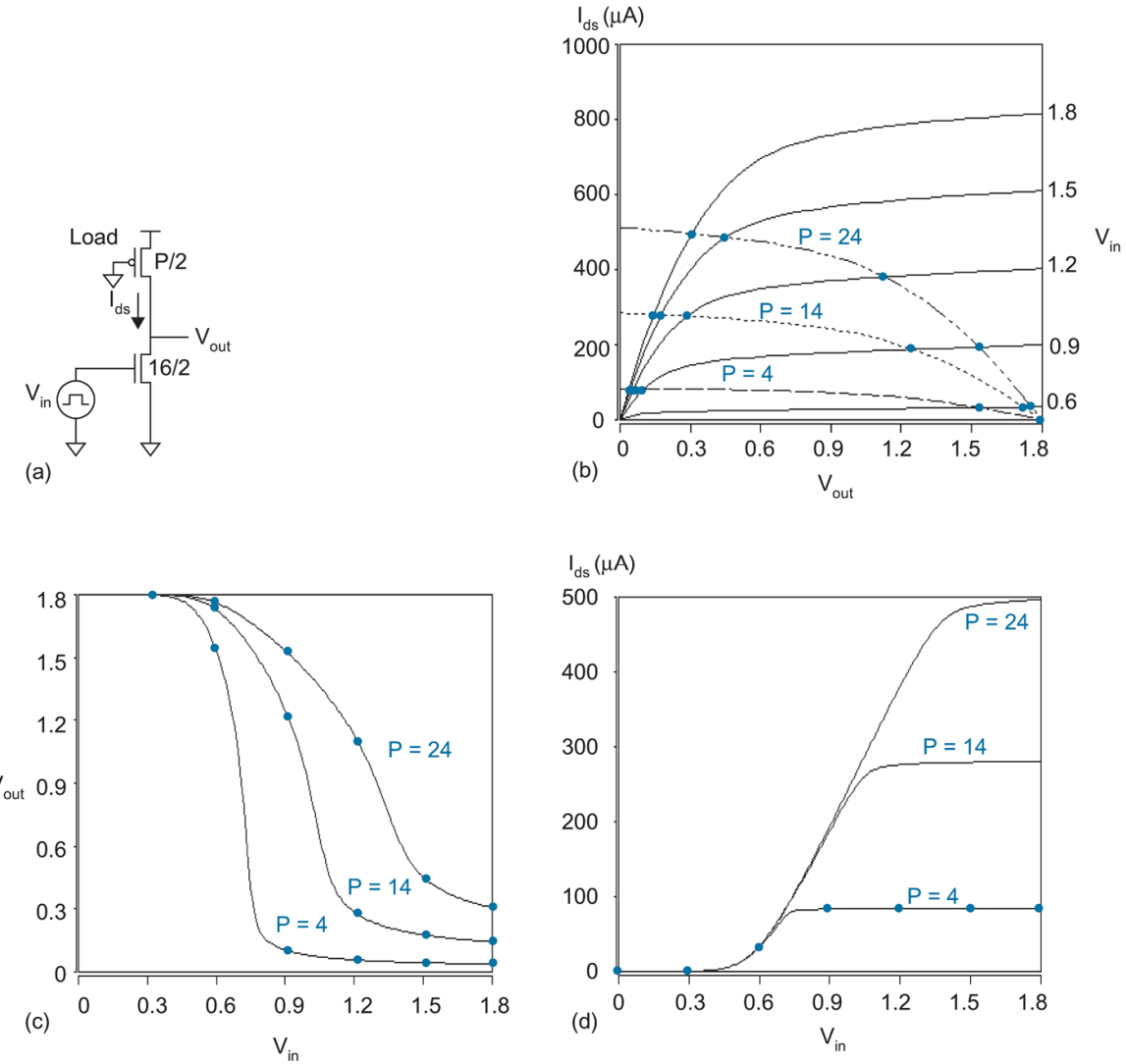
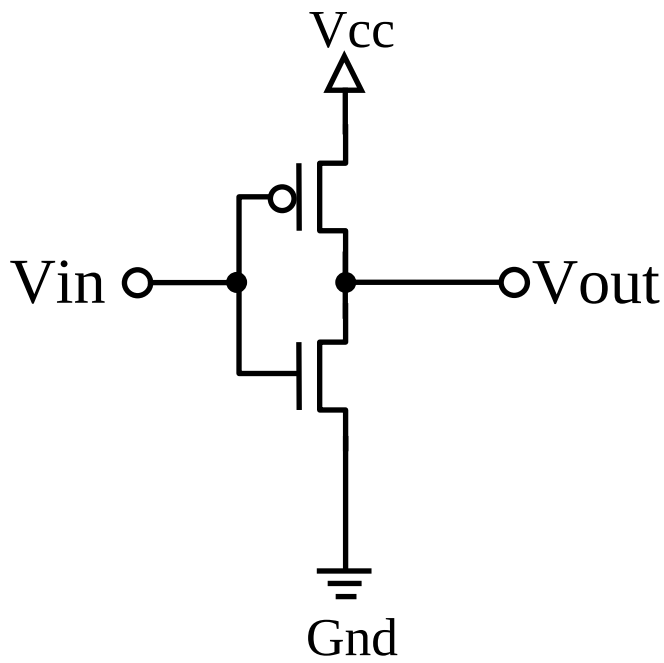


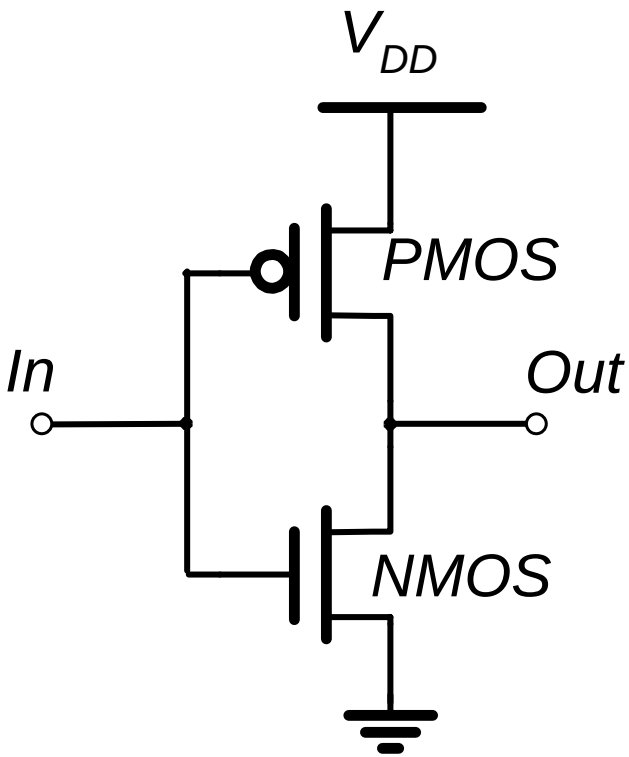
FIG 2.30 Pseudo-nMOS inverter and DC transfer characteristics

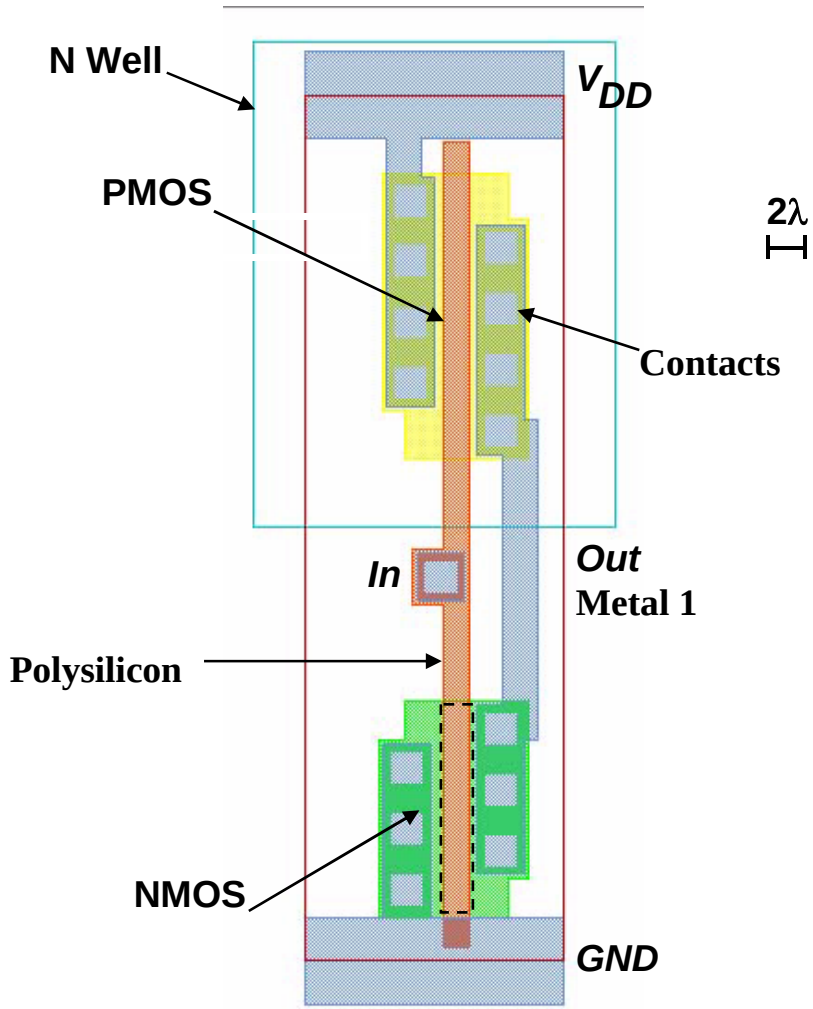
CMOS Inverter

- Complementary NMOS and PMOS devices
- In steady-state, only one device is on (no static power consumption)
- Vin=1: NMOS on, PMOS off
  - Vout = V_{OL} = 0
- Vin=0: PMOS on, NMOS off
  - Vout = V_{OH} = Vcc
- Ideal V_{OL} and V_{OH}!
- High input resistance (insulated gate) and low output impedance (finite resistance path between output and Vcc or Gnd)
- **Ratioless logic**



CMOS Inverter

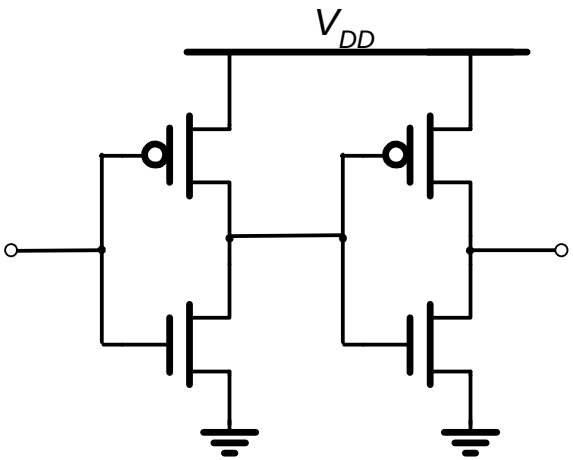


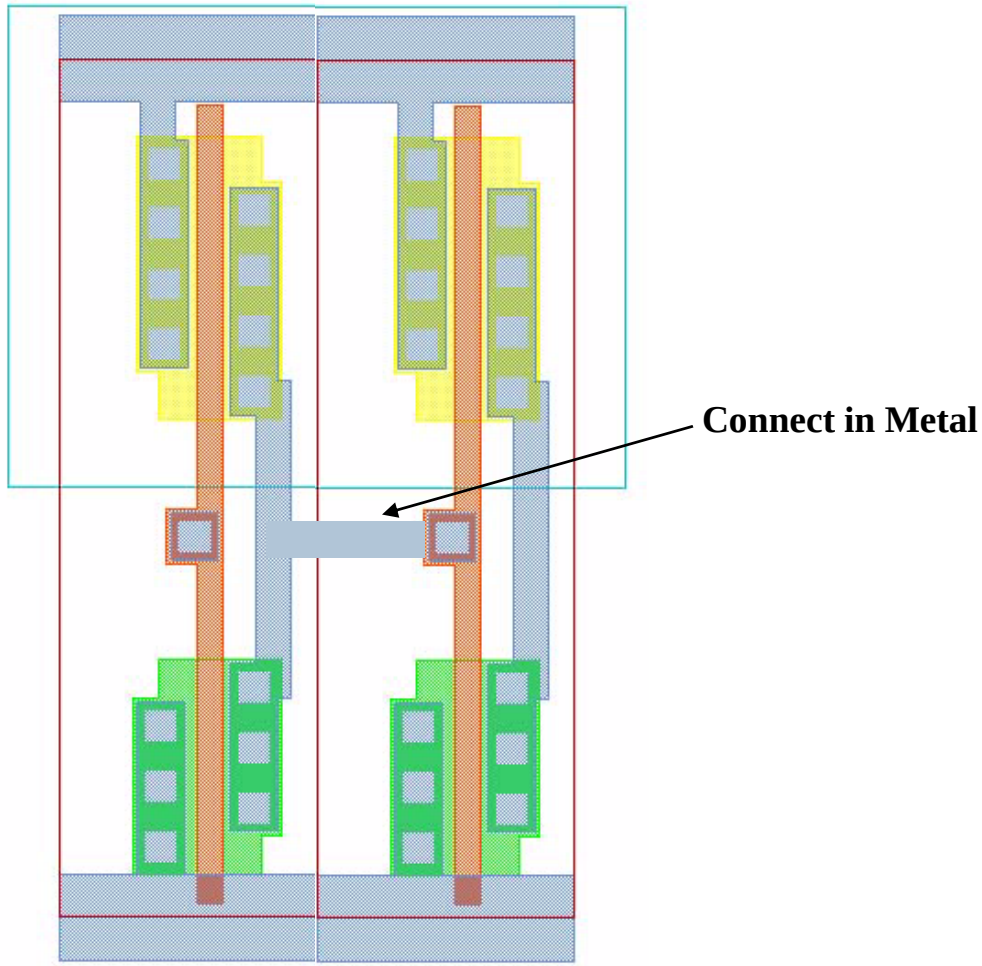


Two Inverters

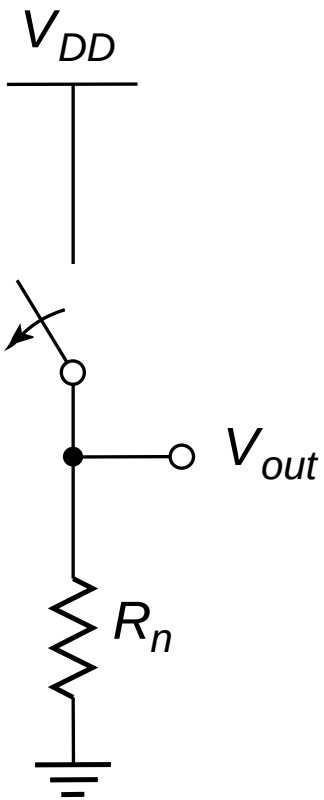
Share power and ground

Abut cells

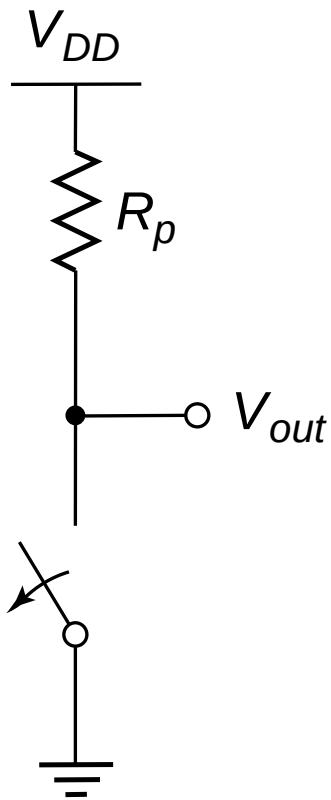




CMOS Inverter
First-Order DC Analysis



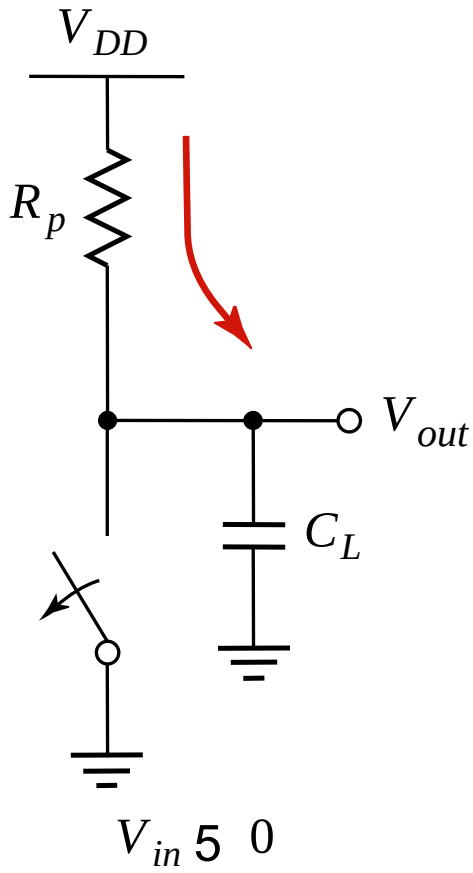
V_{in} 5 V_{DD}



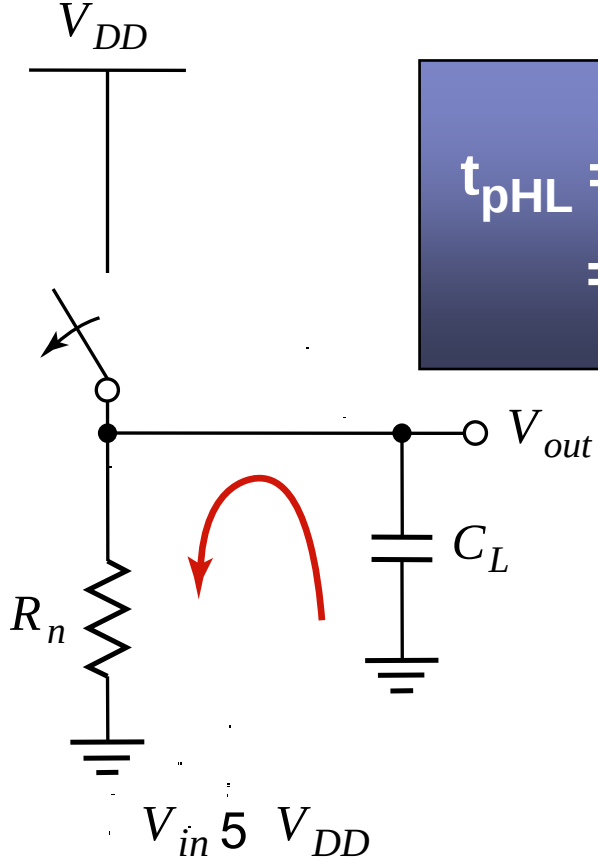
V_{in} 5 0

$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

CMOS Inverter: Transient Response



(a) Low-to-high



(b) High-to-low

$t_{pHL} = f(R_{on}.C_L)$
$= 0.69\ R_{on}C_L$

CMOS Inverter Operation (summary)

Table 2.2 Relationships between voltages for the three regions of operation of a CMOS inverter

	Cutoff	Linear	Saturated
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$
		$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
		$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

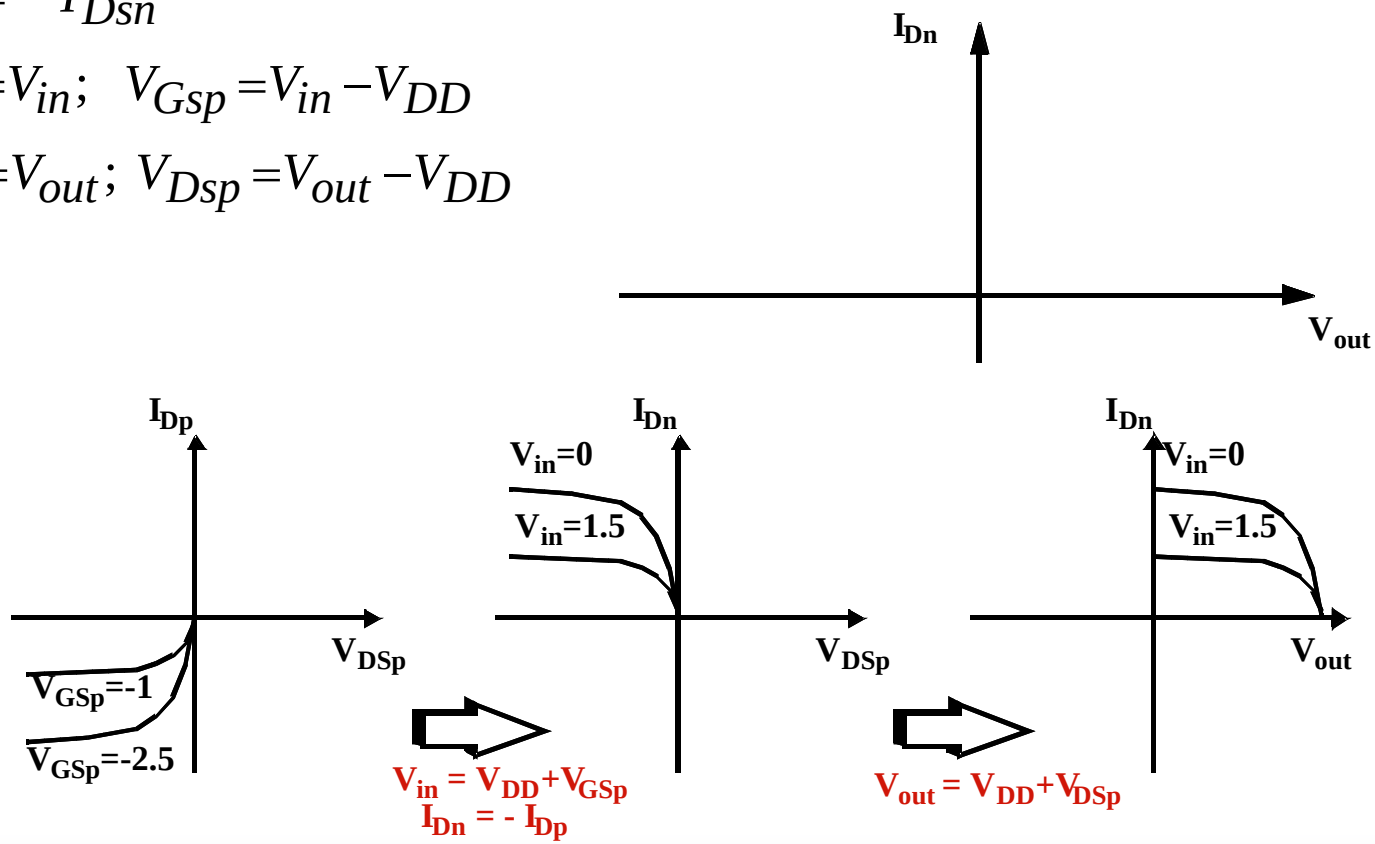
Generating the Inverter VTC

A. *Translate PMOS I-V Relations into NMOS Variable Space using the following:*

$$I_{Dsp} = -I_{Dsn}$$

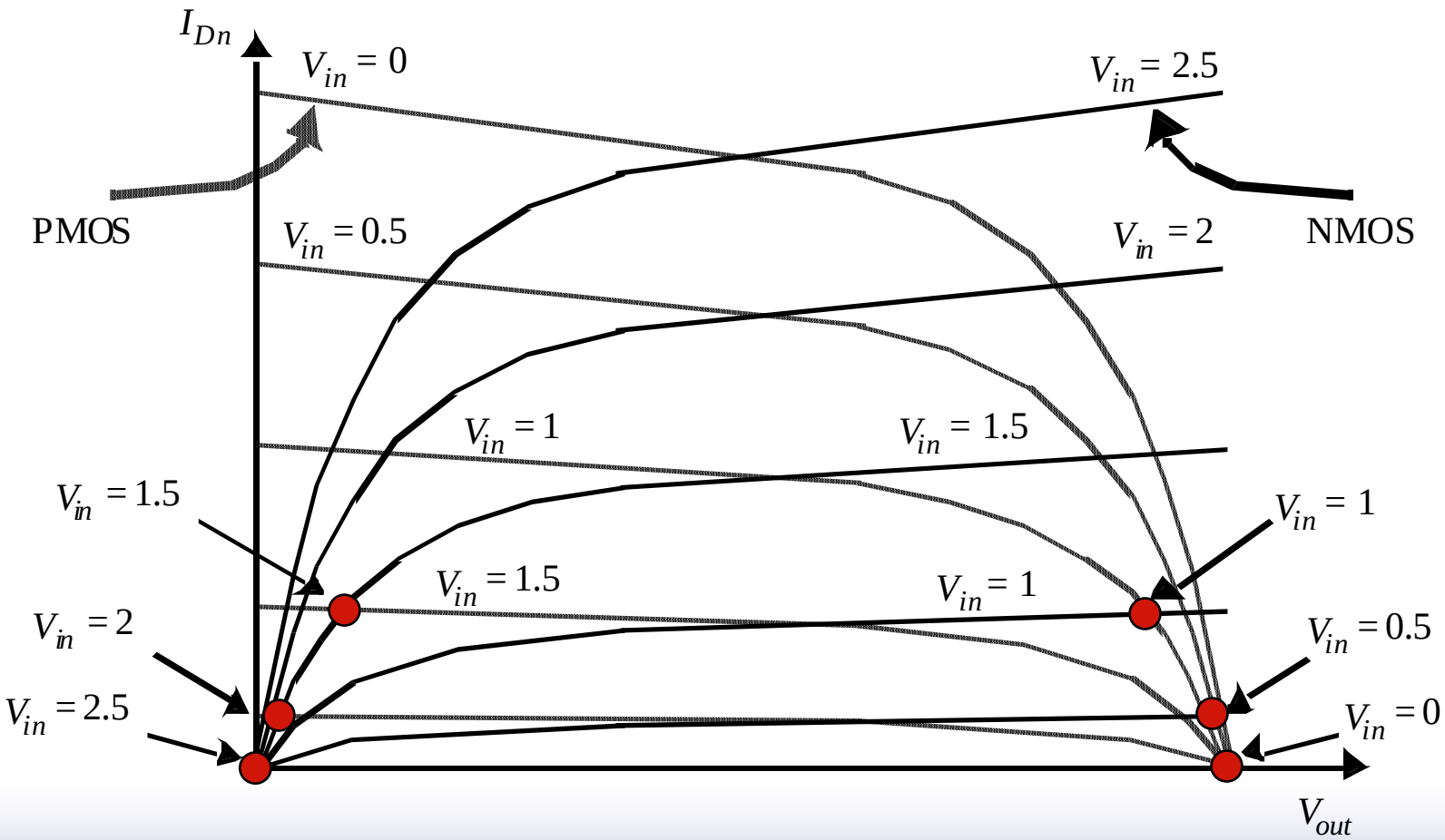
$$V_{Gsn} = V_{in};\quad V_{Gsp} = V_{in} - V_{DD}$$

$$V_{Dsn} = V_{out};\quad V_{Dsp} = V_{out} - V_{DD}$$

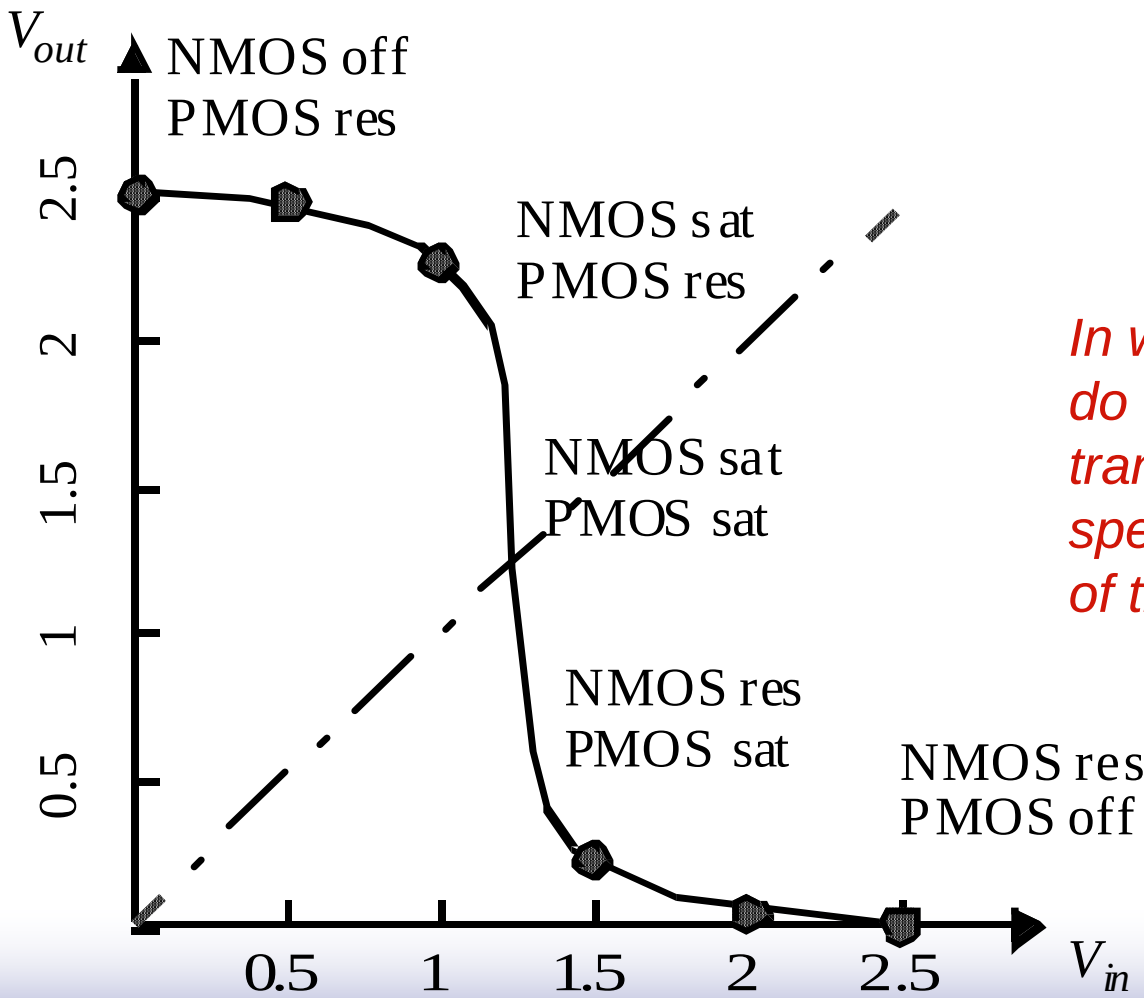


CMOS Inverter Load Characteristics

B. For a DC operating point to be valid, currents through NMOS and PMOS must be equal, hence find the points of intersection.

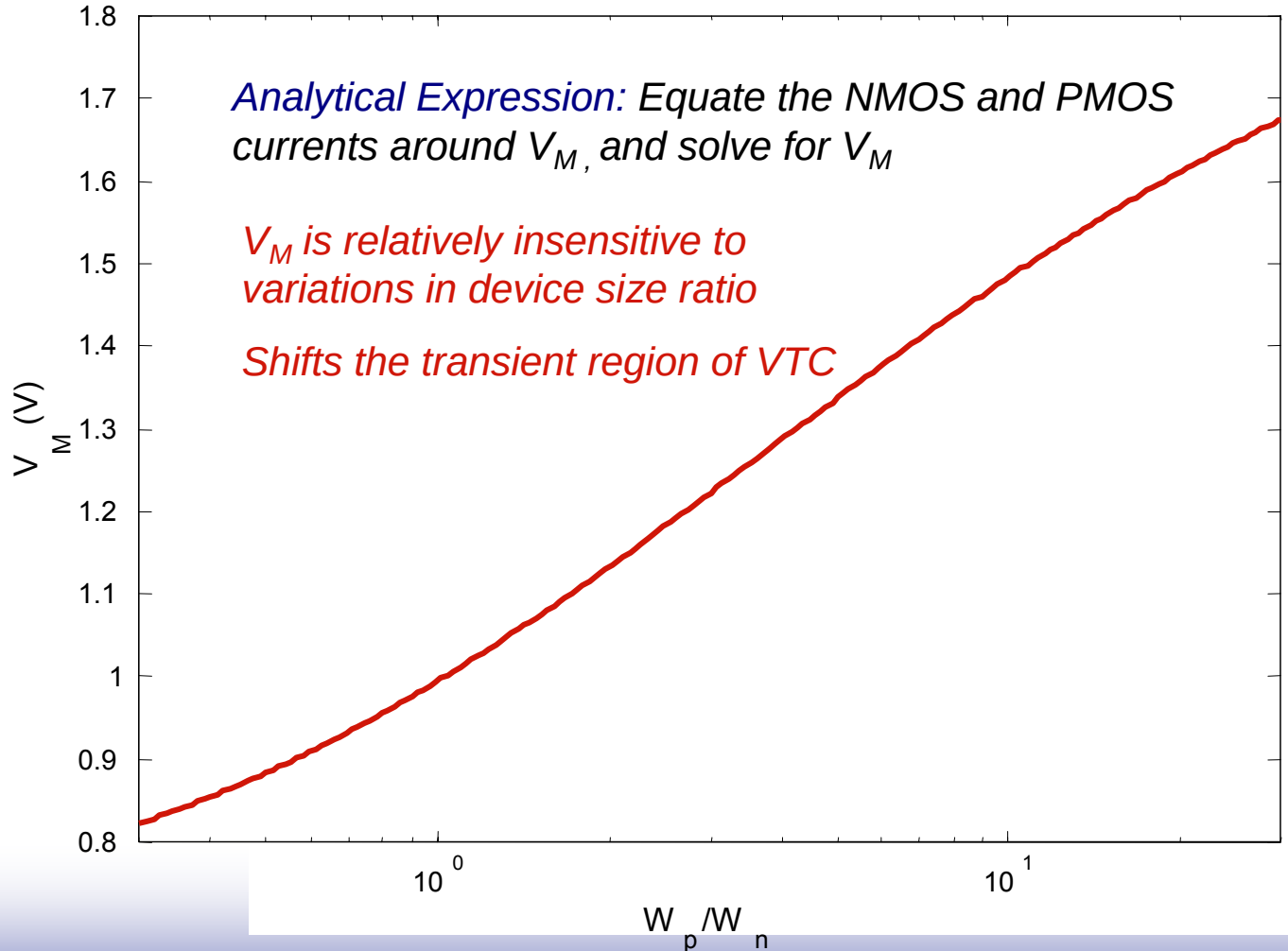


CMOS Inverter VTC



In which state do the transistors spend most of their time?

Switching Threshold as a function of Transistor Ratio

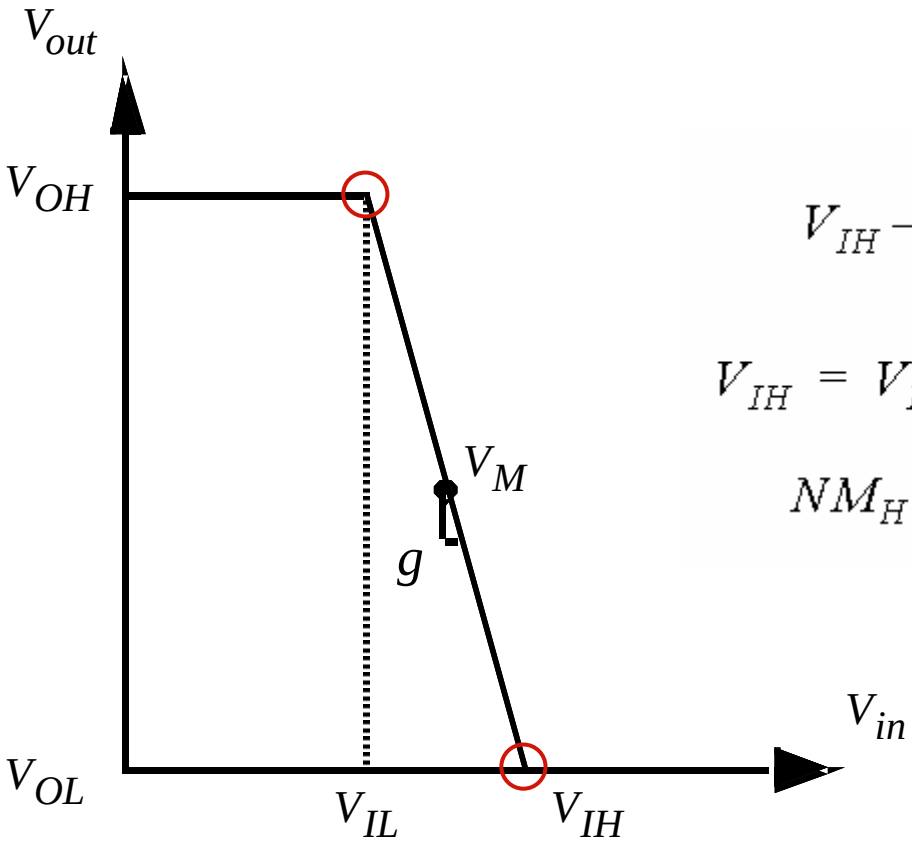


Analytical Expression: Equate the NMOS and PMOS currents around V_M, and solve for V_M

V_M is relatively insensitive to variations in device size ratio

Shifts the transient region of VTC

Determining V_{IH} and V_{IL}



i.e., $V_{OH}=V_{DD}$ and $V_{OL}=0$

$$V_{IH} - V_{IL} = -\frac{(V_{OH} - V_{OL})}{g} = \frac{-V_{DD}}{g}$$

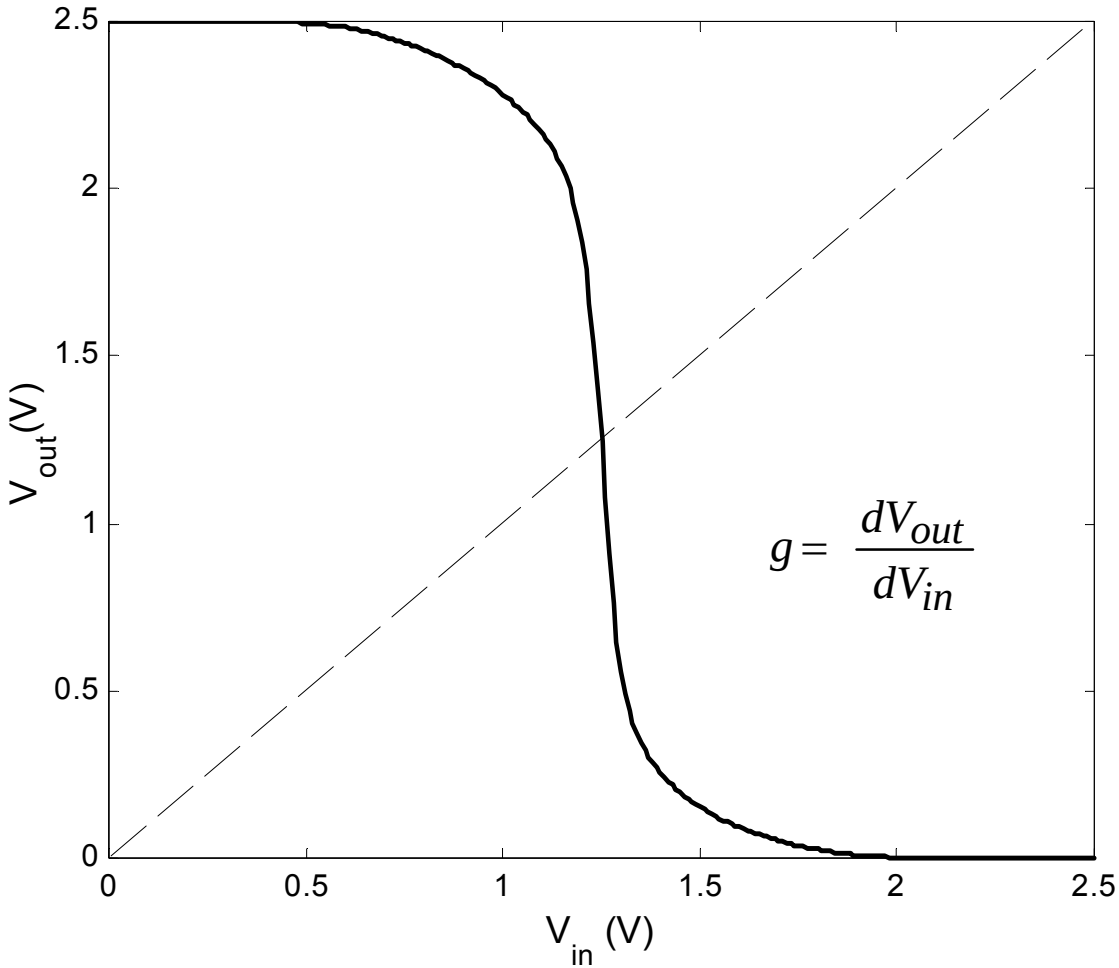
$$V_{IH} = V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$NM_H = V_{DD} - V_{IH} \qquad NM_L = V_{IL}$$

Note: As $g \to \infty$, $V_{IH}=V_{IL}=V_M$, i.e., ideal inverter

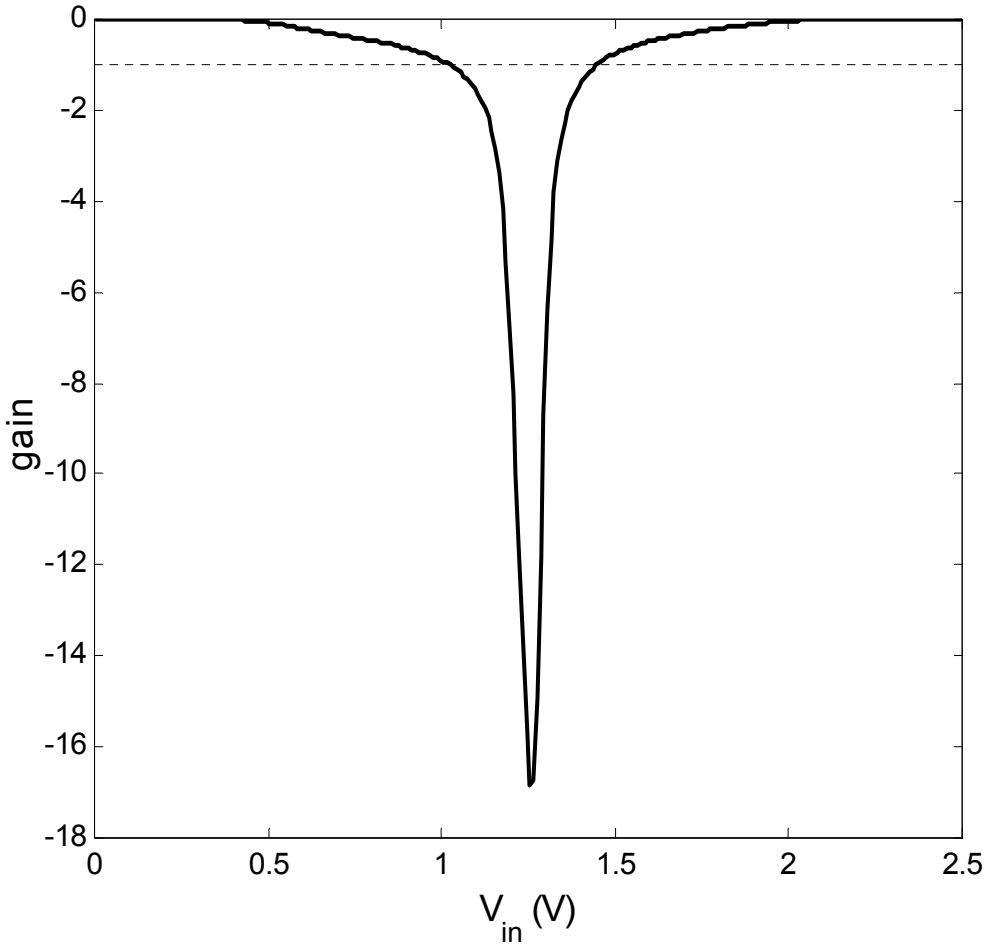
A simplified approach: piecewise linear approximation of the VTC

Simulated VTC



Note: piecewise linear approximation of the VTC would lead to higher gain

Inverter Gain



Gain is mostly determined by technology parameters, especially channel length modulation, but also by V_{DD}

Note: approximately $V_M \propto V_{DD}$

Inverter Skew

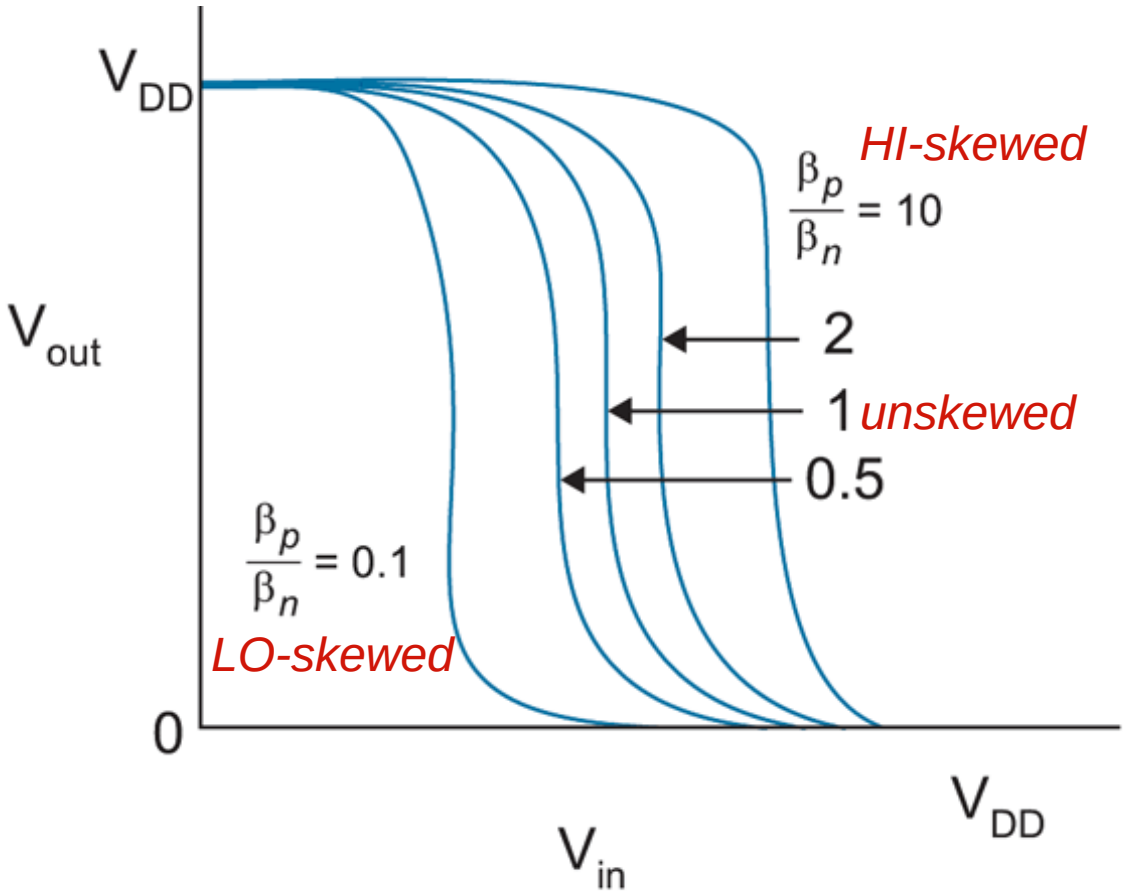
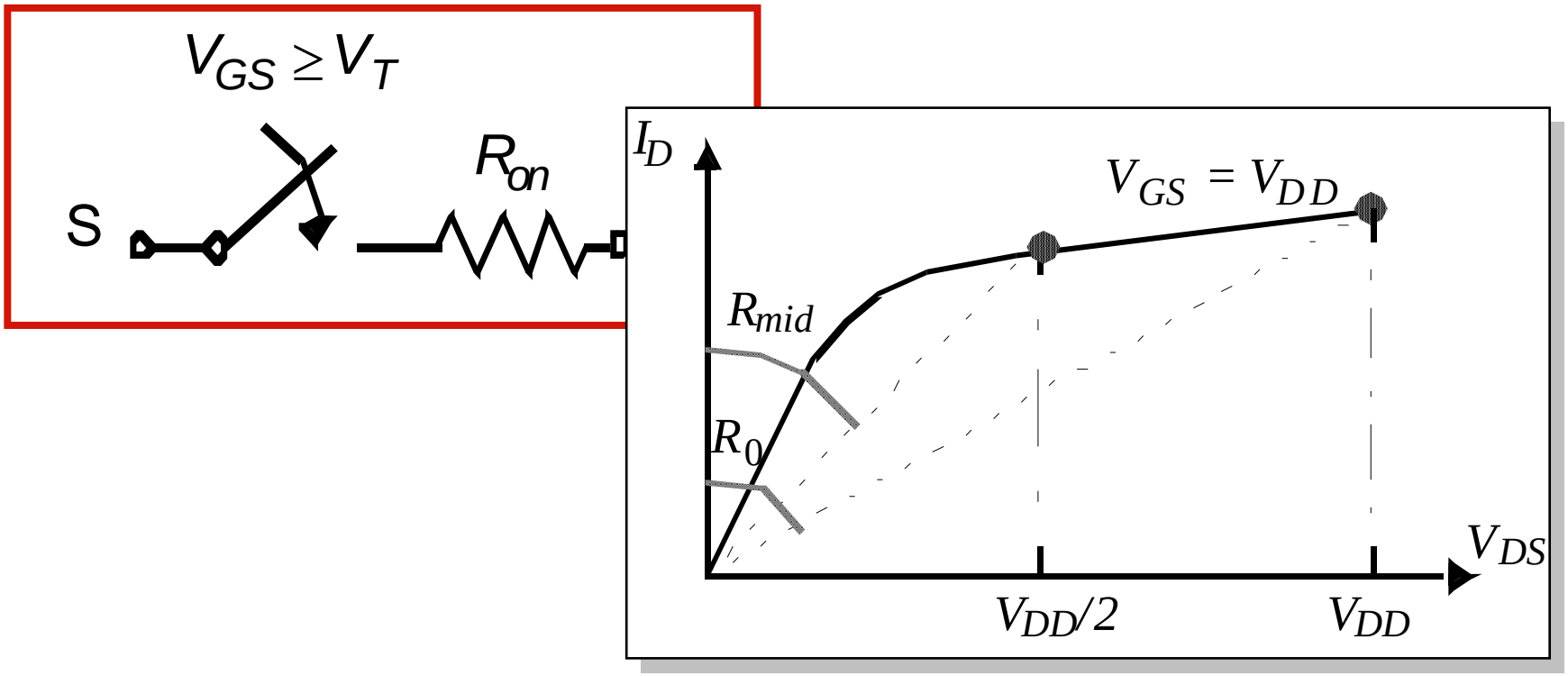


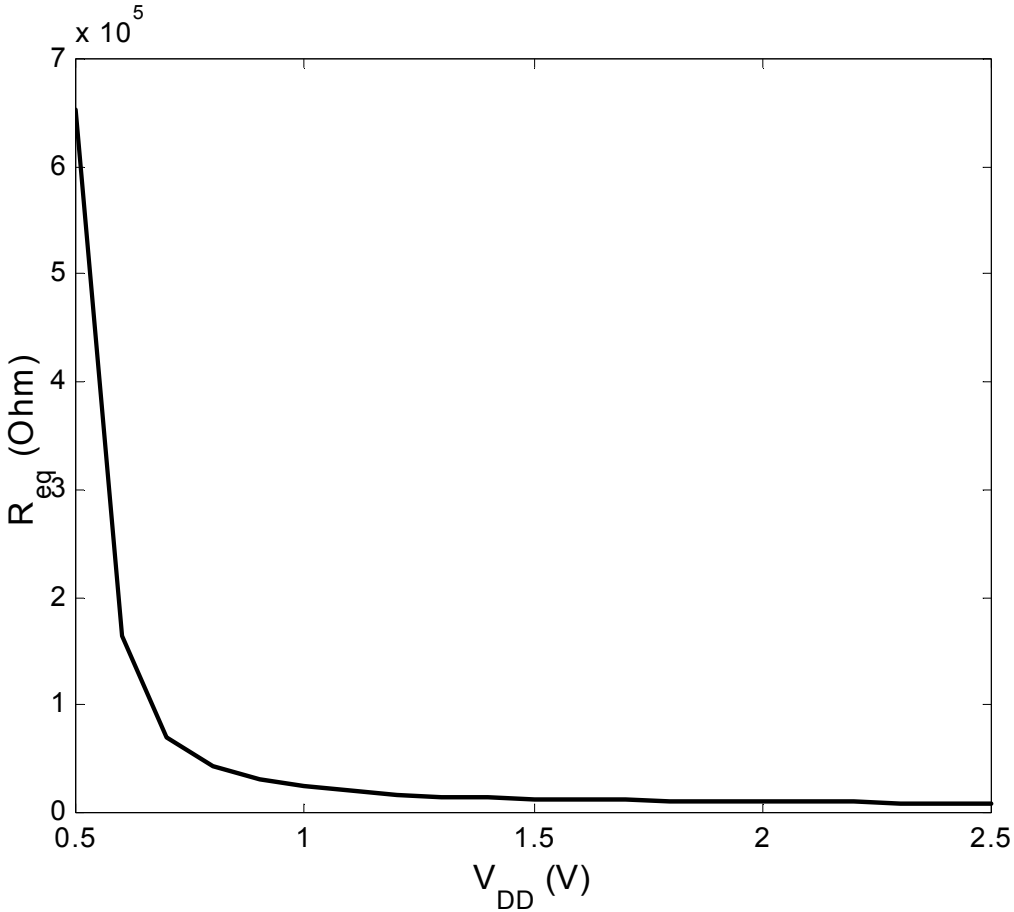
FIG 2.26 Transfer characteristics of skewed inverters

The Transistor as a Switch



$$R_{eq} = \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1+\lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1+\lambda V_{DD}/2)}\right) \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{5}{6}\lambda V_{DD}\right)$$

The Transistor as a Switch



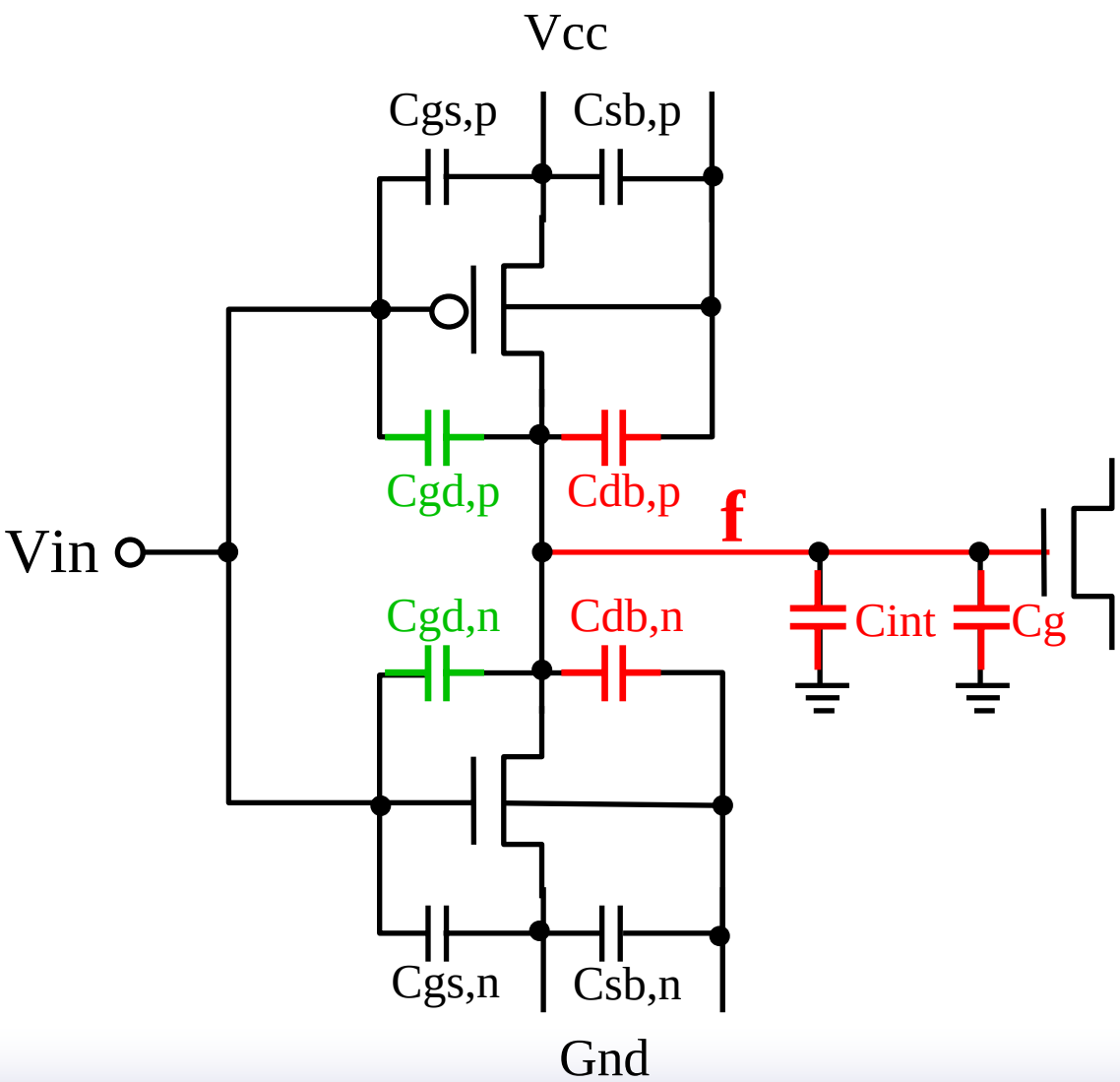
The Transistor as a Switch

Table 3.3 Equivalent resistance R_{eq} (W/L= 1) of NMOS and PMOS transistors in 0.25 μm CMOS process (with $L = L_{min}$). For larger devices, divide R_{eq} by W/L.

V_{DD} (V)	1	1.5	2	2.5
NMOS (kΩ)	35	19	15	13
PMOS (kΩ)	115	55	38	31

Propagation Delay

CMOS inverter capacitances



Cap on Node f:

- Junction cap: $C_{db,p}$ and $C_{db,n}$
- Gate (overlap) capacitance $C_{gd,p}$ and $C_{gd,n}$ (beware of Miller effect)
- Interconnect cap: C_{int}
- Receiver gate cap: C_g

CMOS inverter capacitances

$$C_{load} = \underbrace{C_{db,n} + C_{db,p}} + \underbrace{C_{gd,n} + C_{gd,p}} + C_{\text{int}} + \underbrace{C_{gate}}$$

$$C_{db,n}, C_{db,p} = AK_{eq}C_{j0} + PK_{eqsw}C_{jsw}$$

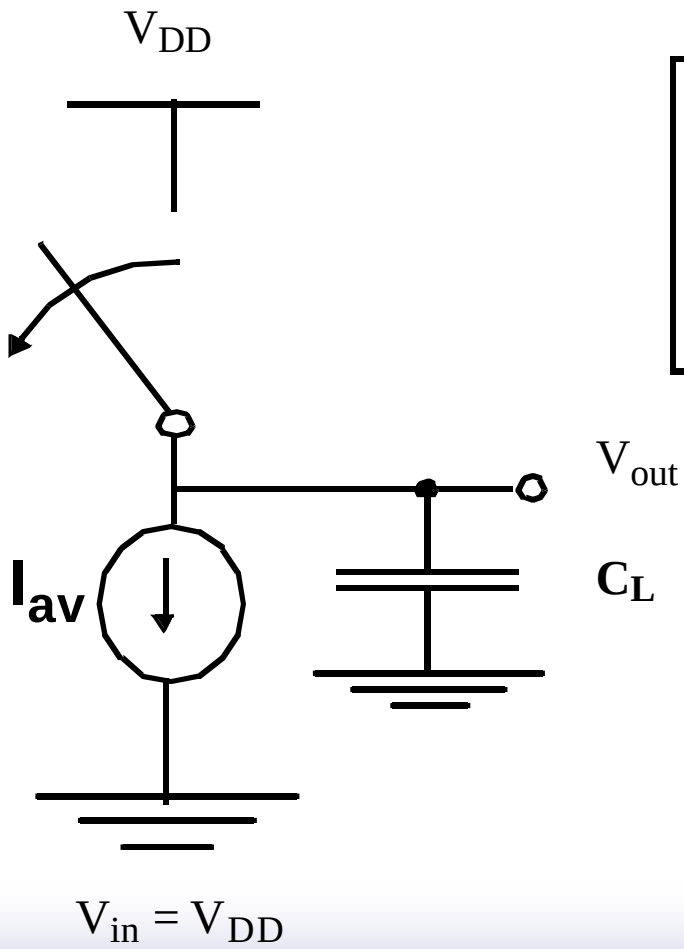
$$C_{gd,n}, C_{gd,p} = 2WL_DC_{ox}$$

Miller effect

$$C_{gate} = WL_{drawn}C_{ox}$$

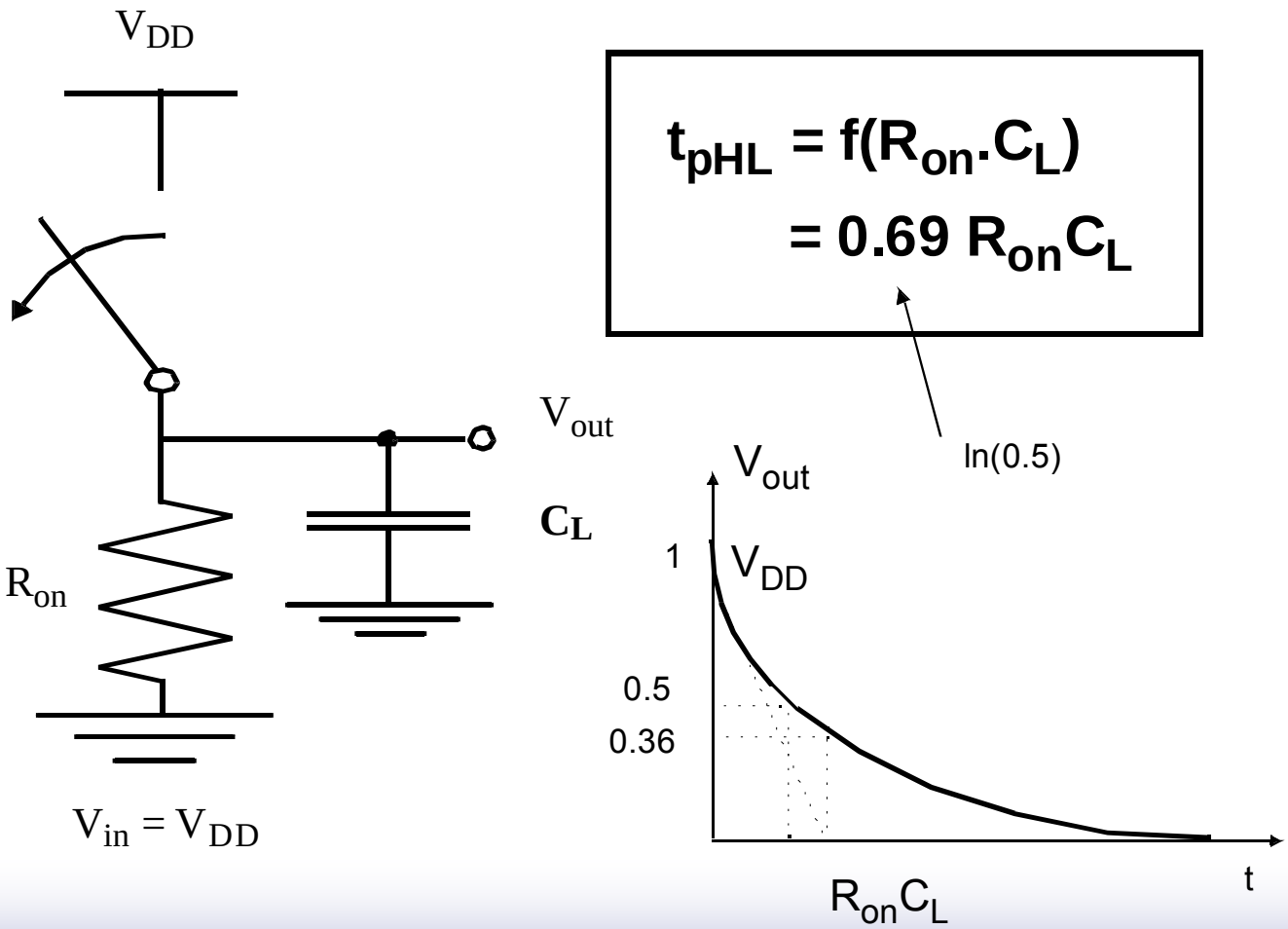
For each gate

CMOS Inverter Propagation Delay Approach 1

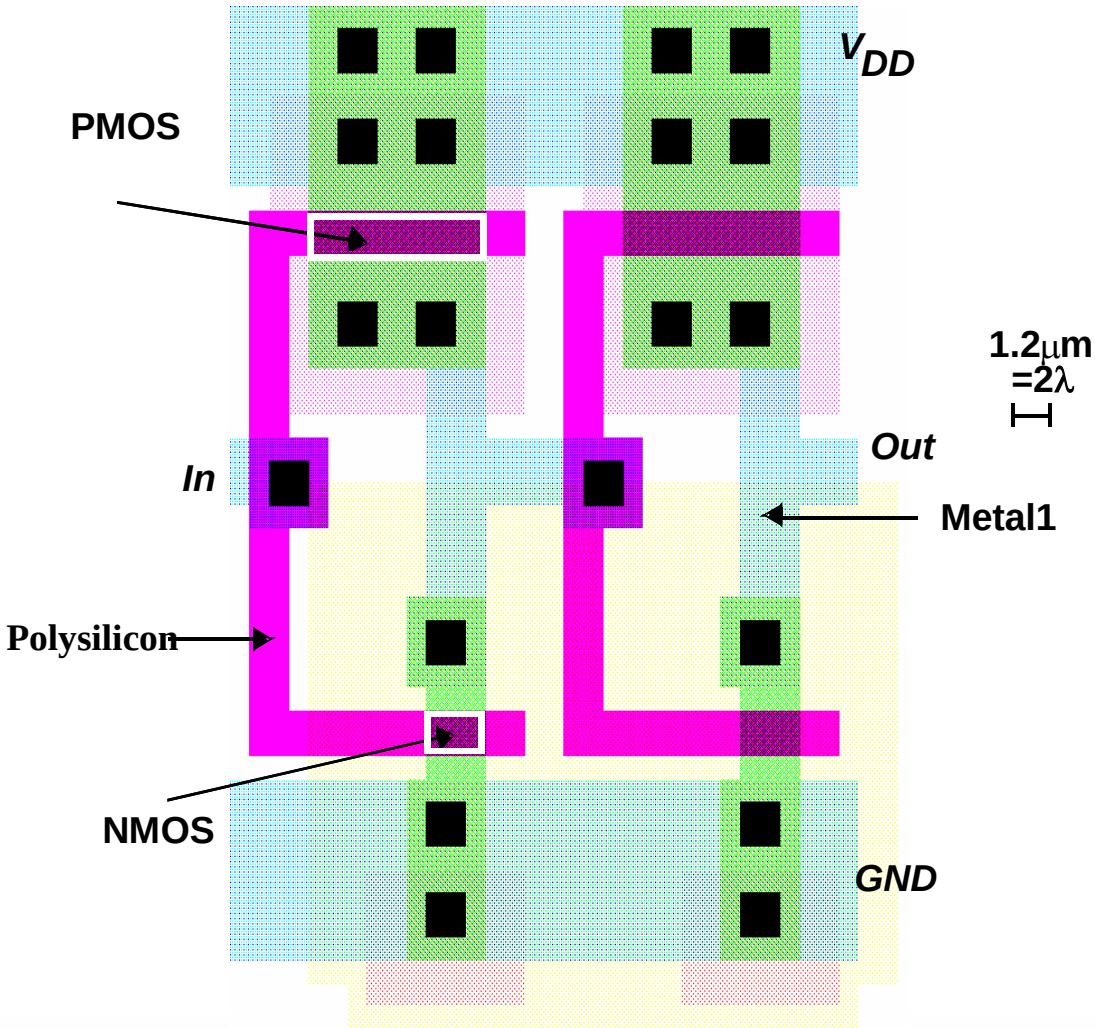


$$t_{pHL} = \frac{C_L \, V_{swing}/2}{I_{av}}$$

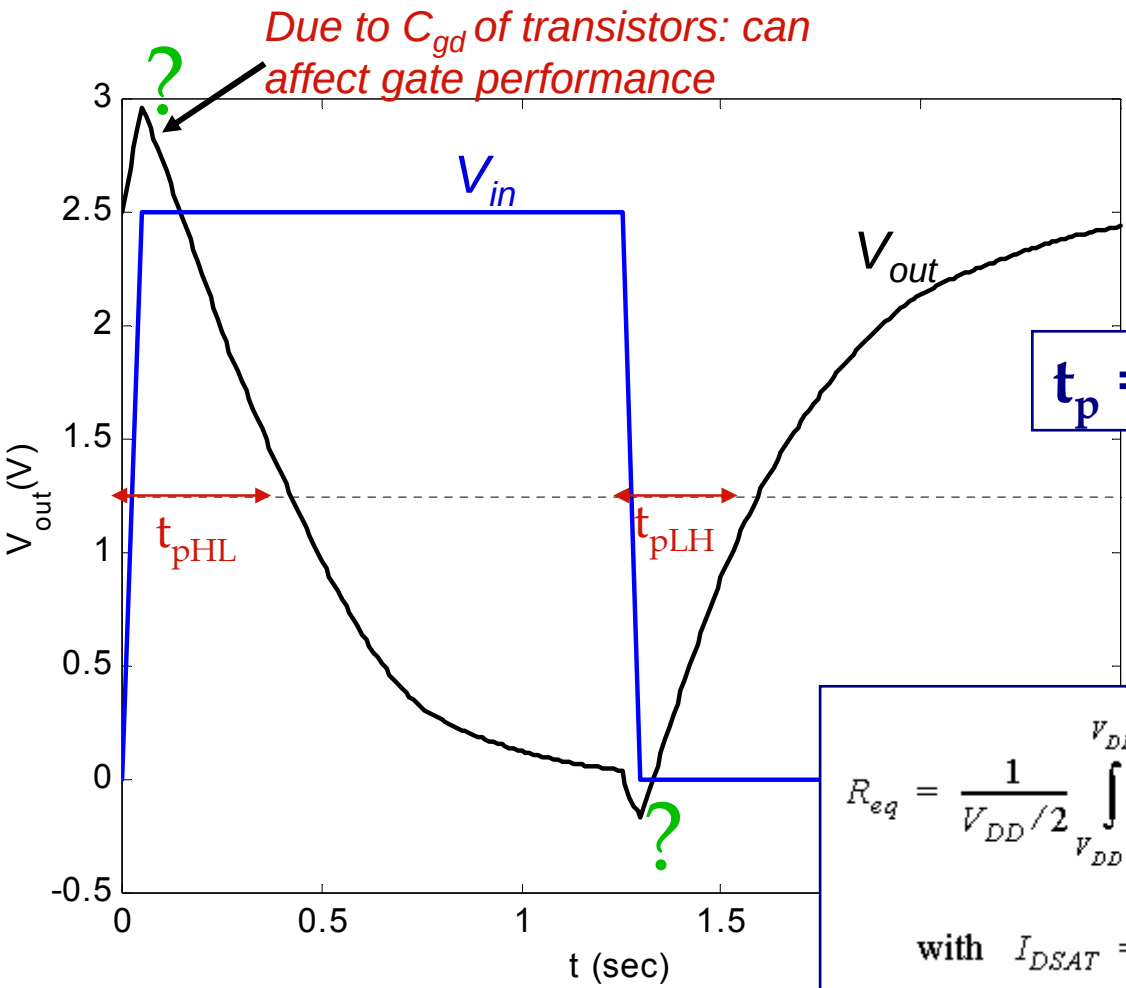
CMOS Inverter Propagation Delay Approach 2



CMOS Inverters



Transient Response



Symmetric inverter has $t_{pHL}=t_{pLH}$

$$t_p = 0.69\, C_L\, (R_{eqn}+R_{eqp})/2$$

$$R_{eq} = \frac{1}{V_{DD}/2}\int_{V_{DD}/2}^{V_{DD}} \frac{V}{I_{DSAT}(1+\lambda V)}dV \approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1-\frac{7}{9}\lambda V_{DD}\right)$$

$$\text{with}\quad I_{DSAT} = k'\frac{W}{L}\left((V_{DD}-V_T)V_{DSAT}-\frac{V_{DSAT}^2}{2}\right)$$

Design for Performance

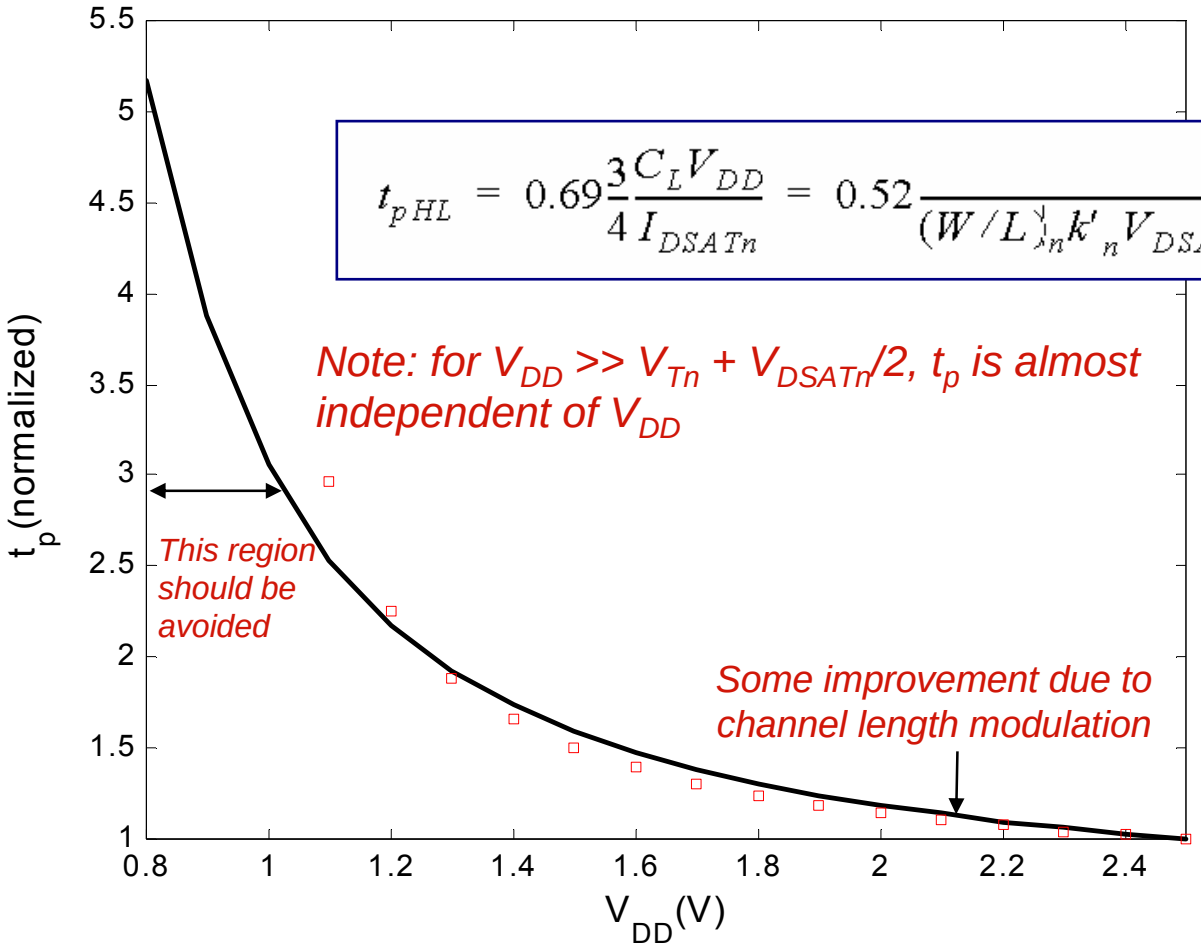
- Keep load capacitances (C_L) small
  - Recall that three major components contribute to the load cap.
    - internal diffusion + overlap caps
    - interconnect cap.
    - fan-out (gate cap)
- Increase transistor sizes
  - watch out for self-loading!
- Increase V_{DD} (??)
  - watch out for reliability issues!

Delay as a function of V_{DD}

Same as the ON resistance of a transistor….

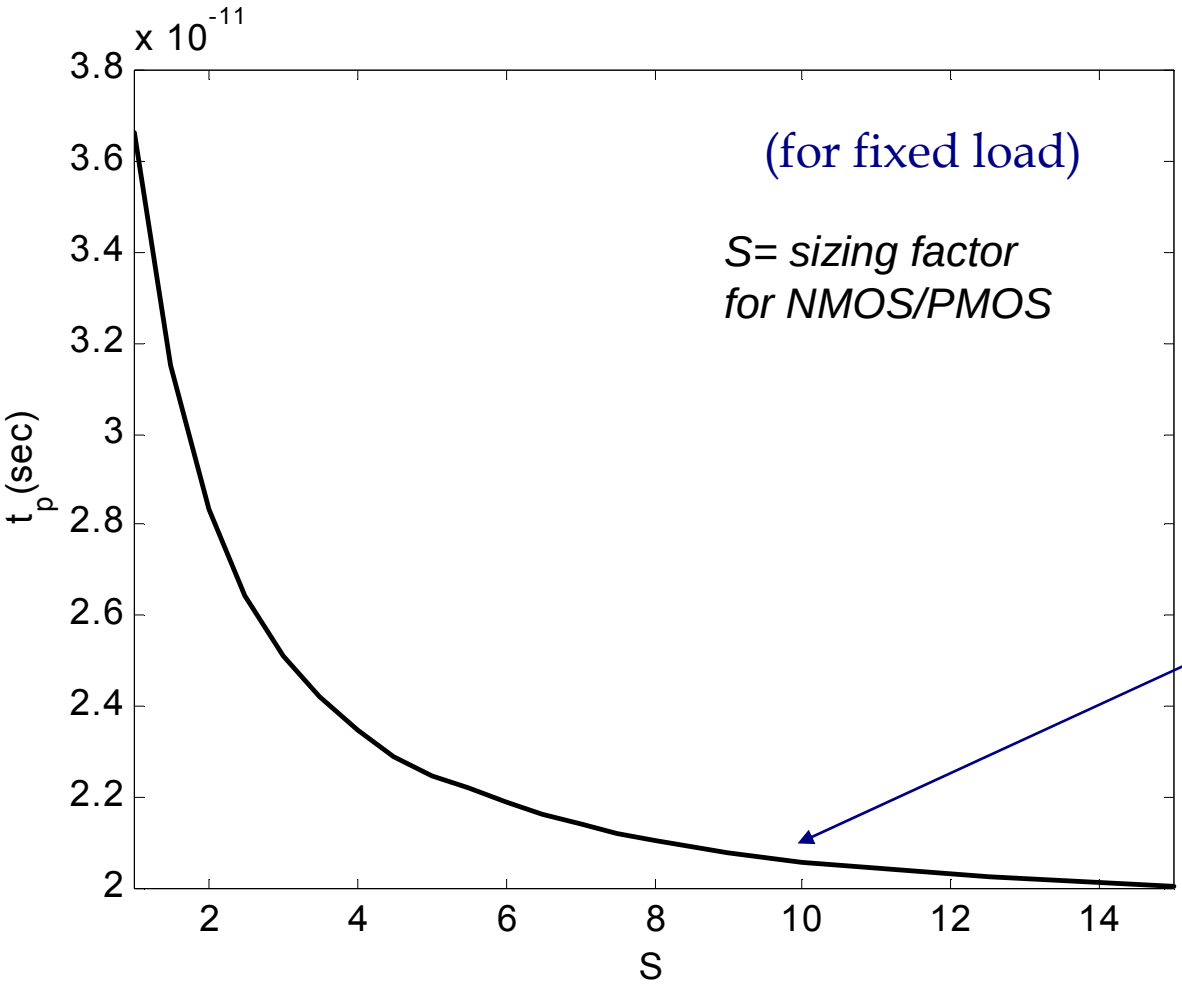
Trade off energy dissipation vs performance…..

$$t_{pHL} = 0.69\frac{3}{4}\frac{C_L V_{DD}}{I_{DSATn}} = 0.52\frac{C_L V_{DD}}{(W/L)_n k'_n V_{DSATn}(V_{DD} - V_{Tn} - V_{DSATn}/2)}$$



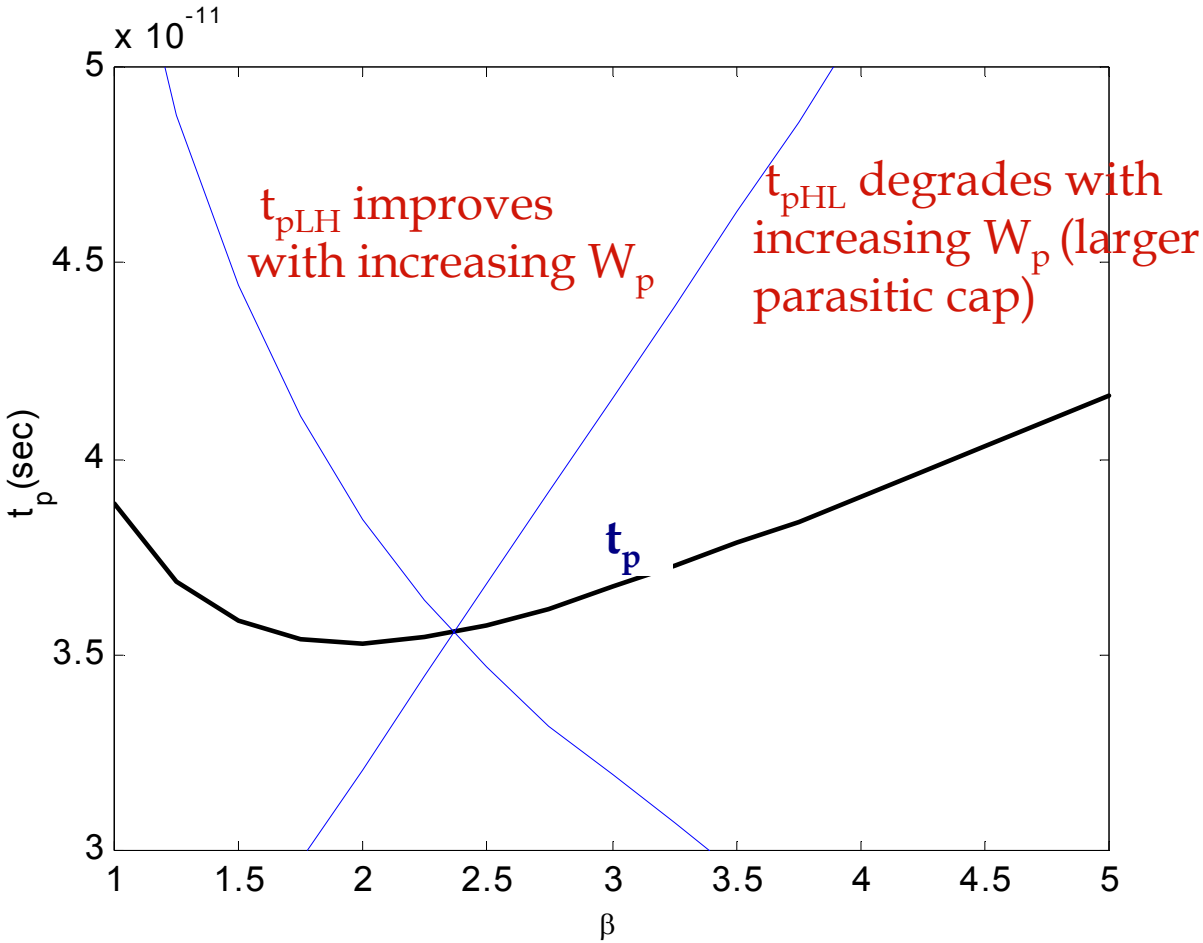
Reliability concerns at high V_{DD}….

Device Sizing



Self-loading effect:
Intrinsic capacitances dominate

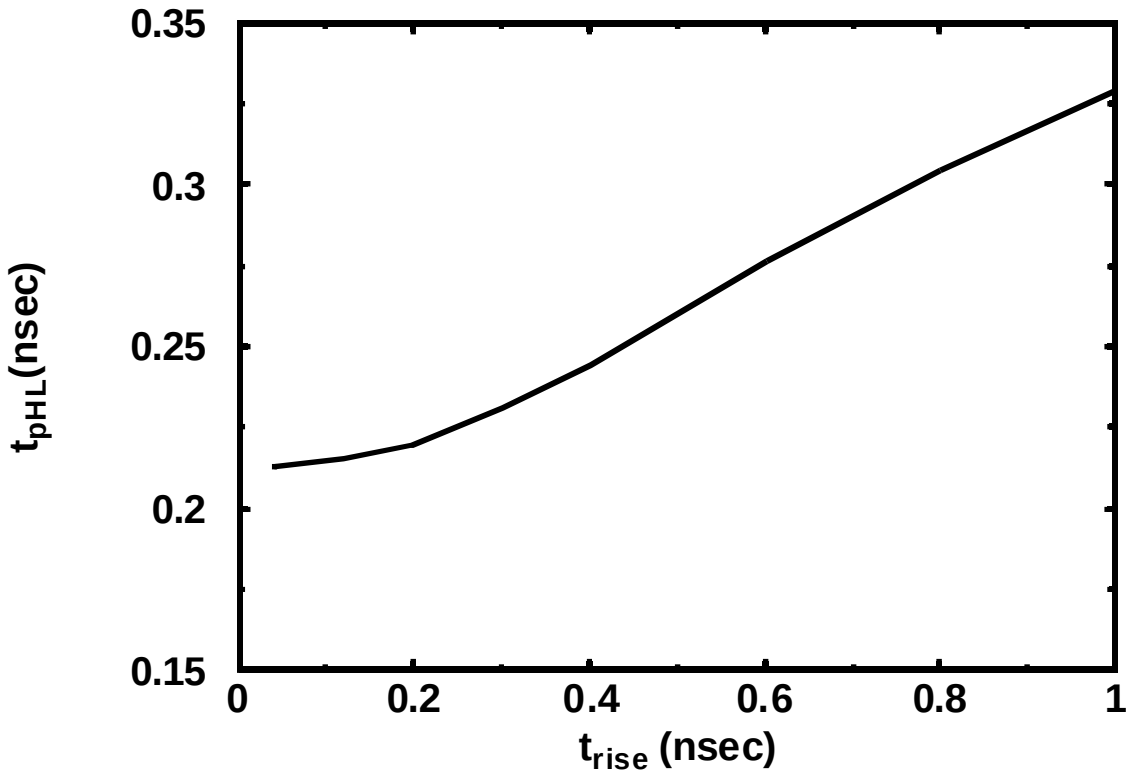
NMOS/PMOS ratio



$\beta = W_p/W_n$

If symmetry and noise margins are not of prime concern, inverter delay can be reduced by reducing the width of PMOS….

Impact of Rise Time on Delay



$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$