

University Of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 225 High-Speed Digital Integrated Circuit Design

Assignment #1

Due Date: Monday, May 2, at 4 pm in class (To be collected by Junkai Jiang)

Problem 1 Semiconductor Physics

- Consider a cube of semiconductor crystal with length L on each side. Derive the density of electron states $D_{3D}(E)$. Similarly, derive the density of electron states for a 2-dimensional system $D_{2D}(E)$. Sketch the density of states for the 3D and 2D cases. Assume the electron effective mass is m_n .
- In a silicon sample doped with 10^{17} cm^{-3} of phosphorus atoms, what fraction of the donors are not ionized. The donor level E_d is located at 45 meV below conduction band edge for phosphorus.
- Use the Matthiessen's rule to calculate and plot the mobility vs. temperature $\mu(T)$ from 10 K to 500 K for Si doped with $N_d = 10^{14}$, 10^{16} , and $10^{18} \text{ donors cm}^{-3}$. Consider the mobility to be determined by impurity and phonon (lattice) scattering. Impurity scattering limited mobility can be described by

$$\mu_i = 3.29 \times 10^{15} \frac{\epsilon_r^2 T^{3/2}}{N_d^+ (m_n^* / m_0)^{1/2} [\ln(1+z) - \frac{z}{1+z}]}$$

where

$$z = 1.3 \times 10^3 \epsilon_r T^2 (m_n^* / m_0) (N_d^+)^{-1}$$

Assume that the ionized impurity concentration N_d^+ is equal to N_d at all temperatures.

The conductivity effective mass m_n^* for Si is $0.26m_0$. Acoustic phonon (lattice) scattering limited mobility can be described by

$$\mu_{AC} = 1.18 \times 10^{-5} c_1 (m_n^* / m_0)^{-5/2} T^{-3/2} (E_{AC})^{-2}$$

where the stiffness (c_1) is given by

$$c_1 = 1.9 \times 10^{12} \text{ dyne-cm}^{-2} \text{ for Si}$$

and the conduction band acoustic deformation potential (E_{AC}) is

$$E_{AC} = 9.5 \text{ eV for Si.}$$

Problem 2 MOS Capacitor CV

The MOS capacitor theory was covered in detail in the lectures (for p-type body). Using the lecture notes, repeat all derivations for an n-type body. All other parameters can be assumed to be same as those used for the p-type body. You may assume $E_F - E_C = 0.4$ eV

Draw the band diagrams and derive expressions for the following conditions:

- Flat-band condition.
- Surface-accumulation condition.
- Surface-depletion condition.
- Threshold condition and threshold voltage.
- Strong-inversion (beyond V_T).
- Using the expressions derived above in (a)-(e), plot the C-V characteristics of such MOS capacitor for both low and high frequency conditions.

Problem 3 MOSFET Scaling Issues

- According to your understanding of the so-called short-channel effect, what kind of electric field distribution inside the device is desirable in order to minimize this effect? Hint: make connection with DIBL.
- Sketch the curve of carrier velocity vs. lateral electric field for a device in which velocity saturation occurs and briefly describe the cause of velocity saturation.
- Analyze how velocity saturation affects the voltage-transfer-characteristics (VTC) of a balanced CMOS inverter.
- In short channel MOSFETs, retrograded doping profile is usually adopted to suppress the punch-through effect. Please refer to the paper below to get familiar with such devices. Try to derive the expression of SS for these devices in the long-channel case. You can assume that the doping profile is abrupt at the junction between the lightly and highly doped layers. (Reference: Indranil De et al., "Impact of Super-Steep-Retrograde Channel Doping Profiles on the Performance of Scaled Devices," *IEEE Transactions on Electron Devices*, vol. 46, no. 8, Aug. 1999.)

Problem 4 MOSFET Electrostatics

Following the discussions in class, derive the expressions for the Natural Length (λ) for the following devices:

- Planar Bulk MOSFETs (with and without high-k dielectric)
- Ultra-thin Body (UTB) SOI MOSFETs (partially depleted and fully depleted)

- c) Double-gate FETs: (FinFET) and Tri-gate FET
- d) Gate-all-around FET (or a nanowire FET)

Problem 5 Tunnel-FETs

Please review lecture 8, slide 12 showing the slow V_{ds} turn-on.

- a) Why the I_D - V_D is not linear at low V_D regime? Is this an intrinsic or extrinsic property? Is there any possibility to eliminate it? If tunnel FETs are used to design a 1T-DRAM, what effect could be expected?
- b) Analyze the enhanced Miller effect in a tunnel FET based inverter with load capacitance, reproduce the figure (showing Miller effect) by SPICE simulation. (hint: you can use MOSFETs instead of tunnel FETs in the simulation, and artificially change the capacitance).