University Of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 225 High-Speed Digital Integrated Circuit Design

Assignment #2

Due Date: Monday, May 16, at 4 pm in class (To be collected by Junkai Jiang)

Problem 1 Digital Design Styles

Consider a minimum size CMOS inverter in a 22nm technology node. The technology files (device models) can be downloaded from Predictive Technology Model (http://ptm.asu.edu/). Use the 22nm PTM HP model.

a) By using SPICE simulations, plot the effect of V_{dd} scaling (while keeping V_{th} fixed) on the delay, power dissipation (various components), noise margins and the DC transfer curve of the CMOS inverter.

b) Repeat a) assuming V_{th} scales at the same rate as V_{dd}.

c) Repeat a) for a pseudo-NMOS inverter.

d) Repeat a) for a pass-transistor based inverter.

e) Repeat a) for a dynamic inverter.

f) Compare the area consumption of the design styles in a) c) d) and e).

Problem 2 Power Dissipation

As derived in class, the minimum required V_{dd} for a digital CMOS logic circuit is given by a few times kT/q. What will be the minimum V_{dd} for pseudo-NMOS (NMOS only) designs? You must support your answers through detailed (theoretical) analysis.

Problem 3 Interconnects

Read these papers from the class website:

[1] K. Banerjee, et al, "A Power-Optimal Repeater Insertion Methodology for Global Interconnects in Nanometer Designs," *IEEE Trans. on Elect. Dev.*, 2002

[2] K. Banerjee, et al, "Analysis of On-Chip Inductance Effects for Distributed RLC Interconnects," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 2002

[3] A. H. Ajami, et al, "Modeling and analysis of Nonuniform Substrate Temperature Effects on Global ULSI Interconnects," *IEEE Trans. on CAD*, 2005

Answer these questions:

a) Draw the Equivalent circuits of a driver-interconnect-load segment (Use both RC model and RLC model) for interconnect.

b) Find the optimum interconnect length and repeater size for 180 nm technology.

c) Explain the effect of inductance in interconnect modeling for different technology (180nm, 90nm, 65nm, and 45nm).

d) Explain the effect of driver resistance and driver output capacitance on the step response of the circuit.

e) What is the relation of the repeater size obtained from RC model to the repeater size obtained from RLC model (for different inductance)?

f) What is the relation of the optimum interconnect length obtained from RC model to the optimum interconnect length obtained from RLC model (for different inductance)?

g) Plot the curve of Elmore delay *vs.* maximum wire temperature (assume a minimum wire temperature of 40℃, wire length of 500 μm and 1500 μm, and other configurations of the wire are the same as those in Ajami's paper), for exponential thermal profile and Gaussian distribution thermal profile. Explain briefly how the interconnect delay is affected by the wire temperature.

Problem 4 3D Integration

a) Explain briefly via-first, via-middle, and via-last process. Which one do you prefer in a 3D integration, if you are the process/circuit designer, and why?

b) Read the reference paper (C. Xu, et al, "Compact AC Modeling and Performance Analysis of Through-Silicon Vias in 3-D ICs", *IEEE Trans. on Device*, 2010). Plot the parallel admittance (CG), and serial impedance (RL) vs. frequency for a typical pair of TSVs. Estimate the delay and IR drop induced by a TSV, assuming 22nm high performance MOSFETs.