Tunneling Field-Effect Transistors (TFETs) With Subthreshold Swing (SS) Less Than 60 mV/dec

Woo Young Choi, *Member, IEEE*, Byung-Gook Park, *Member, IEEE*, Jong Duk Lee, *Member, IEEE*, and Tsu-Jae King Liu, *Fellow, IEEE*

***Abstract*—We have demonstrated a 70-nm n-channel tunneling field-effect transistor (TFET) which has a subthreshold swing (SS) of 52.8 mV/dec at room temperature. It is the first experimental result that shows a sub-60-mV/dec SS in the silicon-based TFETs. Based on simulation results, the gate oxide and silicon-on-insulator layer thicknesses were scaled down to 2 and 70 nm, respectively. However, the ON/OFF current ratio of the TFET was still lower than that of the MOSFET. In order to increase the ON current further, the following approaches can be considered: reduction of effective gate oxide thickness, increase in the steepness of the gradient of the source to channel doping profile, and utilization of a lower bandgap channel material.**

***Index Terms*—Subthreshold swing (SS), tunneling field-effect transistor (TFET).**

I. Introduction

As MOSFETs are scaled down, the power supply voltage should also go down in order to reduce power density. For example, a 45-nm low-operating-power devices should have a power supply voltage of 0.9 V [1]. In order to maintain a high ON-state current with an acceptable OFF-state leakage, a reduction of the subthreshold swing (SS) is necessary and has emerged as one of the most important technological issues. However, even in the ideal case of infinite gate capacitance, the SS of MOSFETs cannot be reduced below 60 mV/dec at room temperature. Some novel devices have been proposed to achieve a sub-60-mV/dec SS such as impact-ionization MOS devices [2], [3], nanoelectromechanical FETs [4], suspended-gate MOSFETs [5], and tunneling FETs (TFETs) [6]–[8]. Among them, this letter focuses on the TFET.

The TFET is merely a gated p-i-n diode operating under reverse bias, as shown in Fig. 1. Unlike the MOSFET which uses thermal carrier injection, the TFET utilizes band-to-band tunneling as a source carrier injection mechanism. Fig. 1 shows the band diagrams of the n-channel TFET in the OFF and ON states. In the OFF state, the potential barrier between the source and the channel is so wide that no tunneling occurs. Only a very small leakage current exists. In the ON state, when the gate voltage exceeds the threshold voltage, the potential barrier between the channel and the source becomes narrow enough to allow a significant tunneling current.

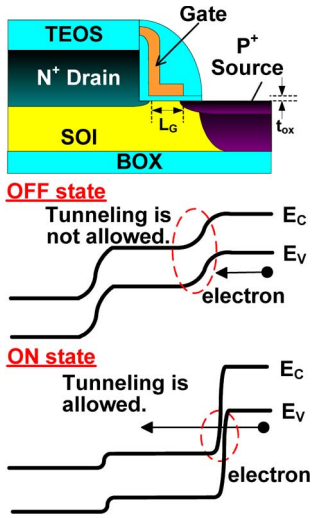

Fig. 1. Device schematic and band diagram in the ON/OFF states of the n-channel TFET.

Since the TFET has a different source carrier injection mechanism than does the MOSFET, it can achieve sub-60-mV/dec SS. Since Wang *et al.* [6] showed the feasibility of the TFET for low-power applications, some interesting studies have been reported. Zhang *et al.* [9] provided a theoretical analysis that the SS value of TFETs can be reduced below 60 mV/dec. Bhuwalka *et al.* [10] showed a vertical Si/SiGe TFET with an SS of 44 mV/dec through device simulation. The first tunneling device which has an SS less than 60 mV/dec was implemented by Appenzeller *et al.* [11] based on carbon nanotube technology. However, in the case of silicon-based TFETs, there has been no experimental result demonstrating sub-60-mV/dec SS.

In this letter, TFETs with an SS that is less than 60 mV/dec have been fabricated on a silicon-on-insulator (SOI) substrate. To the best of our knowledge, it is the first experimental observation of sub-60-mV/dec SS for the silicon-based TFETs.

II. Device Design and Fabrication

Since the output current of the TFET is the tunneling current between the source and the channel determined by the gate

Manuscript received April 18, 2007; revised May 22, 2007. This work was supported by the Korea Research Foundation Grant funded by the Korean Government (MOEHRD) under Grant KRF-2006-352-D00086. The review of this letter was arranged by Editor A. Chatterjee.

W. Y. Choi and T.-J. K. Liu are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA (e-mail: wychoi@eecs.berkeley.edu).

B.-G. Park and J. D. Lee are with the Interuniversity Semiconductor Research Center, School of Electrical Engineering and Computer Sciences, Seoul National University, Shinlim-dong, Gwanak-gu, Seoul 151-742, Korea.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2007.901273

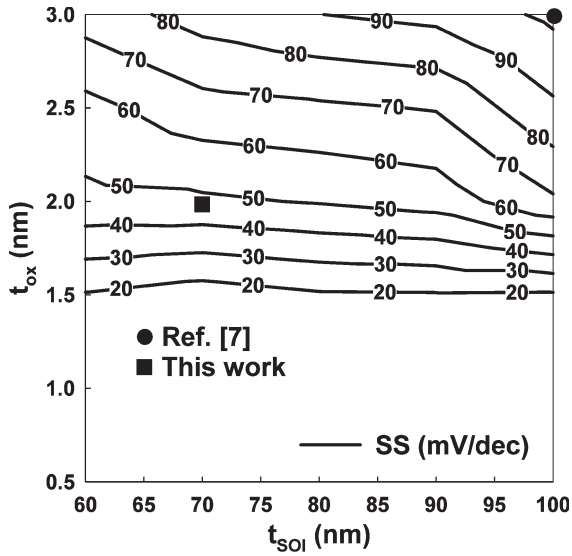

Fig. 2. Variation of the SS value as a function of gate oxide thickness $(t_{\rm ox})$ and SOI layer thickness $(t_{\rm SOI})$.

voltage, its SS value is dependent on several parameters, including the gate oxide thickness $(t_{\rm ox})$, the SOI layer thickness $(t_{\rm SOI})$, and the steepness of the source doping profile. In our recent study, we have successfully fabricated 70-nm n- and p-channel TFETs which have a gate oxide thickness and an SOI layer thickness of 3 and 100 nm, respectively [7]. However, their SS values were still over 60 mV/dec, ranging from 73.2 to 120.6 mV/dec. In order to guide the device design for sub-60-mV/dec SS, 2-D device simulations were performed with Sentaurus using the parameters as in [7]. Fig. 2 shows the dependence of SS on $t_{\rm ox}$ and $t_{\rm SOI}$. The SS value is observed to become smaller as the gate oxide and the SOI layer thicknesses are decreased. This is because the SS value is generally determined by two factors: the coupling between the gate voltage and the channel potential and the influence of the drain voltage on the tunneling barrier. As $t_{\rm ox}$ and $t_{\rm SOI}$ are scaled down, the channel potential becomes more closely coupled to the gate voltage versus the drain voltage, which leads to a decreased SS value. When $t_{\rm ox}$ and $t_{\rm SOI}$ are sufficiently small, the SS value falls below 60 mV/dec.

On the basis of the simulation results, the 70-nm n-channel TFETs were fabricated using the process flow that was previously reported [7]. Fig. 3 shows the scanning-electron-microscope (SEM) images of a fabricated device. Although its layout looks similar to that of the MOSFET due to its novel self-aligned structure, it features a mesa-shaped drain and sidewall spacer gate. In this letter, $t_{\rm ox}$ and $t_{\rm SOI}$ are reduced to 2 and 70 nm, respectively, for sub-60-mV/dec SS.

III. Results and Discussion

Fig. 4 shows the transfer curves of the fabricated 70-nm long n-channel TFET. Normal transistor operation was observed with an SS value of 52.8 mV/dec at room temperature. The threshold voltage was measured to be 0.12 V by using the constant current method [12]. The drain-induced-current-enhancement factor is 51.1 mV/V [13]. The ON and OFF currents were 12.1 μA and 5.4 nA per μm, respectively, at 1-V operation. The drain current increases when the gate is biased around 0 V due to the p-channel TFET operation. Although the TFET exhibits an extremely low SS value, its ON/OFF current ratio is lower than that of the conventional MOSFETs.

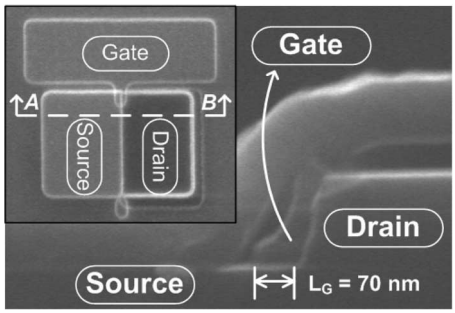

Fig. 3. Cross-sectional SEM image of the fabricated TFET when cutting through the A–B line. Its gate length (L_G) is measured to be 70 nm. The inserted figure shows the plan-view image.

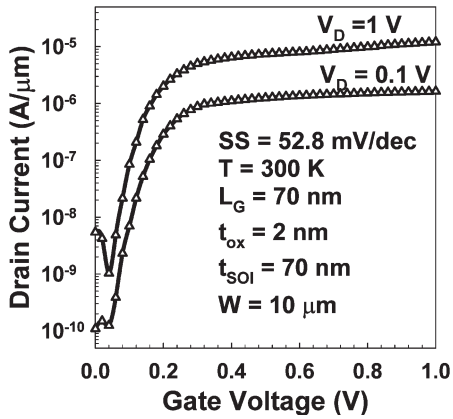

Fig. 4. Transfer curve of the fabricated TFET. The SS value is 52.8 mV/dec at room temperature. The ON and OFF currents were measured to be 12.1 μA and 5.4 nA per μm, respectively, when the power supply voltage was 1 V.

The low ON current stems from the difference of carrier injection mechanisms between the TFET and the MOSFET. It is well known that the band-to-band tunneling current becomes less sensitive to the electric field as the potential difference between the channel and the source increases. Thus, beyond the subthreshold region, it is difficult to achieve large transconductance. For further improvement in the ON current, three approaches can be considered as follows: the use of lower bandgap material, lower equivalent oxide thickness (EOT), and a more abrupt source doping profile. First, the lower bandgap material increases the band-to-band tunneling generation rate which is an exponential function of the bandgap. Thus, the use of SiGe or Ge will increase the ON current. The lower bandgap material can be used in the entire active device area or only in the selected region where the band-to-band tunneling occurs. Since the former option also increases the OFF current dramatically, which leads to lower ON/OFF current ratio, the latter option is more appropriate. Second, the lower EOT contributes to higher ON current by increasing the coupling between the gate voltage and the channel potential. However,

in this letter, we have already used a 2-nm thick silicon oxide. Below 2 nm, the silicon oxide is difficult to use due to direct tunneling leakage. High-κ dielectric material may be needed for further improvement. Lastly, an abrupt source doping profile also helps to increase the ON current by reducing the tunneling-barrier width. However, because the TFET uses the band-to-band tunneling instead of thermionic emission, its ON current is expected to be lower than that of the MOSFET, for the same channel material.

The OFF current of the TFET should be lower than that of the MOSFET since the former is dominated by the leakage current of a reverse-biased p-i-n diodes. However, in this letter, the OFF current is relatively large due to the drain-to-gate leakage current, which is measured to be about 1 nA/μm when the gate is biased at 0 V. Because the fabricated TFET has a mesa-shaped drain for self-alignment, the drain area overlapped by the gate is larger than for the conventional TFET in [6]. What is worse, as gate oxide thickness is scaled down, is that the oxide thickness between the gate and the drain decreases, since the oxide layers are grown using the same oxidation process step. In this letter, the separation gap between the gate and the drain is estimated to be 4 nm. If the two oxide layers are formed separately using an improved process flow, it is expected that the OFF current, in addition to the gate-to-drain capacitance, will be suppressed.

IV. Conclusion

A 70-nm n-channel Si TFET was fabricated with an SS of sub-60-mV/dec at room temperature, for the first time. By reducing the gate oxide and SOI layer thicknesses from [7], the SS value of the TFET reached 52.8 mV/dec. Although the fabricated device showed the MOSFET-like operation with low SS value, its ON/OFF current ratio was still lower than that of the MOSFET. For performance enhancement, the following approaches can be considered: further gate oxide and SOI layer thickness reduction, lower bandgap channel material, abrupt source doping profile, and improved fabrication process.

References

[1] *The International Technology Roadmap for Semiconductors (ITRS)*, 2006. [Online]. Available: http://public.itrs.net

[2] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q," in *IEDM Tech. Dig.*, 2002, pp. 289–292.

[3] W. Y. Choi, J. Y. Song, J. D. Lee, Y. J. Park, and B.-G. Park, "100-nm n-/p-channel I-MOS using a novel self-aligned structure," *IEEE Electron Device Lett.*, vol. 26, no. 4, pp. 261–263, Apr. 2005.

[4] H. Kam, D. T. Lee, R. T. Howe, and T.-J. King, "A new nano-electromechanical field effect transistor (NEMFET) design for low-power electronics," in *IEDM Tech. Dig.*, 2005, pp. 463–466.

[5] N. Abele, N. Fritschi, K. Boucart, F. Casset, P. Ancey, and A. M. Ionescu, "Suspended-gate MOSFET: Bringing new MEMS functionality into solid-state MOS transistor," in *IEDM Tech. Dig.*, 2005, pp. 1075–1077.

[6] P.-F. Wang, K. Hilsenbeck, T. Nirschl, M. Oswald, C. Stepper, M. Weiss, D. Schmitt-Landsiedel, and W. Hansch, "Complementary tunneling transistor for low power applications," *Solid State Electron.*, vol. 48, no. 12, pp. 2281–2286, May 2004.

[7] W. Y. Choi, J. Y. Song, J. D. Lee, Y. J. Park, and B.-G. Park, "70-nm impact-ionization metal–oxide–semiconductor (I-MOS) devices integrated with tunneling field-effect transistors (TFETs)," in *IEDM Tech. Dig.*, 2005, pp. 975–978.

[8] T. Nirschl, M. Weis, M. Fulde, and D. Schmitt-Landsiedel, "Correction to revision of tunneling field-effect transistor in standard CMOS technologies," *IEEE Electron Device Lett.*, vol. 28, no. 4, p. 315, Apr. 2007.

[9] Q. Zhang, W. Shao, and A. Seabaugh, "Low-subthreshold-swing tunnel transistors," *IEEE Electron Device Lett.*, vol. 27, no. 4, pp. 297–300, Apr. 2006.

[10] K. K. Bhuwalka, J. Schulze, and I. Eisele, "Performance enhancement of vertical tunnel field-effect transistor with SiGe in the δp^+ layer," *Jpn. J. Appl. Phys.*, vol. 43, no. 7A, pp. 4073–4078, Jul. 2004.

[11] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, no. 19, pp. 196 805-1–196 805-4, Nov. 2004.

[12] N. Arora, *MOSFET Models for VLSI Circuit Simulation*. New York: Springer-Verlag, 1993.

[13] W. Y. Choi, J. Y. Song, J. D. Lee, Y. J. Park, and B.-G. Park, "A novel biasing scheme for I-MOS (impact-ionization MOS) devices," *IEEE Trans. Nanotechnol.*, vol. 4, no. 3, pp. 322–325, May 2005.