Understanding the Superlinear Onset of Tunnel-FET Output Characteristic

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***Abstract*—In this letter, we report that the source and channel Fermi–Dirac distributions in interband-tunneling-controlled transistors play a fundamental role on the modulation of the injected current. We explain the superlinear onset of the output characteristics based on the occupancy function modulation. Thus, we point out that, along with the tunneling barrier transparency, the availability of carriers and empty states, at the beginning and at the end of the tunneling path, respectively, should be always taken into account for a proper modeling of tunnel FETs.**

***Index Terms*—Band-to-band tunneling (BTBT), steep swing switch, subthermal subthreshold swing, subthreshold slope, tunnel-FET (TFET).**

I. Introduction

DURING the last years, a rising interest of the scientific community on tunnel-FET (TFET) devices has been observed [1], [2]. This has been mainly motivated by the extremely low off-current resulting from their reverse-biased gated p-i-n configuration and by the appealing possibility of achieving subthermal switching slopes owing to their quantum–mechanical band-to-band tunneling (BTBT) carrier injection mechanism.

Together with its remarkable promises as a low-power transistor enabling an aggressive supply-voltage scaling, some intrinsic limitations are still threatening its employment in commercial integrated circuits. Indeed, one of the most important drawbacks is its low-driving-current capability.

In order to overcome this issue, much research has been accomplished toward the improvement of the tunneling barrier transparency, namely, small-band-gap strained heterostructures [3]–[5], light-effective-mass structures as III–V compounds [6] or CNTs [7], [8], and direct-band-gap semiconductors [9]. With the same target of maximizing the tunneling probability, nonconventional architectures featuring high-k gate dielectrics [10] and vertical tunnel devices [11] have also been widely explored.

Nevertheless, as Esaki pointed out already in 1958, a general expression for the elastic tunneling current between "originating region 1" and "destination region 2" is congruent with [12]

$$I_{T,1\to 2} \propto \int P_T(E) f_1(E) G_1(E) \left(1 - f_2(E)\right) G_2(E) dE \quad (1)$$

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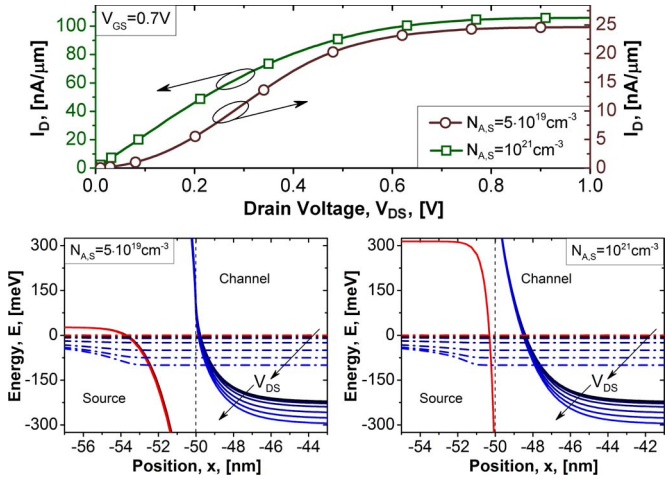

Fig. 1. TCAD finite-element simulation showing (top) the output characteristics and (bottom) the surface band diagrams at the source/channel interface for two silicon TFETs with source doping equal to (left) $N_{A,s} = 5 \cdot 10^{19}$ cm^{-3} and (right) $N_{A,s} = 10^{21}$ cm^{-3}. The metal gate workfunction is 3.975 eV, while 2.5 nm of HfO_2 have been used as gate oxide. The dashed–dotted lines refer to the electron and hole quasi-Fermi levels; $V_{\rm GS} = 0.7$ V and $V_{\rm DS} = \{0; 5; 10; 25; 50; 75; 100\}$ mV.

where P_T is the probability of penetrating the tunneling barrier and f and G are the Fermi–Dirac distribution and the density of states (DOS) of region 1 or 2.

Although sometimes overlooked, (1) shows that a large tunneling current requires not only a tunneling barrier transparent enough but also the availability of carriers (at the initial point of the tunneling event) and the availability of empty states (at the end of the tunneling path) into which the carriers can tunnel.

Together with rigorously defined TFET compact models [13], several analytical approaches have been proposed, consisting of a simple BTBT generation formula that does not take into account the Fermi–Dirac distributions [14], [15]. It is the purpose of this letter to show, through a study of the device output characteristics, that a proper analytical model of TFETs would be even more accurate if, besides the tunneling probability contribution, also the source and channel occupancy functions are taken into account.

Moreover, this work also explains the physical motivation that causes the well-known detrimental onset of the TFET output characteristics [16].

II. Working Principle of TFETs

Fig. 1 shows the simulated output characteristics of two planar silicon n-type TFETs and their conduction and valence bands, along the current transport direction, during the initial $V_{\rm DS}$ sweep. The simulation is performed with the TCAD Synopsys Sentaurus SDevice simulator. Both devices are in

the ON state (i.e., the maximum energy of the source valence band $VB_{s,\max}$ is larger than the minimum energy of the channel conduction band $CB_{\mathrm{ch,min}}$), and a dynamic nonlocal path BTBT model [17] takes self-consistently into account the device tunneling current.

A. Occupancy Probability Contribution

To gain a better insight on the relation between the tunneling current and the Fermi–Dirac distributions, for the first part of this study, we assume that the tunneling barrier is perfectly transparent inside the allowed tunneling energy window (i.e., $P_T\{CB_{\mathrm{ch,min}} < E < VB_{s,\max}\} = 1$) and zero if otherwise. Moreover, for a small tunneling window, the DOS can be considered independent of the energy. In this case, we can express the total tunneling current (resulting from the two contributions of current from the valence band to the empty states of the conduction band and from the conduction band to the empty states of the valence band [12], [17]) as proportional to

$$I_T \propto \int_{CB_{\mathrm{ch,min}}}^{VB_{s,\max}} [f_s(E) - f_{\mathrm{ch}}(E)]\, dE. \tag{2}$$

With a simple change of variables, the aforementioned integral can be expressed as a difference of complete Fermi integrals of order 0

$$\begin{aligned} I_T &\propto [F_0(\alpha) - F_0(\beta) - F_0(\gamma) + F_0(\delta)] \\ &= \ln\left\{\frac{[1+\exp(\alpha)]\,[1+\exp(\delta)]}{[1+\exp(\beta)]\,[1+\exp(\gamma)]}\right\} \end{aligned} \tag{3}$$

where the arguments α, β, γ, and δ are defined as

$$\begin{aligned} \alpha &= \frac{E_{\mathrm{Fp},s} - CB_{\mathrm{ch,min}}}{k_B T} & \beta &= \frac{E_{\mathrm{Fp},s} - VB_{s,\max}}{k_B T} \\ \gamma &= \frac{E_{\mathrm{Fn,ch}} - CB_{\mathrm{ch,min}}}{k_B T} & \delta &= \frac{E_{\mathrm{Fn,ch}} - VB_{s,\max}}{k_B T} \end{aligned} \tag{4}$$

where $E_{\mathrm{Fp/n,s/ch}}$ denotes the hole and electron quasi-Fermi energy levels of the source and channel, respectively.

As pointed out in the bottom diagrams in Fig. 1, when the TFET operates in the ON state, the drain bias controls both the channel conduction band and the electron quasi-Fermi level at the source/channel interface so that $dE_{\mathrm{Fn,ch}}/dV_{\mathrm{DS}} = dCB_{\mathrm{ch,min}}/dV_{\mathrm{DS}} = -1$. In this work, the hole quasi-Fermi level of the source has been taken as reference for the energy (thus, $E_{\mathrm{Fp},s} = 0$ eV). This means that the parameter β depends on the source degeneracy only, α and δ linearly depend on V_{DS}, and γ can be considered independent of the drain bias under the condition that both $CB_{\mathrm{ch,min}}$ and $E_{\mathrm{Fn,ch}}$ decrease one-to-one for increasing V_{DS}.

Assuming that the tunneling current is the dominant contribution to the device drain current, from (3), it is straightforward to evaluate the output conductance derivative as

$$\frac{\partial^2 I_T}{\partial V_{\mathrm{DS}}^2} \propto \frac{\exp(-\alpha)}{[1+\exp(-\alpha)]^2} + \frac{\exp(\delta)}{[1+\exp(\delta)]^2}. \tag{5}$$

B. Tunneling Probability Contribution

As far as the tunneling probability is concerned, its contribution has been deeply studied and analyzed in the literature. For the purpose of this work, the following approximate expression is used:

$$P_T(E) \approx \exp\left\{-2\int_{x_h}^{x_e}\sqrt{\frac{2m_r}{\hbar^2}\,[CB(x) - E]}\,dx\right\} \tag{6}$$

where x_h and x_e are the spatial coordinates at the beginning and at the end of the tunneling path, respectively, and m_r is the reduced effective mass.

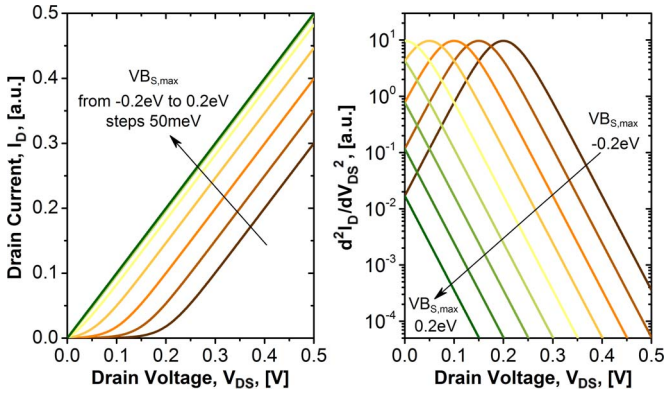

Fig. 2. (Left) Output characteristics and (right) derivative of the output conductance for different source degeneracies. Both plots feature values for $VB_{s,\max}$ ranging from -0.2 to 0.2 eV, with steps of 50 meV.

III. Discussion

According to the degeneracy of the source Fermi level (i.e., $VB_{s,\max} - E_{\mathrm{Fp},s}$) and to the gate voltage (that affects both $E_{\mathrm{Fp},s} - CB_{\mathrm{ch,min}}$ and $E_{\mathrm{Fn,ch}} - CB_{\mathrm{ch,min}}$), the TFET $I_D - V_{\mathrm{DS}}$ curve assumes different shapes.

We consider in the following that the channel conduction band energy at $V_{\mathrm{DS}} = 0$ V is smaller than both $VB_{s,\max}$ and $E_{\mathrm{Fp},s}$ by at least three times the thermal energy $k_B T$. This is, by far, the most common case for conventional all-silicon TFETs operating in the ON state. In this case, the output characteristic can have two different behaviors according to the source degeneracy. In particular, we have the following (see Fig. 2).

1) $VB_{s,\max} > 3k_B T$ that is the condition for a degenerate source. In this case, the drain current is linearly dependent on the drain-to-source voltage drop, since (3) can be approximated as $I_D \propto -E_{\mathrm{Fn,ch}}$. Consequently, this case presents an output conductance derivative proportional to

$$\frac{\partial g_0}{\partial V_{\mathrm{DS}}} \propto \exp\left(\frac{E_{\mathrm{Fn,ch}} - VB_{s,\max}}{k_B T}\right). \tag{7}$$

2) $VB_{s,\max} < -3k_B T$ that is the case with a nondegenerate source. Under this condition, both terms in (5) are equally contributing in the output conductance derivative, and it reaches its maximum when $E_{\mathrm{Fn,ch}} = VB_{s,\max}$. Each term gives rise to one asymptote: the first with exponentially increasing values for increasing V_{DS} going from zero to $V_{\mathrm{DS}} = -VB_{s,\max}/q$ and the other with exponentially decreasing values for $V_{\mathrm{DS}} > -VB_{s,\max}/q$. In this case, the output characteristic shows the well-known

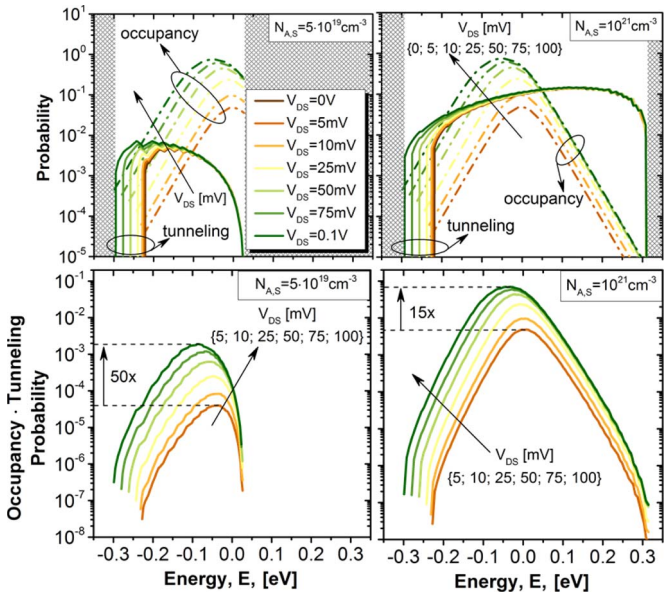

Fig. 3. (Top) Numerical evaluation of the occupancy [that is the integrand of (2)] and tunneling [that is (6)] probabilities for the (left) low- and (right) large-source-doping TFETs whose energy band diagram is shown in Fig. 1. (Bottom) Product of tunneling and occupancy probabilities.

detrimental superlinear onset commonly observed in both simulations and experimental works.

Fig. 2 summarizes the analysis mentioned so far by showing the numerical evaluation of (2) and its second derivative for different doping values corresponding to source valence band energies ranging from -0.2 eV (nondegenerate source) to 0.2 eV (degenerate source).

It is worth observing that the drain current of real TFETs cannot increase arbitrarily, but there is a drain saturation voltage, after which the device current becomes independent of the drain bias. From a physical point of view, this is related to the saturation of the channel conduction band, whose energy cannot be decreased anymore by increasing drain biases. Since this effect has not been taken into account in the analysis presented here, the drain curves shown in Fig. 2 increase indefinitely inside the explored bias range.

Finally, Fig. 3 shows that the modulation of the device current at the beginning of the $V_{\rm DS}$ sweep is mainly determined by a change in the occupancy functions and it is almost independent of the tunneling probability modulation. Thus, as important conclusion, this work shows that the main cause of the superlinear output onset is not the exponential dependence of the device current on the tunneling path. As a matter of fact, while the study of the tunneling barrier is indeed important when understanding the TFET behavior [18], an explanation based on the sole tunneling probability is not enough, and the analysis of the occupancy function dependence on the bias has to be necessarily taken into account.

IV. Conclusion

We have presented strong arguments as to why, for all the TFET models and studies based on a semiclassical description of the BTBT mechanism, the analysis of the sole tunneling probability is not accurate enough if the occupancy functions at the beginning and at the end of the tunneling path are not taken into account as well. We have also found out that the cause of the superlinear onset of the TFET output characteristic should not be related to a modulation of the tunneling barrier but rather to the selection of the allowed energy window where the variation of the occupancy functions can be more or less important. This can be further exploited in the design of TFET architectures to eliminate the superlinear onset of the output characteristic that is detrimental for circuit delay operation.

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