Steep-slope Tunnel Field-Effect Transistors using III-V Nanowire/Si Heterojunction

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Abstract

In this paper, we propose tunneling field-effect transistors (TFETs) using III-V nanowire (NW)/Si heterojunctions and experimentally demonstrate steep-slope switching behaviors using InAs NW/Si heterojunction TFET with surrounding-gate architecture and high-*k* dielectrics. Control of resistances in this device structure is important for achieving steep-slope switching. A minimum subthreshold slope (SS) of the TFET is 21 mV/dec at V_{DS} of 0.10 – 1.00 V.

Introduction:

Si VLSI confront with huge power dissipation owing to increment of transistor integration because transistor scaling has inherent limitations such as enhanced off-state leakage current and short channel effect. The FETs with lower off-state leakage and steeper subthreshold slope (SS) are required for low-power LSI. However, conventional FETs have a physical limit of SS due to carrier thermal diffusion (SS = 2.3 k_BT/q ~ 60 mV). This saturates a scaling of the power dissipation even if a multi-gate structure and III-Vs are applied. Steep-slope transistors such as tunnel FETs (TFETs) [1-4] and impact ionization FETs [5] have therefore been proposed to overcome the limitation. Among steep-slope transistors, TFETs are promising transistor to achieve steep-slope SS with low power. Here, we propose TFET using III-V NW/Si heterojunctions and demonstrate steep-slope TFET based on InAs NW/Si heterojunction with surrounding-gate architecture.

TFET using III-V NW/Si heterojunctions

Fig. 1 illustrates TFET using III-V NWs/Si heterojunctions. Each TFETs are composed of a combination of III-Vs and Si in order to utilize Zener tunnel mechanism working at a band discontinuities across the III-V and Si junctions [6,7]. The TFETs shown in Fig. 1(a) and (b), Si is used as the source region and the III-V NWs are used as drain and gate regions. Fig. 1(c), (d) uses the III-V NWs as source and Si used as gate and source. The III-V NWs in all TFETs are grown by selective-area growth [7-9]. The planar type TFET in Fig. 1(c), (d) smoothly fit into Si-CMOS technologies. At first, we focus on a surrounding-gate TFET using InAs NWs/ Si heterojunction in order to prove a potential of our TFET using III-V NWs/Si heterojuction and to set key parameters for achieving steep-slope behavior in the preliminary TFETs.

NW growth and device fabrication

A. Growth of InAs NWs on Si: Figure 2 illustrates the procedures for selective-area MOVPE. The opening diameters ranged from 30 to 90 nm. Vertically aligned InAs NWs were grown by specific growth sequence to make (111)B surface on Si(111) [8]. During the growth, mono-silane (SiH_4) gas was used to make n^+-InAs/undoped InAs axial junction shown in Fig. 3(a). Fig. 3(b) depicts SEM image of the InAs NWs

B. Device fabrications*:* After the NW growth, the vertical TFET was fabricated by using etch-back process shown in Fig. 4. The gate length was 200 nm.

Results and discussions

Figure 5 shows device performance of the TFET using InAs NWs/Si heterojuction. Switching behavior with a SS of 104 mV/dec (V_{DS} = 0.50 V) was obtained under reverse bias condition. The ratio of on-state/off-state current was about 7×10^4. The threshold voltage (V_T) was – 0.25 V. These device performances correspond to the simulated values using all InAs-based TFET [10]. The output characteristic shown in inset of Fig. 5 exhibits I_D was sub-linearly increased with increasing V_{DS}. The transfer characteristic in Fig. 6 showed no hysteresis curve and inset exhibits low leakage current (I_G) as a function of V_G, which indicates better interface quality of dielectrics/InAs. Although the switching behavior of the TFET was based on Zener tunnel, the SS showed a large value.

Since the SS of TFET is expressed as a function of V_G owing to Zener tunnel current [3], optimization of series resistances in TFET structure is important for biasing the V_{DS} effectively to tunnel junction, which results in small V_G operation, that is, steep slope switching. Fig. 7 illustrates series resistances of the TFET. R1, R2, and R3 are contact, undoped InAs, and heterojunction resistance. We found that lower R1, higher R2, and higher R3 are required for attaining steep slope behavior in the TFET. We therefore enlarged a drain region to reduce R1 and decreased NW-diameter to enhance the R3. This is because that numbers of misfit dislocation at the InAs/Si heterojunction is decreased with decreasing the NW-diameter in Fig. 8, which suppress a phonon-assisted tunneling via the defect states.

Fig. 9 and 10 shows the transfer characteristics at the V_{DS} = 1.00 and 0.10 V. The NW-diameter was 30 nm. Minimum SS reached to 21 mV/dec at V_{DS} = 1.00 V. The on/off ratio was approximately 10^6 at V_{DS} = 1.00 V. The on-state current was 1.0 μA/μm at V_{DS} = 1.00 V and 1 nA/μm at V_{DS} = 0.10 V. Fig. 11 exhibits distribution of the SS in several TFETs with a NW-diameter of 100 and 30 nm. The average SS was 25 mV/dec for TFETs with a NW-diameter of 30 nm.

Conclusion

We have proposed TFETs using III-V NWs/Si heterojunctions and demonstrate steep-slope TFETs with surrounding-gate architecture with high-k dielectrics. In this study, control of series resistances by changing NW-diameter of the TFET was found to be effective approach to attain steep-slope (SS < 60 mV/dec) behaviors.

References

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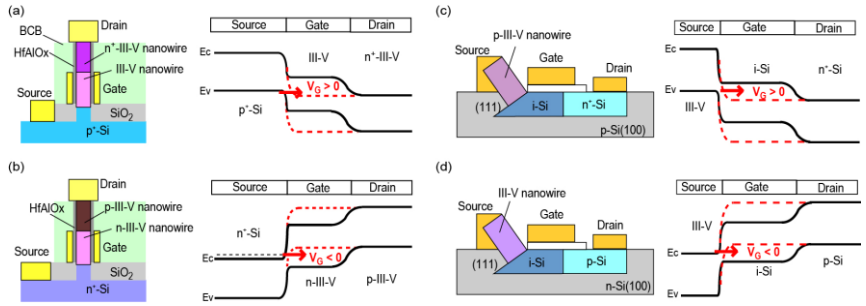

Fig. 1 Schematics of TFETs using III-V NWs/Si heterojunctions. (a),(b) vertical surrounding-gate type TFETs on Si(111) surfaces using Si as source and III-V NWs as gate and drain region. (c), (d) planar type TFET on Si(100). III-V NWs are used to serve as source regions. III-V NWs are grown by selective-area growth on KOH-etched {111} surface on the i-Si. (a) n-type TFETs. The on-state is attained under positive V_G bias. (b) p-type TFETs. (c) n-type TFETs in which he on-state is attained under $V_G > 0$ V. (d) p-type TFETs in which the on-state is attained under $V_G < 0$ V.

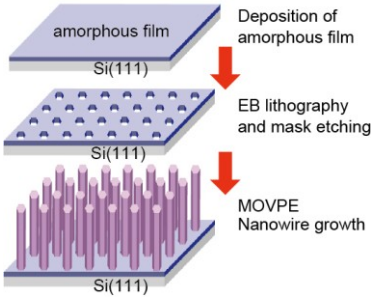

Fig. 2 Procedures for selective-area growth of III-V NWs on Si. After the Si substrate is decreased with organic solvents, 20 nm-thick SiO_2 is formed on Si(111). By using electron-beam (EB) lithography and wet etching, openings are formed. MOVPE is then performed to grow III-V NWs.

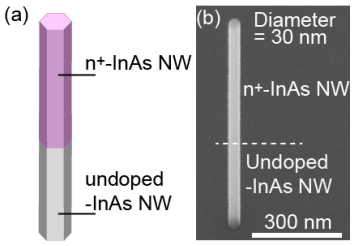

Fig. 3 (a) Illustration of n^+-InAs/undoped-InAs axial junction. (b) Representative SEM image of the NW. The NW-diameter is 30 nm.

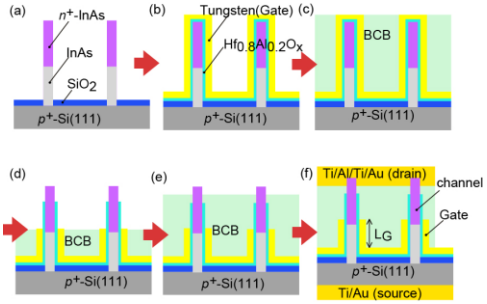

Fig. 4 Device fabrication processes: (a) InAs NW growth. (b) ALD of $Hf_{0.8}Al_{0.2}O_x$ and sputtering of W-gate metal. (c) Spin-coating of BCB polymer. (d) RIE of BCB, gate oxide and W metal. (e)BCB and RIE etch back for electrical separation layer formation. (f) Drain and source metal evaporation.

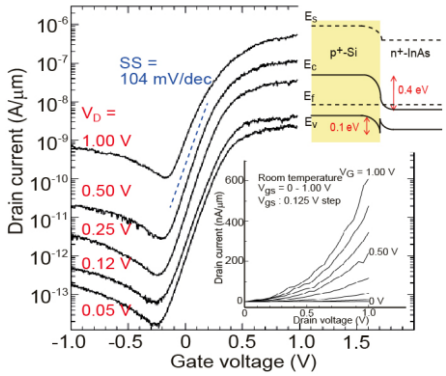

Fig. 5 Transfer characteristic of the TFET using InAs NW/Si heterojunction. The NW-diameter is 90 nm.

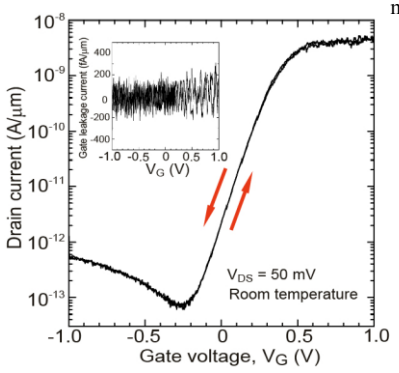

Fig. 6 Transfer characteristics under bidirectional sweeps at V_{DS} = 50 mV. Inset shows the gate leakage current with a variation of V_G. The IG was below ± 200 fA/μm at V_{DS} = 50 mV.

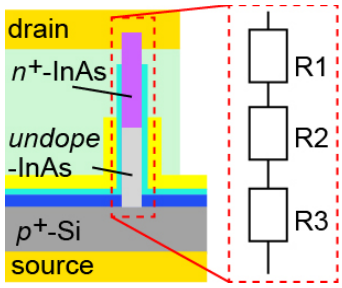

Fig. 7 Schematics of series resistances in the TFET. R1 stands for contact resistance. R2 means a resistance of undoped InAs region. R3 is a resistance of InAs/Si heterojunction owing to band discontinuity.

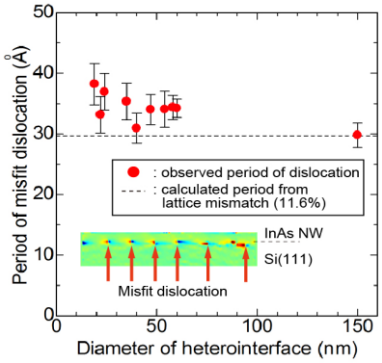

Fig. 8 Period of misfit dislocation at InAs NW/Si interface as a function of NW-diameters. Inset shows strain mapping of the interface. Arrows indicate position of misfit dislocation.

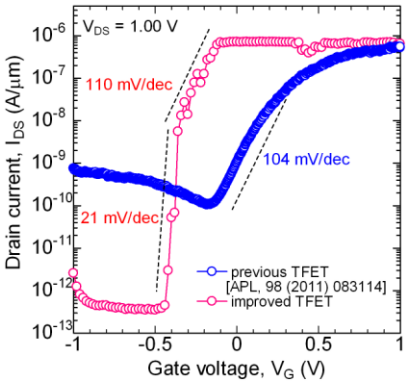

Fig. 9 Experimental transfer characteristics of optimized TFET with a NW-diameter of 30 nm (pink curve) V_{DS} = 1.00 V.

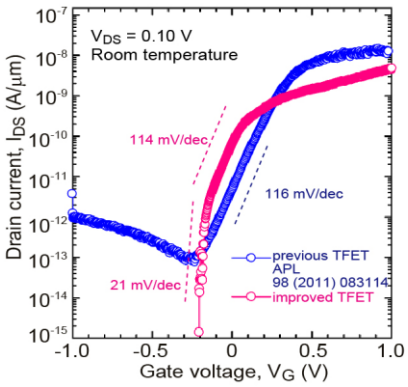

Fig. 10 Experimental transfer characteristics of optimized TFET with a NW-diameter of 30 nm (pink curve) V_{DS} = 0.10 V.

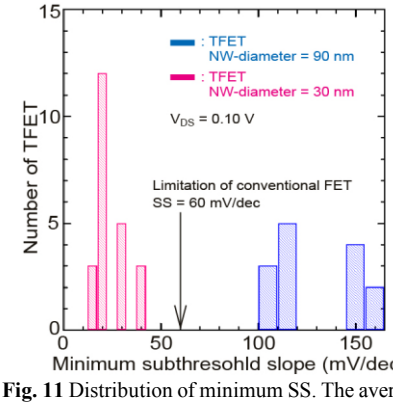

Fig. 11 Distribution of minimum SS. The average SS for TFETs with NW-diameter of 30 nm is 25 mV/dec, which is much lower than the physical limit of SS in conventional MOSFETs.