NANO LETTERS

Letter

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Sub 60 mV/decade Switch Using an InAs Nanowire–Si Heterojunction and Turn-on Voltage Shift with a Pulsed Doping Technique

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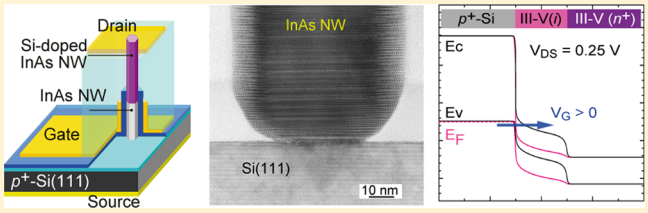
Supporting Information

ABSTRACT: We report changes of turn-on voltage in InAs-Si heterojunction steep subthreshold-slope transistors by the Zn-pulsed doping technique for InAs nanowire channels. The doping of the nanowire channel moderately changes turn-on voltage from negative to positive voltage, while keeping a steep subthreshold-slope of 30 mV/decade under reverse bias direction. The formation of pseudointrinsic InAs segment is found to be important to make a normally off transistor with a steep subthreshold slope.



KEYWORDS: *III–V nanowire, selective-area growth, doping, novel transistor*

Silicon-based integrated circuits are confronted with huge power dissipation owing to inherent problem in size-scaling of field-effect transistors (FETs) such as large off-state leakage current and enhanced short channel effect.[1] New multigate configurations[2,3] and fast channel materials such as III–V[4−6] and germanium[7,8] are promising candidates for reducing power consumption. Further power-scaling, however, will be stopped by carrier thermal diffusion limit of FETs.[9] An effective approach for reducing power consumption in every switches is the use steep subthreshold-slope transistors,[10−12] in which the current involves tunnel[13,14] and impact-ionization[15] mechanisms rather than the thermal diffusion of carriers.

Switching current in conventional field-effect transistors (FETs) involves carrier thermal diffusion mechanism, and their subthreshold-slope (SS) is limited to $2.3k_BT/q \sim 60$ mV/dec at room temperature. This physical limitation prevents further scaling of power consumption in integrated circuits (ICs). A steep-SS transistor with SS < 60 mV/dec are, therefore, required for further reduction in supply voltage (V_{DD}) and power dissipation[1] because the power is proportional to the V_{DD}^2 and the V_{DD} is proportional to the SS. Then, the realization of the steep SS transistors with SS < 20 mV/dec can simply reduce the total power consumption of ICs by over 90%. Therefore, various steep SS transistor such as tunnel FETs (TFETs) using Si,[16,17] III–V materials,[10,11,18] graphene,[19,20] and semiconductor nanowires (NWs)[21,22] have been investigated. All of them, however, have a difficulty in obtaining a steep SS (<30 mV/dec) owing to the significant challenges such as precise doping technique to form an abrupt p–i–n junction. In this regard, a combination of Si and III–V NW materials could provide a decisive solution to the problem because III–V NW/Si heterojunction has an inherently abrupt interface with a band discontinuity.[23,24] Recently, we have demonstrated steep-SS turn-on behavior using InAs NW/Si heterojunction.[25] In this Letter, we report on a modulation of the turn-on voltages of the steep-SS transistor using InAs NW/Si heterojunction by using the Zn-pulse doping technique.

In the experiment, *p*-type Si(111) (carrier concentration; 1×10^{17} to 1×10^{20} cm^{-3}) substrates were used as a starting materials. The process of selective-area growth (SAG) has been previously reported.[26] The details of the SAG are described in Supporting Information (see in Supporting Information Figure S1). Figure 1a illustrates a vertical transistor using InAs NW/Si heterojunction. This architecture is based on surrounding-gate structure; the carrier transport process is assumed to be Zener tunneling current generated at the InAs NW/Si heterojunction, and the current is modulated by gate bias (V_G). InAs NW/Si[11,23,27] can generate large Zener tunneling current across the heterointerface under reverse bias condition. Two-terminal devices composed of the InAs NW/Si shows both Esaki tunneling and the Zener tunneling transport by changing position of Fermi level of the *p*-Si (see Supporting Information S.2). In this case, InAs NWs are used to serve as the channel and source regions. This heterojunction transistor can achieve low off-state current (I_{OFF}) because the heterojunction acts as the barrier against carriers under low V_G. Simulation of band-diagram in Figure 1b indicates the n-type (normally off) can be constructed.

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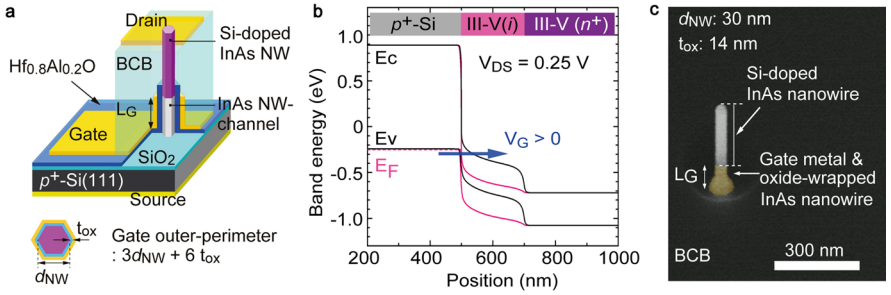

Figure 1. (a) Vertical transistor using InAs NW/Si heterojunction. Surrounding-gate configuration of InAs NW/Si heterojunction. Each InAs NW has a Si-doped InAs/undoped InAs stacked junction with a diameter of 30 nm. At the heterojunction, the diameter of the heterojunction is <30 nm because of isotropic wet etching of SiO_2. The NW is wrapped with $Hf_{0.8}Al_{0.2}$ gate oxide with a thickness of 14 nm and tungsten gate metal. The drain metal is a Ti/Al/Ti/Au multilayer. The gate length is 200 nm. The outer perimeter of the gate is 174 nm. (b) Band diagram simulated by using the one-dimensional Poisson−Schrödinger equation. Under $V_{DS} > 0$, positive V_G induces Zener tunneling transport from *p*-Si to the III−V NW. (c) Representative SEM image showing the vertical transistor.

We fabricated the transistor using single InAs NWs with a diameter (d_{NW}) of 30 nm in Figure 1c. The device process is same as the previous report.[23,25] The NW has axially stacked an Si-doped ($n \sim 1 \times 10^{19}$ cm^{-3}) and undoped layer ($n \sim 1 \times 10^{17}$ cm^{-3}). The gate-oxide is $Hf_{0.8}Al_{0.2}O$ with the effective oxide thickness of 2.67 nm. The diameter of InAs NW/Si heterointerface was 15 nm, and the diameter of the InAs NW was 30 nm. The gate outer-perimeter was 174 nm when d_{NW} = 30 nm.

The effect of the reduction in d_{NW} results in an enhancement of heterojunction resistance. We fabricated a number of heterojunction made with InAs, $In_{0.7}Ga_{0.3}As$, and GaAs NWs on Si. Figure 2a shows a representative scanning electron microscope (SEM) image of InAs NWs on Si(111). Previous works have achieved align only vertical alignment of III−V NWs on Si(111) with various diameters. The transmission electron microscopy (TEM) image in Figure 2b shows that the heterojunction of InAs NW/Si is atomically flat and has no defect such as threading dislocation and antiphase domains, whicgh is usually formed in III−V thin film growth on Si. (Other TEM images for III−V NW/Si heterojunctions are shown in the Supporting Information Figures S.3−S.5.) On the other hand, the strain mapping calculated from the TEM image[26,28] (Figure 2c) reveals that the number of misfit dislocations in grown III−V NW/Si interfaces falls appreciably below the calculated numbers from their lattice mismatch. InAs NW/Si and InGaAs NW/Si had larger lattice mismatch of 11.6 and 8.1%, respectively, but the effective lattice mismatch of these III−V NWs on Si decreased as the diameter decreased; for example, the numbers of the misfit dislocations for InGaAs NW with a diameter of 18 nm is the same as that of GaAs/Si (4.1%, purple dashed curve in Figure 2d). As for GaAs NW on Si, the misfit dislocation completely vanished with a diameter of 19 nm which is coherent growth. This diameter scaling effect on the formation of misfit dislocation is resulted from the reduction of strain field owing to the nanometer-scale footprint of NW, which has been already predicted by some calculations.[29,30] Thus, these heterojunction with small d_{NW} and a fewer misfit dislocation quantitatively suppress trap-assisted tunneling via dislocation levels[27] and dominate pure band-to-band tunneling process. The reduction on d_{NW}, therefore, increases heterojunction resistance.

The device characteristic with undoped InAs NW-channel, showing a pink curve in Figure 3, demonstrated the steeper SS with a minimum SS of 12 mV/dec at V_{DS} = 1.00 V and average SS of 21 mV/dec within 5 decades (see the Supporting

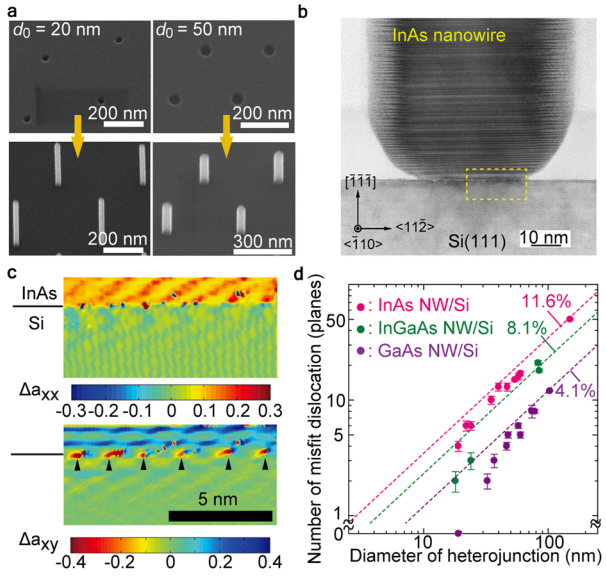

Figure 2. (a) Representative SEM images showing selective-area growth of vertical InAs NWs on Si. The NW has a hexagonal pillar shape surrounded by six-sided {−110} planes and a (111)B top surface. (b) Representative TEM image of the heterointerface of InAs NW/Si. The incidence of electron-beam is the <−110> direction. The heterojunction has atomically flat interface. (c) Displacement of latticeconstant for *xx*-direction (Δa_{xx}) and *xy*-direction (Δa_{xy}) mappings estimated from a filtered image of dashed squared part in panel b. *xx* is [−1−12] direction, and *xy* is [001] direction. (d) Numbers of misfit dislocation at III−V NW/Si heterojunction with a variation of diameter of heterointerface. Dashed lines are calculated values from the lattice mismatch. The close squares are the experimental data counted from the mapping and the TEM images.

Information, Figure S6).[25] Although the output characteristic shows imperfect characteristics as compared to that of typical field effect transistors, showing a large turn-on voltage shift and sublinear dependence without pinch-off properties (see the Supporting Information, Figure S7), the on-state current (I_{ON}) reached to 1.0 $\mu A/\mu m$, and the off-state current (I_{OFF}) was achieved to <1 $pA/\mu m$ at V_{DS} = 1.00 V which is much smaller than the I_{OFF} of conventional Si-based FETs. A more detailed study in terms of reduction in series resistance, specifically heterojunction resistance, is required for obtaining the pinch-off behavior. The steeper SS thought to be originated from an enhanced heterojunction resistance, in which the large internal

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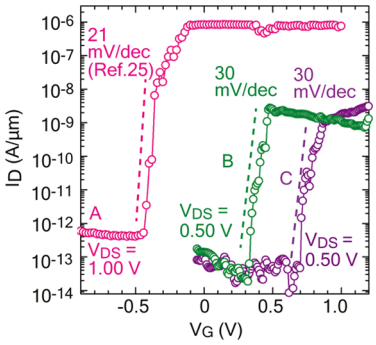

Figure 3. (a) Transfer characteristic of a steep-SS transistor using an InAs NW/Si heterojunction. The pink curve (A)[25] is the transfer characteristic of Figure 1 at V_{DS} = 1.00 V. Curves labeled B (as green curve) and C (as purple curve) show the steep-SS characteristic at V_{DS} = 0.50 V using an InAs NW/Si heterojunction with a Zn pulse doped InAs NW-channel segment with a 1 s pulse at 29 s intervals and Zn-pulse doped InAs NW-channel with a 2 s pulse at 28 s intervals.

field was induced at the heterinterface under the low V_G, because the SS under the tunnel transport mechanism is expressed with a function of V_G and V_{DS}.[10] The transfer curve for the device has two slopes with a SS of 21 mV/dec and 110 mV/dec on average. These two slopes are assumed to be from a coexistence of trap-assisted tunneling and simple band-to-band tunneling process. Since the current was reasonably fit to Kane's tunnel model[31] (see the Supporting Information, Figure S10), the on-state current is thought to be resulted from tunneling process. The device with a larger diameter such as d_{NW} = 80 nm showed a large SS at room temperature.[23] In this case, the trap-assisted tunneling became dominant, and a low heterojunction resistance owing to larger d_{NW} with a large number of misfit dislocations is induced a low internal field by V_G and V_{DS}. On the other hand, in the case of Figure 1c with d_{NW} = 30 nm, the simple band-to-band process became dominant rather than the trap-assisted process because of a few numbers of misfit dislocation. The steeper SS could, therefore, appear in the early stage of applied V_G. These behaviors relating to the d_{NW} predict the realization of coherent growth without misfit dislocation in InAs/Si system which will suppress the large SS region in the transfer curve.

The threshold turn-on voltage (V_T) is −0.42 which is attributed from surface accumulation owing to Fermi level pinning inside the conduction band and an inherently high carrier concentration. Next, we investigate the doping effect of the undoped InAs NW-channel segment. The V_{DS} is still high, and the V_T is negative though the steep SS is achieved with decreasing the d_{NW}. The negative V_T is inadequate performance for the low-power transistor. The undoped InAs NW has unintentional carbon-dopants with carrier concentrations of 10^{16}–10^{17} cm^{-3}.[32] The high carrier concentration induces a low internal field in the InAs NW-channel segment or the heterointerface of InAs NW/Si. As a result, a large internal field under high V_{DS} is required.

The V_T for III–V MOSFETs usually exhibits negative or near zero values with higher carrier concentrations. The formation of an intrinsic InAs segment with suppressing the accumulation is therefore important to control and shift the V_T to positive voltage while avoiding the unintentional doping. Furthermore, a single Zn atom in InAs nanowires with a diameter of 30 nm and 1 nm in height corresponds to 4.7 × 10^{17} cm^{-3} if the single dopant was effectively activated in such a tiny NW. An ordinal doping technique such as coflow will overdose against the small amount of unintentional impurities. Thus, we used the Zn-pulse doping technique for the growth of the InAs NW-channel in order to compensate the unintentional carbon impurity. The flow sequence of the Zn-pulsed doping technique is shown in

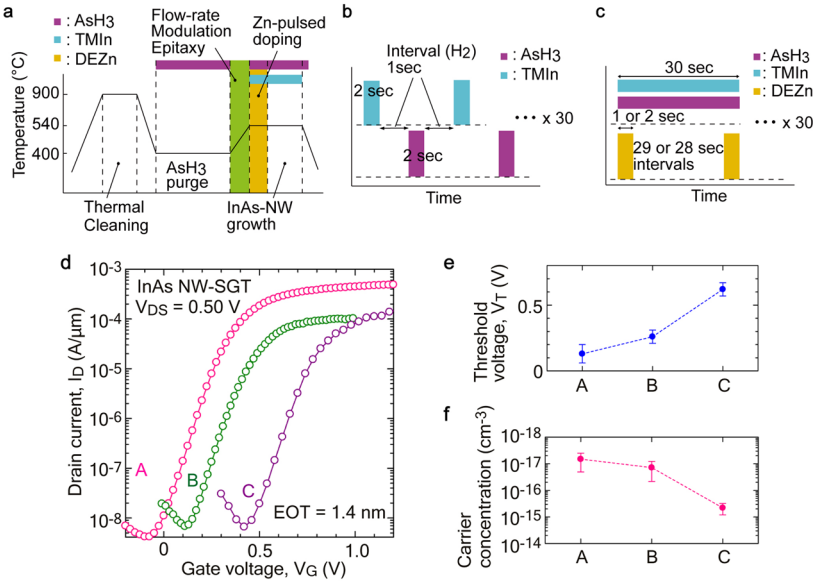

Figure 4. (a) Growth sequence for aligning vertical InAs NWs on Si with the Zn-pulse doping technique. (b) Schematic diagram of flow-rate modulation epitaxy. TMIn (2 s) and AsH_3 (2 s) are alternately supplied with an interval of H_2 (1 s). This sequence is repeated 30 times. (c) Diagram of Zn-pulse doping technique. DEZn (1 or 2 s) are alternately supplied with an interval of 29 or 28 s. This sequence is repeated six times to make pseudointrinsic InAs channel region. (d) The curve labeled A (pink plots) is the transfer characteristic of InAs NW-SGT with an undoped segment. Curves labeled B and C show transfer properties of InAs NW-SGTs with a Zn-pulse doped InAs NW-channel segment with a 1 s pulse with 29 s intervals (green plots) and with 2 s pulse with 28 s intervals (purple plots). (e) Variation of V_T of an InAs NW vertical SGT with a different InAs NW-channel segment. (f) Variation of N_D estimated from the V_T.

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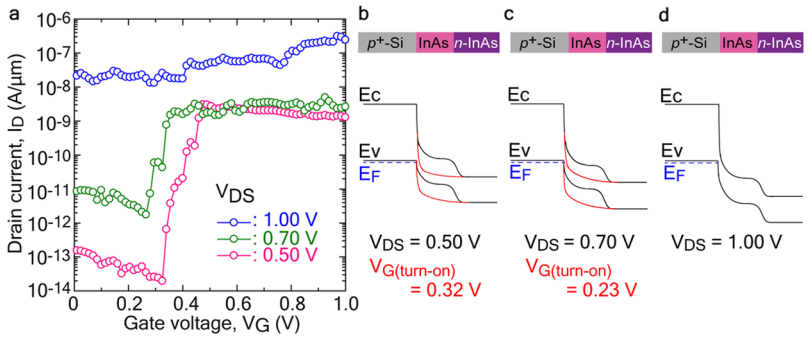

Figure 5. (a) V_{DS} variation of the transfer curve for the steep-SS transistors using InAs NW/Si heterojunction with a Zn-doped InAs NW-channel segment (1 s). (b–d) Illustrations of the band diagram for the steep-SS switch at V_{DS} = 0.50 V (b), 0.70 V (c), 1.00 V (d). Red curves in panel b and c show the band bending under positive gate bias.

Figure 4a–c. In this case, Diethyl Zinc (DEZn) with a pulse of 1 or 2 s are alternately supplied with an interval of 29 or 28 s. This sequence is repeated six times to make the pseudointrinsic InAs channel region. The doping concentration of the technique is estimated to the order of 10^{16} cm^{-3}, and these Zn impurities would compensate the carbon with forming pseudointrinsic InAs channel segment. This resulted in positive V_T shifting from −0.42 V to 0.4 (for Zn-doping with a pulse of 1 s) or 0.60 V (for Zn-doping with a pulse of 2 s) shown in Figure 3. This indicates that "normally-off" steep-SS transistor can be moderately obtained by controlling the channel conductance. The SS maintained sub 60 mV/dec, and the average SS was 30 mV/dec. The V_{DS} for the curves decreased to 0.50 V which means the internal field was effectively induced at the heterointerface or the pseudointrinsic InAs layer under lower bias.

To characterize the actual carrier concentration of the grown InAs NW-channel region, we fabricated the vertical InAs NW-MOSFET by changing the Si substrate from p-type to n-type wafers. The structure is the same as in a previous report.[5] The MOSFET is consists of 10 NW ensembles. By assuming that a Schottky barrier height of the InAs NW-channel is approximately same as the built-in potential (V_{bi}) in the inversion mode of cylindrical coordination, we can roughly estimate the carrier concentration (N_D) from the measured V_T and V_{bi}.[33]

$$V_T = V_{bi} - \alpha N_D \qquad \alpha = \frac{q(d_{NW}/2)^2}{4\varepsilon_0\varepsilon_{InAs}}$$

where ε_{InAs} is the permittivity of the InAs (ε_{InAs} = 12.3). d_{NW} is 70 nm.

Figure 4d shows the variation of V_T of vertical InAs NW MOSFETs with different InAs NW-channel segments. The V_T clearly changed from 0.13 ± 0.07 V for the undoped InAs NW-channel to 0.26 ± 0.05 V for the Zn-compensated InAs NW-channel with the Zn pulse of 1 s or 0.62 ± 0.05 V for that of Zn pulse of 2 s (see the Supporting Information, Figure S9). In addition, the V_{bi} is changed from 0.197 to 0.619 V. Thus, the N_D was approximately estimated to (1.49 ± 0.1) × 10^{17} cm^{-3} for the undoped InAs NW-channel, (7.17 ± 0.8) × 10^{16} cm^{-3} for the InAs NW-channel with the Zn pulse of 1 s, and (2.2 ± 0.3) × 10^{15} cm^{-3} for the InAs NW-channel with the Zn pulse of 2 s. The advantage of the doping technique is to form intrinsic segments in the nanometer-scale materials. Conventional doping by DEZn usually forms *p*-type materials for III-Vs. The Zn-pulse doping technique, therefore, decreases N_D for the InAs NW-channel regardless of the formation of p-type InAs and shifts the V_T toward positive bias; that is, compensation effects of Zn dopants were obtained by the pulsed doping technique. Although the reduction in the N_D by the compensation effect degrades the performance of NW-SGT, the compensated InAs NW-channel can induce a large internal field under reverse bias direction owing to the increment of the channel resistance. Thus, the switching under reverse bias direction works with moderately low V_{DS} and V_G as simulated in Figure 1b. The reduction of the N_D with the Zn-pulse doping technique consequently changes the V_T of the steep-SS transistor.

Figure 5 depicts the transfer curve for the steep-SS switch using the InAs NW-channel by pulsed doping for 1 s under various V_{DS}. The on/off ratio and off-state current increased with increased V_{DS} (in this case reverse bias), and at last the switching behavior was no longer obtained at V_{DS} = 1.00 V. This is because that larger reverse bias narrows the energy gap between the p^+-Si and InAs NW in Figure 5d. Since the SS in ideal tunnel FET is expressed as ln(10) × E_g (E_g is the energy gap between the source and channel),[34] narrowing the energy gap reduces the SS. However, we think this reduction in SS by narrowing the energy gap should be distinguished with gate bias and drain–source reverse bias. In the case of the narrowing the energy gap by reverse V_{DS}, the tunneling leakage always occurs, and the gate bias has no contribution to the switch. In contrast, additional internal field from gate bias is required for narrowing the gap between the Si and InAs under lower reverse bias in Figure 5b and c. Thus, switching behaviors were obtained under lower V_{DS}. These properties in Figure 5 imply that the transport mechanism is based on tunneling such as tunneling FET. Further detailed investigation is, however, required to identify the origin of this sub-60 mV/dec switch.

In summary, we have demonstrated a steep-SS transistor using the InAs NW-Si heterojunction and modified the turn-on voltage of the steep-SS transistor by using the Zn-pulse doping technique. The Zn-pulse doping forms a pseudointrinsic InAs NW-channel owing to the compensation of the inherent carbon impurities by Zn atoms and the shift of the threshold voltage positively as well as the turn-on voltage of the steep-SS transistor. Although we have achieved steep-SS below 60 mV/dec at room temperature, this device has some issues regarding low I_{ON} and the no pinch-off behavior. Detailed investigations such as temperature dependence should be required to bear out the transport mechanism. Moreover, further advanced techniques are required for high I_{ON} and pinch-off under low bias because future low standby power devices in 2025 require on-state current of 360 μm/μm at a supply voltage of 0.54 V.[35]

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After this progress, the III−V NW/Si hererojunction consisting of a 1D nanostructure and their steep-SS transistor would be a good candidate as building blocks for future energy-efficient transistors in integrated circuits.

■ ASSOCIATED CONTENT

Supporting Information

Figure S1, method of selective-area growth; Figure S2, diode characteristics of III−V NW/Si heterojunction; Figures S3−S5, TEM images and strain analysis; Figure S6, minimum SS for the transistor; Figure S7, device performance of the steep-SS transistor; Figure S8, the device design of obtaining steeper SS; Figure S9, estimation of threshold voltage; Figure S10, fitting Kane's tunnel model. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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